1. a. **i)** A transmission gate is formed using an nmos and pmos transistor as shown in your notes. Your diagram should show how the transistors are connected and contain the clearly labelled input, output and control lines. Describe in a couple of sentences the operation of the gate and its main characteristics. **(5)**

ii) Your diagram should show the series nmos connection to ground for a NAND gate but the parallel pmos transistors should be replaced by a pull-up resistor. This can be found in your notes. The operation should be described by considering the state of the transistors (ON or OFF) for each of the four possible input combinations for a two input gate. The output should match that of a standard two input NAND gate truth table. **(5)**

b. The NAND gate will generally perform faster than the NOR gate. Three of the four marks are for describing the reason why. This is related to the mobility of majority carriers and hence, the ON resistance of the transistors. Once you have this information, you can give the reason by applying it to the configurations for a NAND gate and a NOR gate. The series transistor connection is the one to consider. A full explanation is in your notes.

(4)

c. This is extended bookwork from your notes. The important points to consider in your answer are as follows:

i) The sequence of control signals required between the peripheral, the DMAC and the CPU for the entire transaction.

ii) The way that the CPU isolates itself when the DMAC takes control.

iii) Describe how data would be transferred via the CPU without DMA and the problems associated with this; hence describe the circumstances under which DMA would improve matters.

(6)

2. a. The diagram and a description of operation can be found in your notes. **(2)**

For a data write, describe the voltages that must be put on the bit-line and word-line for storage of both a **1** and a **0**. **(2)**

For a data read, describe the voltages that must be put on the bit-line and word-line for storage of both a **1** and a **0**. Describe the pre-charging process and the function of the sense-amplifier. **(3)**

b. A diagram and description can be found in your notes. The key components are a four bit register, a four bit Digital-to-Analog converter and a comparator. Describe how you proceed to set one bit of the register at a time from the MSB until each bit has been applied. **(6)**

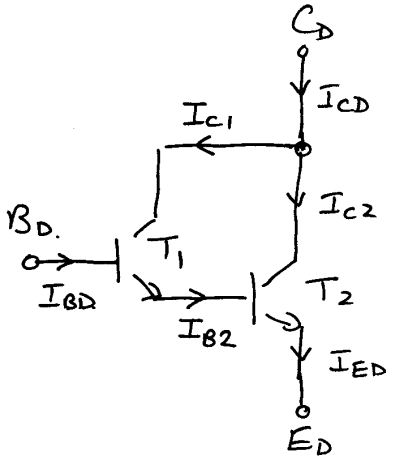
Step1, set SAR to 1000 22.3 is greater than 16 so keep bit
Step2, set SAR to 1100 22.3 is less than 24 so reset bit
Step3, set SAR to 1010 22.3 is greater than 20 so keep bit
Step4, set SAR to 1011 22.3 is greater than 22 so keep bit

Hence 1011 = 22V is the approximation of 22.3V **(4)**

c. This is about aliasing. Describe what this is and under what conditions it occurs. You can then give the reason for including the low-pass filter. **(3)**

EEE 225 June 2014 Q3 + Q4 solution guide.

Q3 (a) (i) The solution to this question lies in finding I_{CD} in terms of I_{BD}. so that the ratio I_{CD}/I_{BD} can be found.



$I_{C1} = h_{FE1} I_{BD}$.

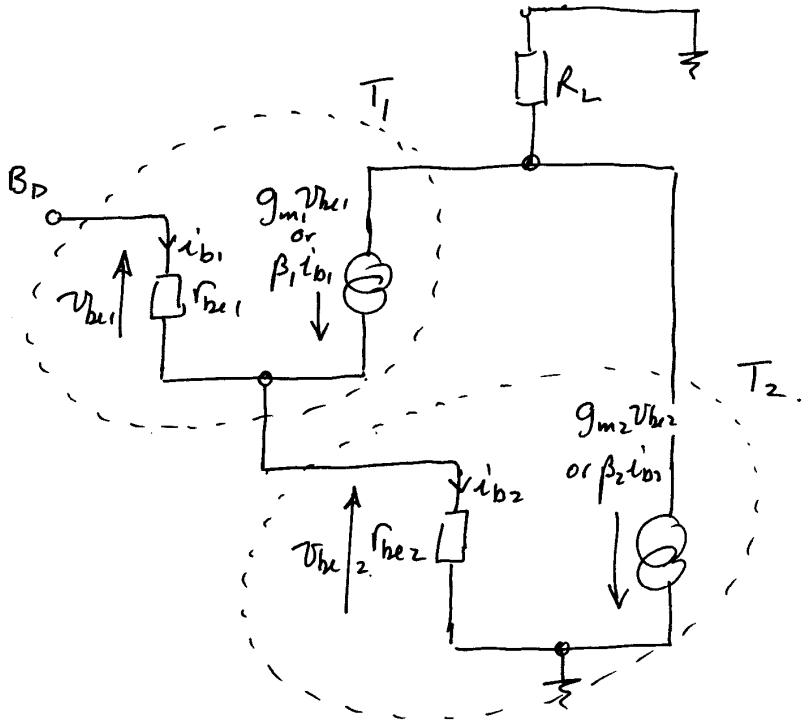
$I_{B2} = I_{E1} = I_{C1} + I_{BD} = h_{FE} I_{BD} + I_{BD}$.

$I_{C2} = h_{FE2} I_{B2}$.

$I_{CD} = I_{C1} + I_{C2}$.

collect terms together and find $\frac{I_{CD}}{I_{BD}}$.

(ii)



(ii) it is important first to recognise that the collector current of T_1 is considerably smaller than that of T_2 since

$$I_{B2} = I_{E1} = \frac{I_{C2}}{h_{FE2}}.$$

You can assume if you like that $I_{E1} \approx I_{C1}$. If you don't make that assumption..

$$I_{E1} = I_{C1} + I_{B1} = I_{C1}\left(1 + \frac{1}{h_{FE1}}\right).$$

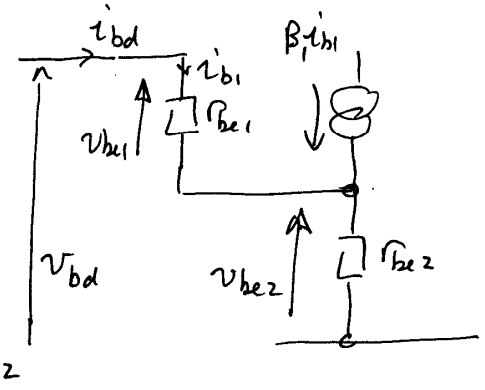
Then you can calculate g_{m1} and g_{m2} and from those obtain r_{be1} and r_{be2}.

[0.385 mA/V, 38.5 mA/V, 520 kΩ, 5.2 kΩ].

$$r_i = \frac{v_{bd}}{i_{bd}} = \frac{v_{bd}}{i_{b1}}$$

$$v_{bd} = v_{be1} + v_{be2}$$

$$i_{b1} r_{be1} \qquad i_{b1}(1+\beta_1) r_{be2}$$



This allows v_{bd} to be expressed in terms of i_{b1} so r_i is easily obtained.

[1.057 MΩ]

Q3(b) (i)

(i) BW of amplifier with gain of 50 and GBP of 40 MHz is given by

$$BW = \frac{GBP}{gain}.$$ [No].

(ii) Here you need to remember that for a first order system, $\tau = \frac{1}{\omega_{3dB}} = \frac{1}{2\pi f_{3dB}}$.

and that rise time $= 2.2\tau$.

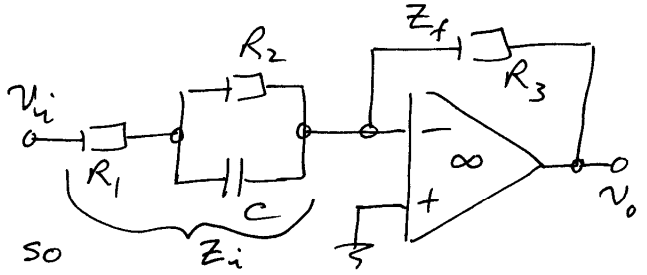
[438 ns].

(iii) You need to remember that the max rate of change of voltage in a sinusoidal waveshape is $V_p\omega$. Note that the question asks for $V_{peak\ to\ peak}$:

[7.96 V]

In parts (ii) + (iii) if you cannot remember the relationships needed they can be derived within a few minutes!

Q4 a.(i)



For l.f. $X_C \to \infty$ so
the $R_1 + R_2 \| \frac{1}{sC} \Rightarrow R_1 + R_2$.

For h.f. $X_C \to 0$ so
the $R_1 + R_2 \| \frac{1}{sC}$ combination $\Rightarrow R_1$
The amplifier is inverting so gain $= -\frac{Z_f}{Z_i}$

(ii) This is simply a matter of manipulating the three relationships given.

$$k = \frac{R_3}{R_1 + R_2} = \frac{R_3/R_1}{1 + \frac{R_2}{R_1}}$$

$$\frac{f_1}{f_0} = \frac{\frac{R_1 + R_2}{2\pi C R_1 R_2}}{\frac{1}{2\pi C R_2}} = 1 + \frac{R_2}{R_1}$$

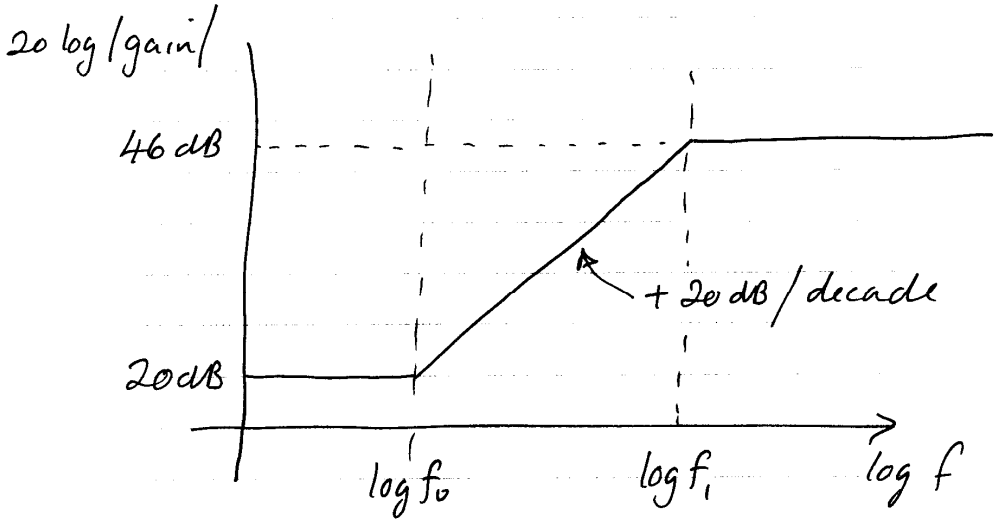
finding $\frac{R_3}{R_1}$ and $\frac{R_2}{R_1}$ from here is straightforward.

$f_0 = \frac{1}{2\pi C R_2}$ leads directly to CR_2

$$\left[3{\cdot}18\,\text{mS},\ 200,\ 19\right]$$

R_3 should have a value somewhere in the range 2kΩ to 1MΩ. A number of combinations of component value are OK.

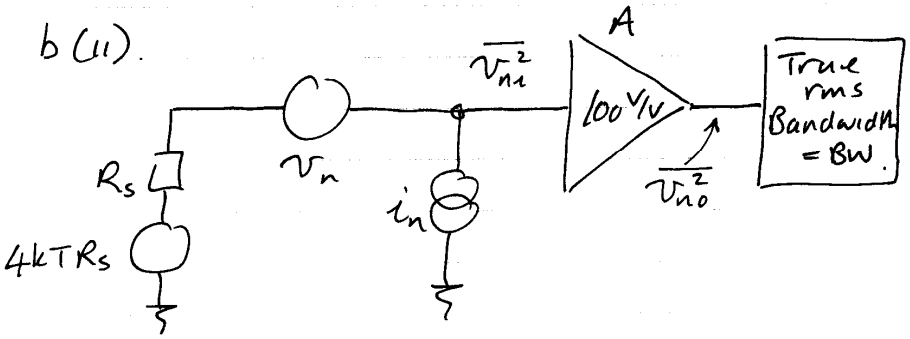
Q4 a.(iii).



You should be able to tell easily from the $\frac{v_o}{v_i}$ expression that l.f. gain < h.f. gain – even if you got part (i) wrong.

b (i) Signal to Noise ratio is what it says. The only thing you need to remember is that it is a mean-squared voltage ratio. S/N measures signal quality at some point in the circuit so it cannot provide any system noise information.

b (ii).



The noise at the amplifier input is due to three contributors

$$\overline{v_{ni}^2} = 4kTR_s + \overline{v_n^2} + \overline{i_n^2}R_s^2 \qquad V^2Hz^{-1}$$

$$\overline{v_{no}^2} = A^2\overline{v_{ni}^2} \qquad V^2Hz^{-1}$$

The meter reads the root of the integrated noise

$$v_{meter} = \sqrt{\overline{v_{no}^2} \times BW} \quad V$$

$[111\mu V]$

b(iii). To get an output signal to noise ratio of unity

$$P_{signal} = \text{integrated output noise}$$

or $$\frac{V_p^2}{2R} = \frac{\overline{v_{no}^2}\, BW}{R}$$

and because R is common to both signal and noise it can be cancelled. This gives V_p^2 at the amplifier output – the question asks for V_p at the input which is of course A times smaller than V_p at the output

$[1.57\mu V]$

EEE 225 2014 Solutions

Q5

a (i) Given N_A and N_D

If $|N_A - N_D| \gg n_i$ it is extrinsic

If $|N_A - N_D| < n_i$ it is intrinsic (2)

Many did not define this properly

(ii) $N_A \approx p$ at RT (1)

(iii) $np = n_i^2$ (1)

(iv) The Fermi Level is the energy where the probability of occupancy by an electron is 50% or 0.5

very few got this part correct (2)

b (i) $\sigma = n_i e(\mu_e + \mu_h) = 2\times10^{12} \times 1.6\times10^{-19} \times 0.89$

$= 2.85 \times 10^{-7}$ or 0.285 if $n_i = 2\times10^{18}\ m^{-3}$ (1)

Doping it increases conductivity by 5×10^5, so

$2.85\times10^{-7} \times 5\times10^5 = 0.1425$ or 0.142×10^6

$n e \mu_e = 0.1425$

$n = 0.1425 / (0.85 \times 1.6\times10^{-19})$

$= 1.05 \times 10^{18}\ m^{-3}$ or 1.05×10^{24} (2)

* To get an LED we need a p-n junction so dope top layer with acceptors

$10^{21}\ m^{-3}$ is sufficient to make it a p-type semiconductor as $(10^{21} - 10^{18}) \gg n_i$ (3)

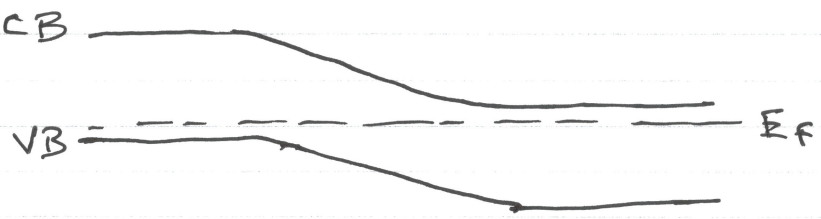
or $10^{25}\ m^{-3}$

(ii) Top layer $N_A = p = 10^{21}\ m^{-3}$ or $10^{25}\ m^{-3}$

$$n = \frac{n_i^2}{p} = \frac{(2\times10^{12})^2}{10^{21}} = \frac{4\times10^{24}}{10^{21}} = 4\times10^3\ m^{-3}$$ (2)

$n_i = 2\times10^{12}\ cm^{-3}$ but many assumed that this was in m^{-3}. I accepted either as OK.

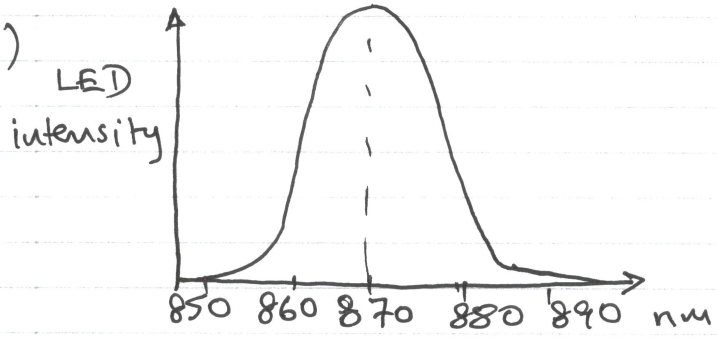
(c)



No problems

LED Band structure in equilibrium (3)

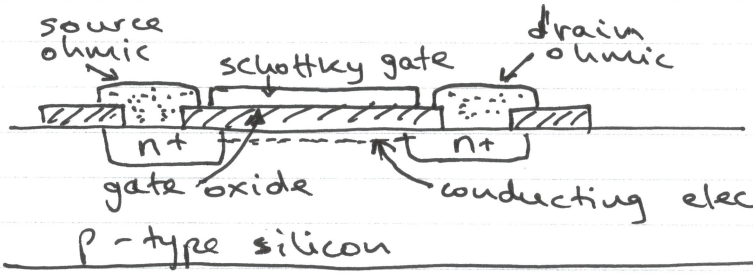
(d)



Mostly OK

(3)

Q6 (a)



A few still got the gate position wrong

(4)

At low tive gate voltage, holes repelled from under gate. At higher V_g, electrons accumulate and form a conducting channel between Source + drain. V_{ds} causes a current to flow between S + D when channel is formed. (2)

(b) (i) Saturation of drain current occurs when $V_{ds} \geq V_{gs} - V_T$

(ii) To obtain I_{ds}, substitute $V_{ds} = V_{gs} - V_T$ into the expression given

$$I_{ds} = \frac{\mu_e C_g}{l^2} \frac{(V_{gs} - V_T)^2}{2}$$

Fairly straightforward

(iii) Transconductance $(g_m) = \left.\frac{d\,Id}{d\,Vgs}\right|_{Vd\ constant}$

$$g_m = \frac{\mu_e C_g}{l^2}(V_{gs} - V_T)$$

(c) $V_{ds} = V_{gs}$ when drain connected to gate

$$I_{ds} = \frac{\mu_e C_g}{l^2}\left(\frac{V_{ds} - V_T}{2}\right)^2$$

Very few got this completely correct.

$I_{ds} = 1mA$ when $V_{ds} = 4V$
$I_{ds} = 2.77mA$ when $V_{ds} = 5V$

$$1mA = \frac{\mu_e C_g}{l^2}\left(\frac{4 - V_T}{2}\right)^2$$

$$2.77mA = \frac{\mu_e C_g}{l^2}\left(\frac{5 - V_T}{2}\right)^2$$

$$2.77 = \frac{(5 - V_T)^2}{(4 - V_T)^2}$$, taking square root

$$(4 - V_T)\,1.66 = 5 - V_T$$
$$6.68 - 5 = 1.66\,V_T - V_T$$
$$1.66 = 0.66\,V_T$$
$$V_T = 2.51\,V \qquad (2)$$

$$1mA = \frac{\mu_e C_g}{l^2}\left(\frac{4 - 2.51}{2}\right)^2 = \frac{\mu_e C_g}{l^2}\,1.11$$

$$0.9\,mA\,V^{-1} = \frac{\mu_e C_g}{l^2} \qquad (1)$$

When $V_{ds} = 6V$, $I_{ds} = 0.9\times10^{-3}\left(\frac{6 - 2.51}{2}\right)^2 = 5.48\,mA$ (3)

(d) $$\frac{\mu_e C_g}{l^2} = 0.9\times10^{-3}\,A\,V^{-1}$$

$$l^2 = \frac{0.15\times10^{-12}}{0.9\times10^{-3}} = 0.166\times10^{-9}\,m^2$$

$l = 12.9\,\mu m$ channel length (2)