

University of Sheffield

Department of Electronic and Electrical Engineering

EEE225: Analogue and Digital Electronics – Analogue Component

2018 - 2019 Edition

Dr. James E Green

Videos of Lectures
Videos of Problem Sheet Solutions
Videos of Extended Material

And

Written Exam Solutions
Written Problem Sheet Solutions
Many past Exam Papers
Past Mid-term Papers

And

Circuit Simulation Files

Are available via MOLE

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The University Of Sheffield.

Electronic & Electrical Engineering.

EEE225 ANALOGUE AND DIGITAL ELECTRONICS

Credits: 20

Course Description including Aims

This module brings together the underlying physical principles of BJT, JFET and MOSFET devices to show how structural decisions in device design affect performance as a circuit element. Basic circuit topologies such as long - tailed pairs, Darlington transistors and current mirrors are described as a precursor to exploring the internal design of a typical op-amp. Common applications of op-amps are discussed. The relationship between device structure and performance in simple CMOS circuits is explored and applied to real digital circuit applications. Digital system design strategies are introduced with examples drawn from everyday embedded digital systems.

The specific aims of the unit are . .

1 Give students an understanding of common transistor device structures and of the way that their design affects the application areas for which a device is useful.

2 Provide foundation knowledge of the operating principles of LEDs, lasers and photo-voltaics.

3 Introduce multi transistor circuit blocks that together can be used to form an operational amplifier.

4 Explore a wide range of linear and non-linear op-amp applications

5 Introduce the concept of noise in analogue circuits and systems.

6 Introduce multi transistor circuit blocks that are the basis of the majority of the logic gates that together form complex VLSI digital systems.

7 Outline the differences between various digital logic families with reference to their input/output properties, speed and power consumption. Highlight currently popular families.

8 Review the area of finite state machines and their relationship to programmable systems and extend the discussion to programmable logic and FPGAs.

9 Explore the anatomy of a simple microcontroller system including memory organisation, hardware/software trade-off and speed and present some everyday examples of embedded controller systems.

Outline Syllabus

Band model of materials, metals, insulators and semiconductors. Intrinsic and doped semiconductors, p-n junction diode, BJT and MOSFET device structures and internal operation, modelling for analogue and digital applications, Electrons as waves, LEDs, lasers and solar cells. Noise. Digital circuit organisation. Microcontrollers and embedded systems, practical system organisation and interfacing. Software - hardware trade-offs, power consumption. Introduction to packaging and reliability.

Time Allocation

48 hours of lectures (inc case studies), 24 hours problem classes, 125 hours of guided independent study.

Recommended Previous Courses

Knowledge equivalent to first year EEE117, EEE118 and EEE119.

Assessment

Three hour examination answer. Weighting and sections to be confirmed by the module leader.

Recommended Books

Edwards-Shea, L.	The Essence of Solid-State Electronics	Prentice-Hall
Streetman & Bannerjee	Solid State Electronic Devices	Prentice-Hall
J. Crowe & B. Hayes-Gill	Introduction to Digital Electronics	Prentice Hall
T. L. Floyd	Digital Fundamentals	Prentice Hall
D. D. Gajski	Principles of Digital Design	Prentice Hall
M Morris Mano	Digital Design 3rd ed.	Prentice Hall
Sedra A S & Smith K C	Microelectronic Circuits	Oxford
Horowitz and Hill	The Art of Electronics	Cambridge
Smith, R.J.	Circuits Devices and Systems	Wiley

Objectives

"By the end of the unit, a candidate will be able to"

1 Use basic device relationships to predict the performance of some common semiconductor devices in the analogue, digital and optical arenas.

2 Explain the key issues in device packaging and appreciate the effects of electrical and thermal stress on device reliability.

3 Write down equivalent circuit representations of diodes, BJTs and MOSFETs and use these to predict device behaviour in a circuit context.

4 Recognise the circuit diagrams of and make simple quantitative performance predictions for a number of multi-transistor circuit blocks in both the analogue and digital domains.

5 Design linear and non-linear op-amp circuits for conditions well inside the amplifiers performance envelope.

6 Understand the nature of electronic noise and make quantitative predictions of noise magnitudes and of system noise parameters such as S/N and noise factor.

7 Discuss the merits and disadvantages associated with a number of logic families and be able to design using open collector (drain) logic devices and comparators.

8 Design at high level a simple embedded system and demonstrate awareness of key issues such as speed, power consumption, environment and hardware/software trade-off.

Detailed Syllabus

Lecture	Topic
1 - 2	Band model of electrical materials. Metals, insulators, semiconductors.
2 - 3	Intrinsic and doped semiconductors, transport properties, Ohmic and Schottky contacts
4 - 5	Junction diodes, BJT operating principles and terminal characteristics, relationship between device design and equivalent circuit parameters.
6 - 7	JFETs/MOSFETs, simple models and terminal relationships, relationship between device design and equivalent circuit parameters.
8	Wave nature of electron, de Broglie relation, energy quantisation
9 - 10	Optical devices, absorption, emission, quantum LEDS and lasers. Photodiodes, solar cells. Materials choices.
11 - 13	Electronic device performance limitations (frequency, current and voltage handling,

	temperature). Thermal aspects/relationship with reliability. Power consumption and motivation for management. Device packaging and parasitics.
14 - 15	Basic analogue building blocks: current mirrors, differential amplifier: opamp organisation.
16 - 17	Op-Amp properties and linear circuit applications, bandwidth, gain-bandwidth product and slew rate.
18 - 19	Non-linear op-amp applications, limiters, shaping circuits, precision rectifiers, comparators, schmitt triggers, relaxation oscillators
20 - 22	Introduction to noise in analogue circuits and systems: available noise power, signal to noise ratio, noise factor, noise factor of a cascade, noise temperature.
23 - 24	Basic digital building blocks: CMOS logic circuits and their design.
25 - 27	Input/output properties of digital circuits, open collector (drain), DAC and ADC topologies, signal conditioning
28 - 29	Introduction to noise in digital circuits: sources, effects, noise margins and relationship with logic families
38 - 39	Case study 2: Analogue system
30 - 31	I/O considerations: grounding, protection
32 - 33	Review of Finite State Machines and relationship to programmable systems
34	Programmable logic and FPGAs
35	Microcontrollers: anatomy of a simple system
36 - 37	Organisation and ISA
38	Memory organisation
39 - 40	Software/hardware trade-off, processing speed
41 - 42	Embedded systems, (examples washing machines, car engine management, etc)
43 - 44	External speakers/case studies

UK-SPEC/IET Learning Outcomes

Outcome Code	Supporting Statement
SM1p (was US1)	The behaviour of electrons in solids and the ways in which that behaviour can be manipulated in order to achieve useful engineering devices which themselves must be modelled to enable predictions of performance is a key aspect of Engineering Science covered in this module. The outcome is tested by exam.
SM2p (was US2)	The models that describe the behaviour of electrons in solids and the modelling of analogue circuits provide a variety of opportunities to apply mathematics to achieve solutions to engineering problems. The outcome is tested by examination
SM4m (was US2m)	Some awareness of trends, particularly in the rapidly developing area of opto-electronic devices is included to put the topic in context and to transmit some of the excitement derived from working in this dynamic area. The outcome is tested by exam.
SM3p (was US3)	This module demands knowledge and understanding of internal device physics and circuit modelling for both analogue and digital systems and components. Basic thermal and optical properties of solids and some software system ideas are integral to the module. The outcome is tested by exam.
SM6m (was US4m) Modified	The introduction to quantum well based optical devices leans heavily towards physics and contributes to this outcome. The outcome is tested by exam.
EA1p (was EA1)	Device models at the electron level, at the terminal characteristic level and at the behavioural level together with their application to estimating device, circuit or

	system performance for both digital and analogue environments contributes to this outcome. The outcome is tested by exam.
EA2p (was EA2)	Analytical device models and how to use them intelligently in a engineering context is a thread that runs throughout this module. The outcome is tested by exam.
EA3p (was EA3) Modified	Problem sheets, exam questions and worked examples are based on engineering practice and scenarios where possible.
EA4p (was EA4) Modified	Op-amp circuit analysis and the microcontroller/embedded systems parts of the module contribute to systems engineering ideas. The outcome is tested by exam.
EP2p (was P1)	Knowledge of semiconductor materials contributes to this outcome. The outcome is tested by exam
EP4p (was P4)	Device data sheets are used extensively throughout the module to demonstrate how to obtain the key information needed by the models used to predict device, circuit or system performance. The outcome is tested by exam
D3p	Some problems are posed using real world scenarios in which data is incomplete or intermediary data must be derived from specifications or other parameters. Students are provided with an intellectual toolbox to assess their analogue and digital circuits and electronic device design's ability to meet their design parameters using derived information or testable assumptions where necessary. This outcome is tested by exam.

Problem Sheets

Written and (some) Video Solutions On-Line

EEE225 Transistor Amplifier Circuit Analysis Problem Sheet

This problem sheet builds on the analysis of the two transistor amplifier circuits EEE118. It should prepare students well to tackle general problems involving transistors in analogue circuits. The circuits used in questions 1, 2 & 3 are not directly examinable, nor are questions 8 – 10. The techniques needed to solve the first few questions are the standard techniques of circuit analysis with active devices. These techniques were first introduced in EEE118 and are further developed in EEE225. If you can solve questions 1 – 3 confidently you'll have no problem at all with questions 4 – 7 which *are* examinable. Question 7 is quite similar to the sort of questions that come up in EEE223, and some parts of it to do with crossover distortion are in EEE225 as well.

How to tackle this sheet

Do question 1 or question 2 or question 3. Do *all* of questions 4, 5 & 6. Some of question 7 is needed in EEE225 especially related to crossover distortion, the rest is needed in EEE223.

If you feel that you've not had enough practice, go back and do the other questions as well. It would certainly be a good idea to look at the past exam papers as well for practice questions. You should find the exam questions much easier than the problems in this sheet, consiquently if you can do the sheet the exam should not pose any difficulty.

Questions 8 – 10 are for students who love the topic and want to go on an adventure of their own. The solution of these questions uses many of the techniques in this course but also moves outside the scope of the course. Unless you have lots of time available having done all the other quesetions and being up to date with all your other modules I would not devote time to these questions.

If you're looking for even more analogue try Gray, Hurst, Lewis and Meyer, which is considered by many to be the standard text on the subject. Behzad Ravazi has also written some very well liked books on the topic. He also has video lectures on YouTube which covers much of EEE118 and the semiconductors and analogue aspects of EEE225 https://www.youtube.com/watch?v=yQDfVJzEymI&list=PL7qUW0KPfsIIOPOKL84wK_Qj9N7gvJX6v

Question 1: A Common Emitter Circuit

This question is about the "type 1" common emitter circuit from EEE118. Unless otherwise stated, assume that all capacitors are short circuit in the mid-band. Some solutions will be easier to reach if R_L and R_C are lumped together as R'_L. Similarly R_B may be used to represent the parallel combination of R_1 and R_2.

The objective with the small signal derivations is to show which components are in control of certain circuit parameters, therefore the final form of the answer should be manipulated to reveal this information as clearly as possible. Arranging equations in a way that reveals certain underlying relationships in the circuit parameters is something computers are not very good at, this sort of work is best done by hand.

1. Find the DC conditions of the common emitter circuit in Figure 1 assuming the base current of Q_1 can be ignored.

2. Find the DC conditions again but taking into consideration the base current. Perform your calculations for the full range of h_{FE}. Find the range of h_{FE} from the Fairchild Semiconductor BC549 datasheet.

3. Explain (briefly, using bullet points for example) the job of each component in the circuit.

4. Explain (in words) why the emitter resistor, R_{E} acts to reduce the gain of the circuit unless it is decoupled by C_{E}.

5. Draw and label the small signal equivalent circuit for Figure 1.

6. Calculate the small signal transconductance, g_{m}, and base emitter resistance, r_{be} for the range of h_{FE} given in the Fairchild Semiconductor datasheet. You may assume that the transistor stage will be operated at frequencies considerably below the transition frequency, f_T, and therefore $\beta = h_{\mathrm{FE}}$

7. Show that the mid-band voltage gain of the common emitter circuit shown in Figure 1 is given by (1).

8. Show that the mid-band output resistance of the amplifier circuit in Figure 1 is given by (2).

9. Show that the mid-band input resistance of the amplifier circuit in Figure 1 is given by (3).

10. Show that the mid-band current gain given by (4).

11. Find an expression for the transresistance v_o/i_i of the amplifier stage shown in Figure 1.

12. Draw and label the small signal equivalent circuit for Figure 1 if C_{E} is *open* circuit at all frequencies of interest, all other capacitors may be considered short circuit.

13. Assuming C_{E} is *open* circuit at all frequencies of interest, derive the input resistance, output resistance, voltage gain and current gain of the amplifier. The final solutions take the forms shown in (5) - (8).

14. Given your solution for the small signal properties of the stage without emitter decoupling, determine what components are in control of the voltage gain, current gain, input resistance and output resistance. Comment on the effect of emitter degeneration on the small signal parameters. For example, which components are in control of the voltage gain? Which components dominate input resistance? What are the main components which reduce current gain?

15. State the numerical values of voltage gain, current gain, power gain, input resistance and output resistance with and without emitter decoupling over the range of h_{FE} given in the datasheet.

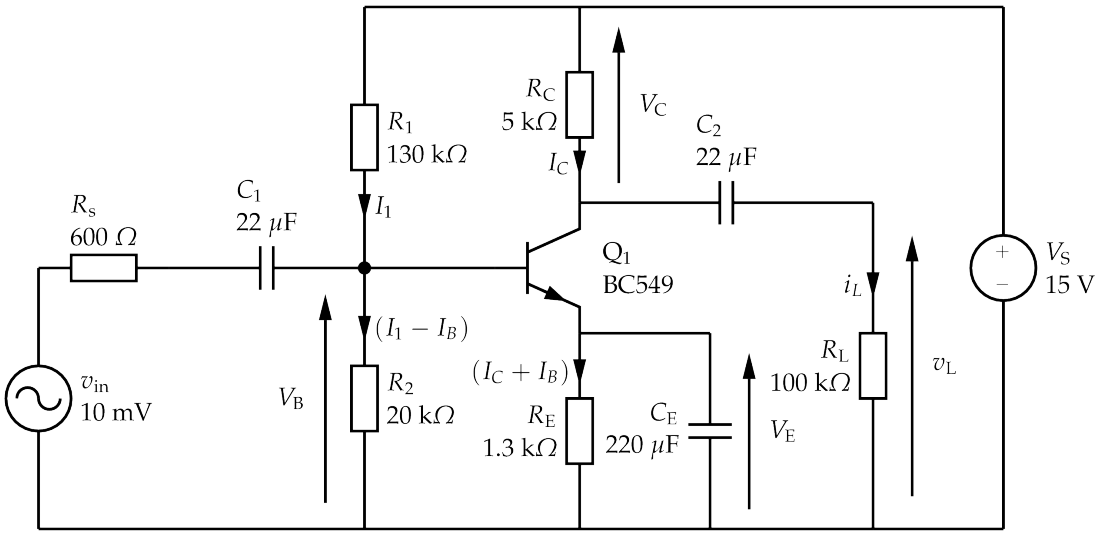


Figure 1: A common emitter amplifier circuit.

$$\frac{v_o}{v_i} = -\frac{g_m\, R'_L}{Rs\left(\frac{1}{R_B} + \frac{g_m}{\beta}\right) + 1} \tag{1}$$

$$r_o = \frac{v_o}{i_t} = R_C \tag{2}$$

$$r_i = \frac{v_i}{i_i} = \frac{1}{\frac{1}{R_B} + \frac{g_m}{\beta}} \tag{3}$$

$$\frac{i_o}{i_i} = \beta \frac{R_B}{R_B + r_{be}} \text{ or } \frac{\beta}{1 + \frac{\beta}{g_m R_B}} \tag{4}$$

$$\frac{v_o}{v_i} = -\frac{g_m R'_L}{R_S \left(\frac{1}{R_B} + \frac{g_m}{\beta} + \frac{1}{R_S} + \frac{(\beta+1)}{\beta} R_E g_m \left(\frac{1}{R_B} + \frac{1}{R_S} \right) \right)} \tag{5}$$

$$r_i = \frac{1 + \frac{\beta}{g_m R_E (\beta+1)}}{\frac{1}{R_B} + \frac{1}{R_E (\beta+1)} + \frac{\beta}{g_m R_E R_B (\beta+1)}} \tag{6}$$

$$r_o = R_C \tag{7}$$

$$\frac{i_o}{i_i} = -\frac{\beta}{\beta \left(\frac{1}{g_m R_B} + \frac{R_E}{R_B} \right) + \frac{R_E}{R_B} + 1} \tag{8}$$

Question 2: A Common Base Circuit

This question is about a capacitively coupled common base amplifier.

1. Find the DC conditions of the common base circuit in Figure 2 assuming the base current of Q_1 can be ignored.

2. Find the DC conditions again but taking into consideration the base current. Perform your calculations for the full range of h_{FE}. Find the range of h_{FE} from the On Semiconductor MJE340 datasheet.

3. Explain (briefly, using bullet points for example) the job of each component in the circuit.

4. Draw and label the small signal equivalent circuit for Figure 2.

5. Calculate the small signal transconductance, g_{m}, and base emitter resistance, r_{be} for the range of h_{FE} given in the Fairchild Semiconductor datasheet. You may assume that the transistor stage will be operated at low frequencies and therefore $\beta = h_{\text{FE}}$

6. Assuming the capacitors are short circuit at all frequencies of interest, show that the input resistance of the amplifier circuit in Figure 2 is given by (9).

7. Assuming the capacitors are short circuit at all frequencies of interest, show that the output resistance of the amplifier circuit in Figure 2 is R_C.

8. Assuming the capacitors are short circuit at all frequencies of interest, show that the transresistance (output voltage / input current) gain of the common base circuit shown in Figure 2 is given by (11).

9. Derive an expression for the current gain. Solution: (12).

10. Derive an expression for the voltage gain. Solution: (13).

11. Practical transistors have a physical resistance between the active part of the base region and the transistor package leg. This is partly made from the ohmic bond-wire resistance inside the package and partly made from the ohmic resistance of the semiconductor between the position at which the bond wire is attached to the semiconducor and the position of the active part of the base material. Draw the small signal equivalent circuit assuming that this base spreading resistance, r_b, appears in series with the base leg. C_1 is still short circuit at all frequencies of interest.

12. Re-derive your small signal results so far assuming taking into account the base spreading resistance. The results are shown in (14) - (17).

13. Reflect on and then qualitatively describe (i.e. in words) the effect of the base spreading resistance on the stage's small signal parameters. Comment on the similarity of the feedback provided by lifting the base node in the common base circuit with the effects of degenerating the emitter in the common emitter circuit.

14. State the numerical values of the small signal metrics of performance with and without the base spreading resistance over the range of β. You may assume that the amplifier is operated at a low frequency and therefore $\beta = h_{FE}$

$$\frac{v_e}{i_{in}} = \frac{1}{\frac{g_m}{\beta} + g_m + \frac{1}{R_E}} \tag{9}$$

$$\frac{v_o}{i_o} = R_C \tag{10}$$

$$\frac{v_o}{i_{in}} = \frac{g_m R'_L}{\frac{g_m}{\beta} + g_m + \frac{1}{R'_E}} \tag{11}$$

$$\frac{\frac{\beta}{r_{be}}}{\frac{1}{r_{be}} + \frac{\beta}{r_{be}} + \frac{1}{R'_E}} \approx \alpha \tag{12}$$

$$\frac{v_o}{v_i} = \frac{g_m R'_L}{\left(\frac{1}{r_{be}} + g_m + \frac{1}{R_s} + \frac{1}{R_E}\right)} \tag{13}$$

$$\frac{v_e}{i_{in}} \approx \frac{r_b}{\beta} + \frac{1}{g_m} \tag{14}$$

$$\frac{v_o}{i_{in}} = \frac{R'_L}{\frac{1+\beta}{\beta} + \frac{1}{g_m R'_E} + \frac{r_b}{R'_E \beta}} \tag{15}$$

$$\frac{i_o}{i_{in}} = \frac{1}{\frac{1+\beta}{\beta} + \frac{1}{g_m R'_E} + \frac{r_b}{R'_E \beta}} \tag{16}$$

$$\frac{v_o}{v_{in}} = \frac{g_m R'_L}{R_s \left(\frac{g_m}{\beta} + \frac{1}{R_s} + \frac{g_m r_b}{\beta R_s} + g_m + \frac{1}{R_E} + \frac{g_m r_b}{\beta R_E} \right)} \tag{17}$$

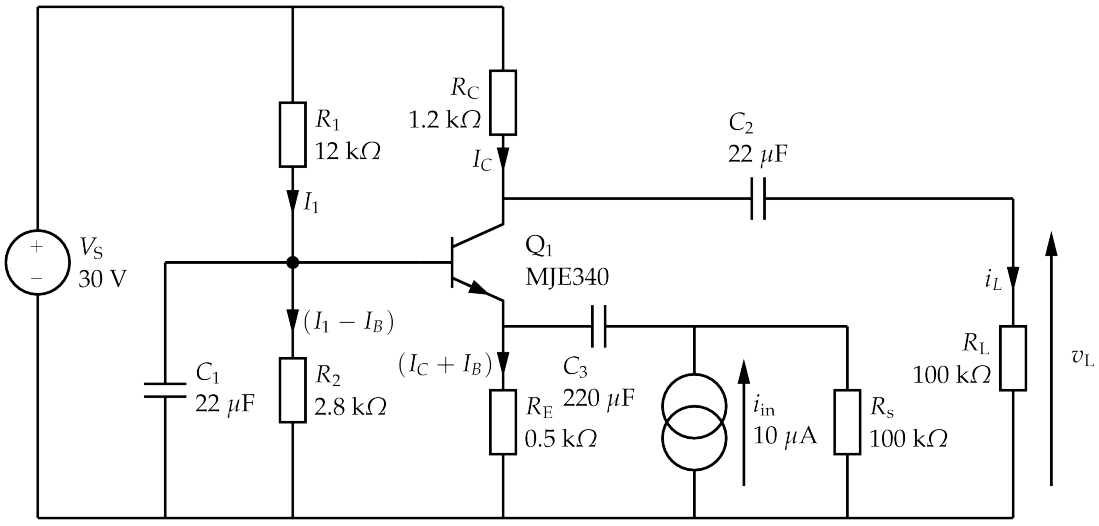


Figure 2: Common Base Amplifier Circuit

Question 3: An Emitter Follower Circuit

This question is about a capacitively coupled emitter (common collector) follower amplifier, shown in Figure 3. This emitter follower stage is used to drive a 16 Ω loudspeaker represented by R_E. The DC current biasing the stage also flows through R_E. This is often not practical but for the sake of making the question easier we will assume that this is a magical speaker (from my office...) that doesn't mind having a large DC component of current flowing through it. Of course the DC current dissipates power in the speaker but this would not be useful output power (sound) it would be heat. It would also hold the voice coil away from the center position but as we have said all these problems are ignored for the sake of simplicity.

1. Find the DC conditions of the emitter follower circuit in Figure 3 assuming the base current of Q_1 can be ignored. Choose V_B such that V_L, the emitter

voltage, is half way between the power supply and ground, thereby providing the largest possible output voltage swing.

2. Find the DC conditions again but taking into consideration the base current. Perform your calculations for the full range of h_{FE}. Find the range of h_{FE} from the On Semiconductor MJ15003 datasheet.

3. Explain (briefly, using bullet points for example) the purpose of each component in the circuit.

4. Sketch the output characteristic (V_{CE} *vs* I_C as a function of V_{BE} or I_B), add the operating point and the load line. On secondary axes, sketch the time dependent sinusoidal waveforms showing how the operating point moves according to the input signal, V_{in} and the output signal, V_L that results from this input.

5. Draw and label the small signal equivalent circuit for Figure 3.

6. Calculate the small signal transconductance, g_{m}, and base emitter resistance, r_{be} at the operating point for the range of h_{FE} given in the On Semiconductor datasheet. You may assume that the transistor stage will be operated at low frequencies and therefore $\beta = h_{\mathrm{FE}}$. Calculate the g_m and r_{be} at the maximum and minimum collector current based on the amplitude of the input waveform. Describe the effect will the variation of g_m and r_{be} have over the course of one cycle on the shape of the voltage and current waveforms in the circuit. To simplify your discussion you may assume β has no I_C dependence and that neither β nor g_m depend on temperature (or that the transistor will not get hot - same thing).

7. Based on the size of the input signal, the DC conditions you've calculated and your knowledge of electronic circuits, how valid is the small signal assumption in this case?

8. Assuming C_1 is short circuit at all frequencies of interest, show that the input resistance of the amplifier circuit in Figure 3 is given by (18). Comment on the size of R_s compared to the input resistance, what would you expect to find when evaluating the voltage gain of this stage.

9. Assuming C_1 is short circuit at all frequencies of interest, show that the output resistance of the amplifier circuit in Figure 3 is given by (19).

10. Assuming C_1 is short circuit at all frequencies of interest, show that the voltage gain of the circuit shown in Figure 3 is approximately unity.

11. Develop an expression for the current gain, determine its maximum value and the conditions required to reach that maximum.

12. Calculate the quiescent power dissipation in Q_1 and R_E.

13. Calculate the average power dissipated in the loudspeaker, R_L in one cycle if $R_s = 0.1\ \Omega$ and if $R_s = 600\ \Omega$. Qualitatively, do these figures relate to the earlier input resistance derivation?

14. Derive an expression for the instantaneous power dissipation in the transistor, Q_1. You may assume that the power dissipated in the transistor is the product of I_C and V_{CE} which will both vary *approximately* sinusoidally given a sinusoidal input. *Hint: this involves some integration of sines and cosines.*

15. Using your derivation find the input signal amplitude which results in the highest power dissipation in the *transistor*.

16. Show that the highest possible efficiency of this circuit is 25%. You may neglect losses in R_1 and R_2.

17. What is the conduction angle of Q_1? What class of operation is this stage operating in?

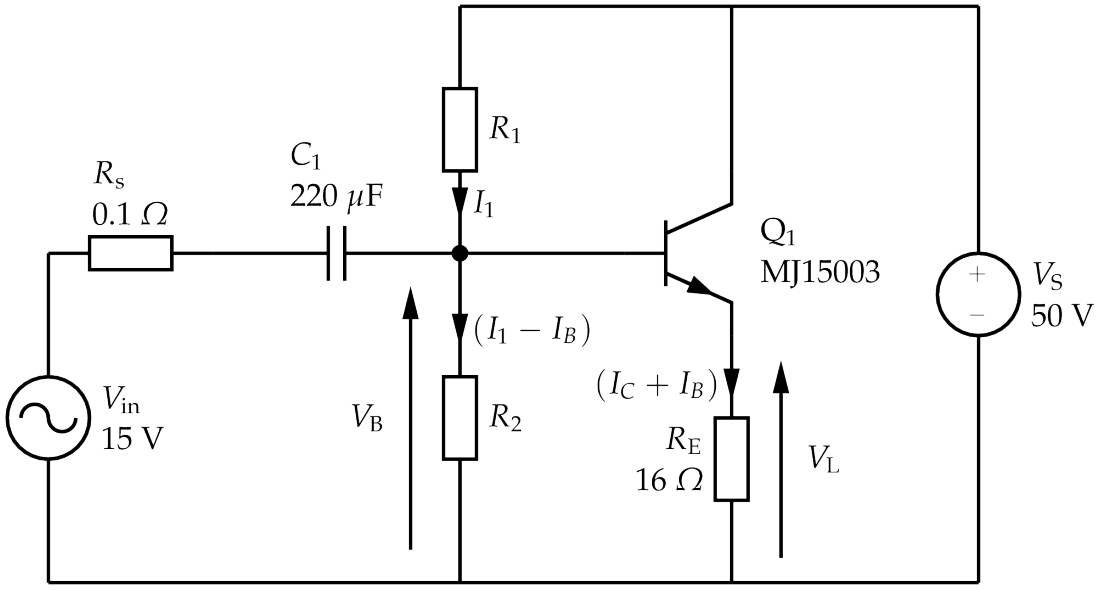


Figure 3: Emitter Follower Amplifier Circuit

$$r_{in} \approx R_B \tag{18}$$

where $R_B = R_1||R_2$.

$$r_o \approx \frac{1}{g_m} + \frac{R_B}{\beta} \tag{19}$$

Question 4: A Darlington Pair

One of the many problems with the circuit in question 3 is the very low input impedance. To ameliorate this a Darlington pair is often used in operational and discrete power amplifier output stages.

1. Re-draw Figure. 3 to make use of a Darlington pair. The upper transistor will be MJE340.
2. Design suitable component values to utilize the available rail voltage appropriately, include base current and the full range of h_{FE} in your calculations.
3. Explain briefly why the Darlington is an improvement.
4. Draw and label the small signal equivalent circuit for your circuit, you may assume that $R_B = R_1||R_2$ is very large compared to R_S and can be ignored.
5. Assuming C_1 is short circuit at all frequencies of interest, develop the input resistance of the Darlington emitter follower amplifier. You may assume that $R_B = R_1||R_2 >> R_S$ and therefore can be ignored. Attempt to find a form of your equation that can show the effect of N transistors cascaded. Comment on the effects of R_S on the stage voltage gain compared to the effects of R_S on the circuit in question 3.
6. Assuming C_1 are short circuit at all frequencies of interest, develop an expression for the output resistance of the amplifier. Similarly to the input resistance, try to arrive at a form of solution which shows the effect of N transistors in cascade.
7. Assuming the biasing network, $(R_B = R_1||R_2)$ can be ignored, derive an expression for the current gain.

Question 5: Widlar Current Mirror

The circuit in Figure 4 is a Widlar current mirror. The transistors are 2N5551. You may assume that the transistors are idential.

1. Show that the current in R_L is related to the current I_S by (20).
2. If I_S is 2000 μA what is the largest value R_L that can be used without pushing Q_1 into saturation? *Hint: you will need to use the datasheet to find* $V_{\text{CE(sat)}}$.

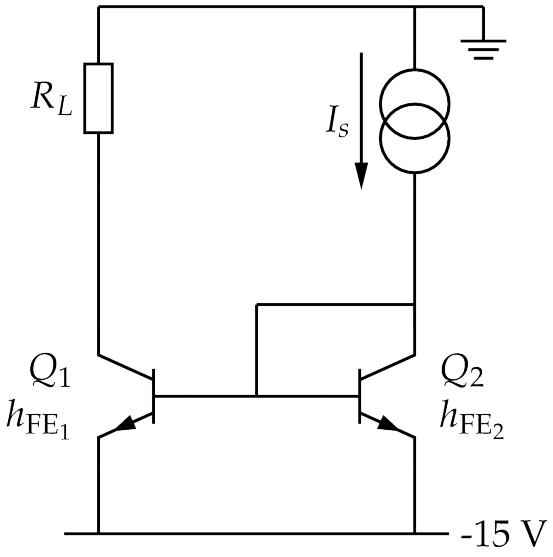


Figure 4: A Widlar current mirror circuit.

3. Draw the small signal equivalent circuit for the mirror, ensure you include r_{ce}.

4. Derive the output resistance of the mirror.

5. Derive the output resistance when emitter degeneration resistors are included.

6. By adding another transistor as in Figure. 5 a significant improvement can be made. What advantage does this circuit have over the two transistor mirror?

7. Derive the relationship between I_S and the load current in Figure 5.

$$\frac{I_S}{I_{R_L}} = \frac{h_{FE}+2}{h_{FE}} \tag{20}$$

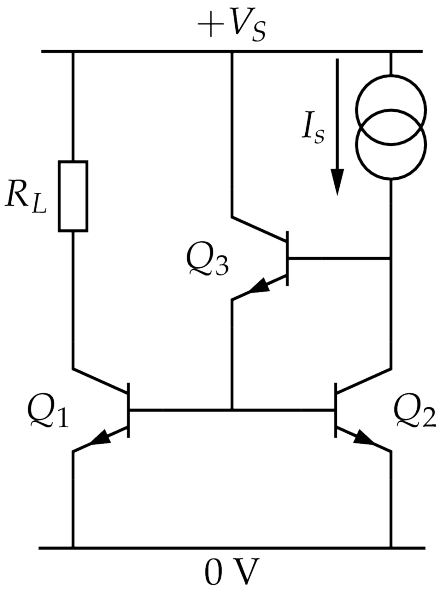


Figure 5: A current mirror circuit with helper transistor.

Question 6: Lin Style Operational Amplifier

There is a video solution to this question on the teaching resources website. The circuit of Figure 6 shows a simple form of op-amp circuit. Assuming that each transistor has a static current gain, I_C/I_B, and small signal current gain, $\Delta I_C/\Delta I_B$, of 100, that $kT/e = 0.026$ V and that each transistor has a V_{BE} of 0.7 V when conducting.

1. Estimate I_E, I_1, I_2 and I_3 assuming that $v_i = 0$ V, $v^+ = 0$ V, $v^- = 0$ V and $V_A = 0$ V.

2. Estimate the gain, v_{o1}/v_i, of the differential amplifier assuming that r_{ce} of Q_1 is very large compared to R_1. Remember to include the effects of Q_3 (ie, its input resistance) in your calculation.

3. Estimate the gain, v_a/v_{o1}, of the voltage gain stage assuming that r_{ce} of Q_3 and the input resistances of Q_4 and Q_5 are very large compared to R_{VA}.

4. Use your results from parts 2 and 3 to estimate the overall gain v_{o4}/v_i. What have you assumed in this calculation?

5. Using your powers of reasoning, identify which stage gain would be significantly improved if the small signal current gain of each transistor increased to 500.

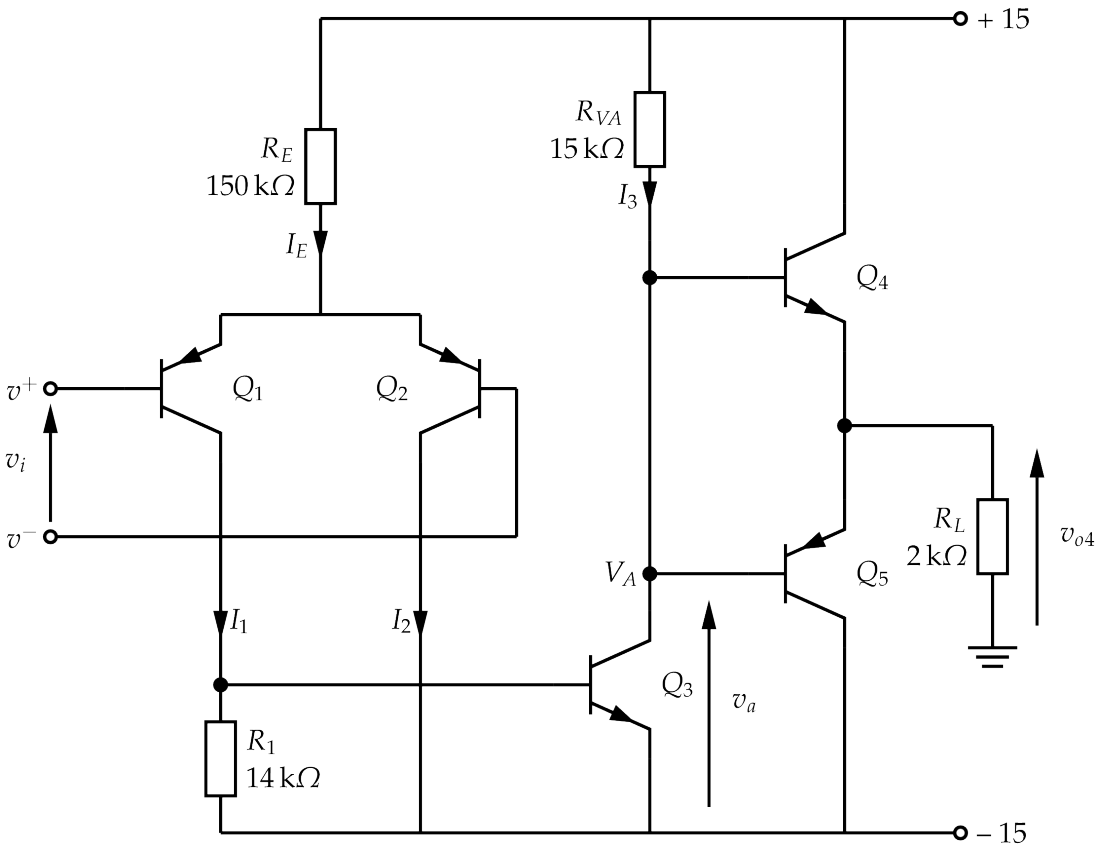


Figure 6: Simplified operational amplifier circuit.

Question 7: Push Pull Emitter Follower

1. Concisely describe the cause of crossover distortion in class B push-pull amplifiers.

2. Use a sketch to show the effects of crossover distortion on a triangle or sinusoidal waveform, taking particular care with your representation of the crossover region.

3. Sketch a circuit diagram of a voltage amplifier and push pull stage which largely overcomes the problems of crossover distortion and describe the operation of your circuit.

4. Calculate the quiescent power dissipation in one of the output transistors in your circuit.

5. Calculate the average power dissipated in the load resistor of your circuit.

6. Derive expressions for the instantaneous power dissipation in one of the output transistors. You may assume that the power dissipated in a transistor is the product of I_C and V_{CE} which will both vary *approximately* sinusoidally given a sinusoidal input. *Hint: this involves some integration of sines and cosines.*

7. Using your derivation find the signal voltage amplitude across the output which results in the highest power dissipation in the *transistor*.

8. Show that the highest possible efficiency of this circuit is approximately 70%.

9. The push-pull stage may operate in class C, B or A depending on the quiescent current flowing in the output transistors, which in turn is related to the voltage between the bases of the two output transistors. Sketch the load voltage and collector current waveforms of the two output transistors for each class, noting the salient features.

10. For each class of operation above, what angle of current conduction exists in each class and what *approximate* range of voltages must exist between the bases of the output transistors?

Question 8: Common Base Transimpedance Amplifier with DC servo

Download the journal paper at http://dx.doi.org/10.1088/0957-0233/23/12/125901. You may need VPN, see http://www.shef.ac.uk/cics/vpn for details. Describe how the transimpedance amplifier in Figure 6 of this paper works. Develop the DC conditions and the small signal parameters of the common base stage driven by the photodiode.

Question 9: A Charge Amplifier for X-Ray Detection

This question relates to a charge amplifier - its output votlage is porportional to the integral of the input current. This sort of circuit is often used to interface certain kinds of semiconductor detectors with signal processing hardware (such as multi-channel analysers). The circuit has a very high input impedace and low output impedance.

1. Describe in words how the circuit acts to stabilise its DC conditions. In so doing identify the circuit building blocks and describe the low frequency feedback (ignore C_3).

2. Calculate the DC conditions (currents through and voltages across all components (except C_3). Assume that for the JFET $I_D = 10$ mA at $V_{GS} = 0$ V. Assume the small signal current gain of all the BJTs is 100.

3. Postulate the purpouse of C_2. What is it likely to form a time constant with?

4. What is C_3's job in this circuit? It may help to think about the input as being short duration pulses of current sepperated by long periods of nothing. This would represent an x-ray generating a number of electron hole pairs as it passes through the detector, these become the pulse. The input impedance is very large so pushing current onto the gate will have to charge up or discharge some capacitors (including those internal to Q_1) the change in gate voltage will act to turn Q_1 on or off somewhat. This signal will propogate through the amplifier until it reaches the output (which is also the right hand side of C_3). Another way to look at it is to ask what will happen if I keep putting charge onto the gate and it doesn't leave. The amplifier will saturate, so how can I avoid this?

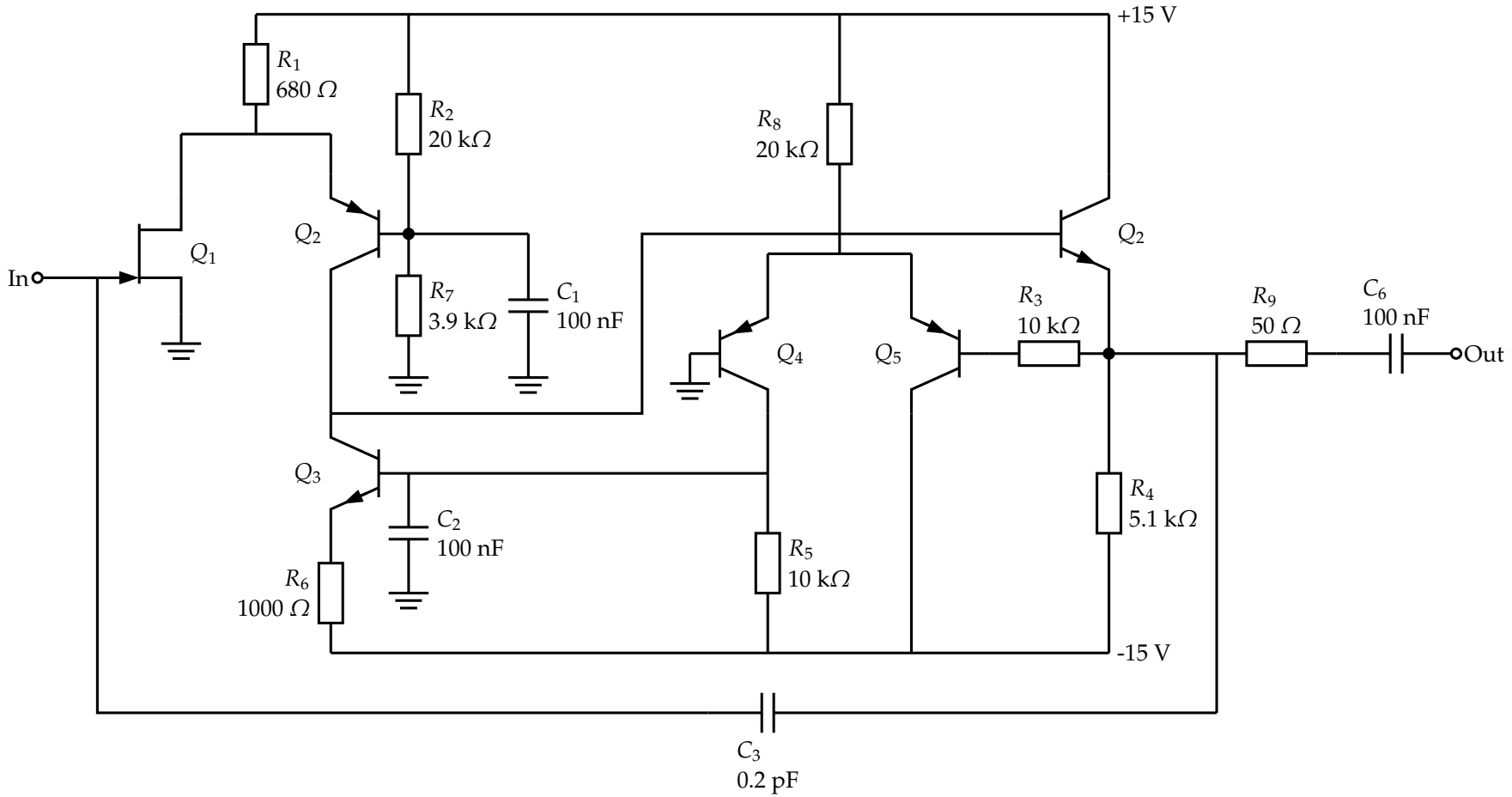


Figure 7: Akeel's charge amplifier.

Question 10: Three Transistor Amplifier with Singleton Input Stage

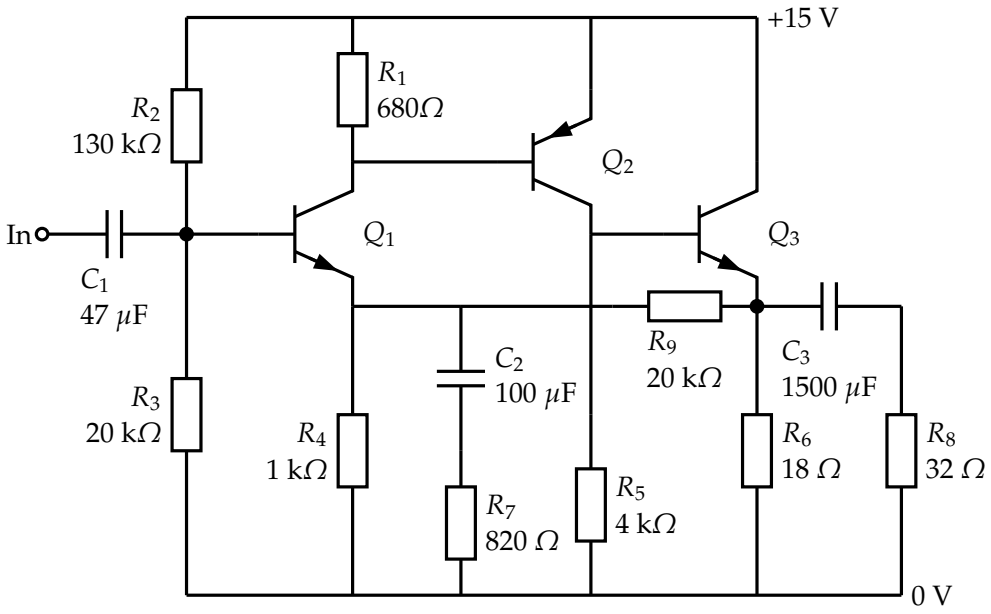


Figure 8: Simple opamp with "singleton" input and current feedback.

1. For the circuit in Figure 8, determine the DC conditions. For a purely analytical approach you will need to write out a system of equations and solve simultaneously. However since you are fleet of mind it is clear to you that this is basically a headphone amplifier therefore it will probably have equal voltage swing above and below the average value on its output. Hence you know that the Emitter of Q3 is likely to be at about 7.5 V. It is now soluble with no equations except Ohm's law.

2. approximate the input resistance (do not derive it, use your engineering brain to make a single calculation that leads you to a value with +/-10% accuracy).

3. What is the gain at DC (It is AC coupled but that does not mean there is no gain at DC).

4. What is the gain in the midband (AC gain, all capacitors short circuit).

5. list the major problems with the circuit and explain how they arrise. Why are real amplifiers not made like this? Think about input and output impedance, gain, distortion etc.

6. If you could only change one thing to improve the performance of the circuit what would it be?

7. how hot is Q3 likely to get if it is a 2N3055 in a TO3 metal package without a heatsink, is that acceptable? Why?

8. I described it as series–shunt feedback what does that actually mean? What impact does the 'mode' of feedback have on the circuit performance? (You will need to do some serious background reading in Grey Hurst Lewis and Meyer - it's to do with input and output impedance).

9. Since you've got Grey open...probably around page 583 if you're in the 5th edition. Teach yourself how to use signal flow graphs to analyse circuits with feedback. Apply the technique to the circuit in this question.

10. Replace the input transistor with a JFET, 2N3819. Re-design the circuit to perform the same function. The input stage biasing resistors can be removed and the gate of the JFET can float at 0 V.

11. Use LTSPICE to compare the input impedance of the two circuits.

12. Use the LoopGain2.asc example file in the "Educational" directory of LTSPICE to assess the open loop gain of this amplifier. Add compensation between collector and base of Q_2 observe the effects of changing the dominant pole frequency on the open loop gain for several values of capacitor (try 100 pF to start). Inspect the *open loop* gain and phase margins, compensate it to ensure stability.

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Analogue and Digital Electronics Problem Sheet

Operational Amplifiers

Q1 The circuit of figure 1a is a non-inverting amplifier based on an operational amplifier (op-amp). The op-amp has a gain-bandwidth product of 10 MHz. If $R_1 = 2$ kΩ and $R_2 = 10$ kΩ, find

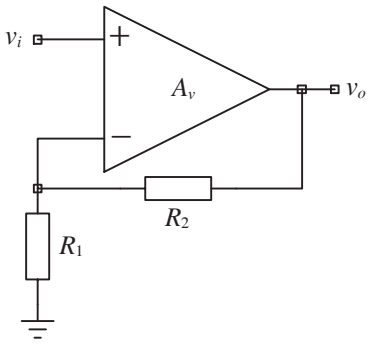


Figure 1a

(i) the gain, v_o/v_i, of the circuit. (6 V/V)

(ii) the -3 dBbandwidth you woud expect the circuit to have. (1.67 MHz)

(iii) the risetime of the output in response to an ideal step input. (*assume here that the step is small, ie., the output is not saturated by the step.*) (0.21 μs)

The circuit of figure 1a is modified by replacing resistor R_1 by the circuit of figure 1b in which $R_3 = 220$ Ω, $R_4 = 2$ kΩ and $C = 10$nF.

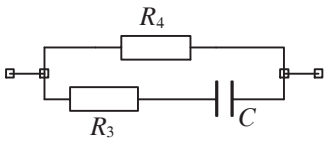


Figure 1b

(iv) Write down the high and low frequency gains of the modified circuit. (l.f. 6 V/V; h.f. 51.5 V/V)

(v) Show that the transfer function, v_o/v_i, of the modified circuit is given by

$$\frac{v_o}{v_i} = k\,\frac{\left(1+j\frac{f}{f_0}\right)}{\left(1+j\frac{f}{f_1}\right)} \text{ where } k = \frac{R_2+R_4}{R_4},\ f_0 = \frac{R_2+R_4}{2\pi C(R_2R_4+R_2R_3+R_3R_4)} \text{ and } f_1 = \frac{1}{2\pi CR_3}$$

(vi) Sketch magnitude and phase response Bode plots for the amplifier using the values given for R_2, R_3, R_4 and C.

Q2 Derive an expression for the gain-bandwidth product of the circuit of figure 2. (*You should find that this inverting amplifier connection behaves slightly differently from the non-inverting case covered in the lecture notes.*)

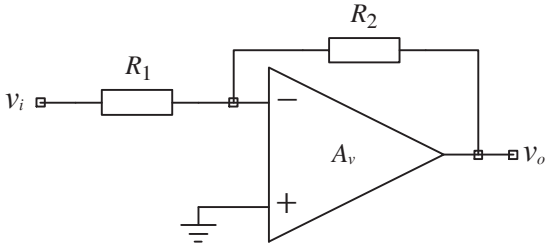


Figure 2

Q3 In medical impedance imaging systems small voltages on the surface of a body are sensed by buffer amplifiers with a very high input impedance. If an op-amp voltage follower circuit is to be used as a sense amplifier which must not introduce a phase error greater than -0.1^{o} at a frequency of 50 kHz, what gain-bandwidth product is required of the op-amp? (28.6MHz) (*remember that the buffer will be a first order system so you can write down its transfer function straight away.*)

Q4 A particular op-amp for which you have no data is observed to have a step response of the form $k\ (1-e^{-t/2.8\times10^{-6}})$ when wired to give a non-inverting gain of 250 V/V.

(i) What is the gain-bandwidth product of the op-amp? (14.2MHz)

(ii) What 3dB bandwidth would you expect for a non-inverting gain of 10V/V? (1.42MHz)

(iii) What circuit risetime would you expect for the non-inverting gain of 10V/V? (246ns)

Q5 A non-inverting amplifier circuit with a gain of 10 V/V uses an op-amp with a slew rate of 25 V/μs and a gain-bandwidth product of 15 MHz.

(i) Evaluate $|\text{gain}|$ and phase shift of the amplifier at a frequency of 5 MHz. (2.87, -73^{o})

(ii) What is the maximum frequency at which a 20 V pk-pk sinusoidal output can be supported in undistorted (ie purely sinusoidal) form? (398kHz)

(iii) At what amplifier circuit gain would the exponential shape of the rising and falling edges of a 15 V pk-pk "square wave" output begin to be affected by the amplifier's slew rate capabilities? Would the exponential shape of the edges be affected by a gain of half this value? (56, Yes)

(iv) Why is the answer to part **(iii)** independent of the fundamental frequency of the square wave? *(assume that you can observe enough of the exponential response to identify its aiming level.)*

Q6 For the circuit of figure 6, show that

$$v_o = \frac{2}{CR}\int v_i\,dt$$

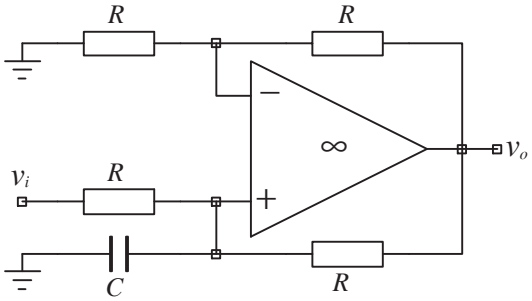


Figure 6

Q7 Demonstrate that the finite gain defect of the op-amp in figure 7a can be represented by the equivalent circuit of figure 7b where the op-amp is ideal. (*This process expresses the effects of finite A_v in terms of normal circuit elements and thus makes them easier to interpret.*) ***Hint:*** *approach the problem by showing that both circuits have the same transfer function.*

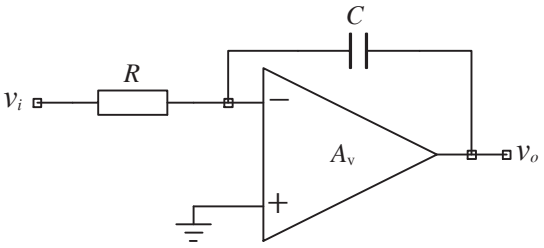


Figure 7a

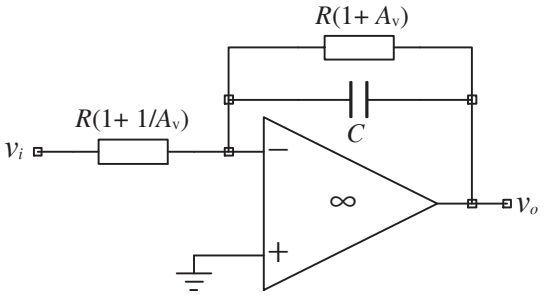


Figure 7b

Q8 Choose values of R_2, R_3, and C in figure 8 to give pole and zero frequencies of 10 Hz and 500 Hz respectively and a high frequency gain of 10 V/V. Sketch the amplitude and phase response of the system. (4.99MΩ, 91.6kΩ, 3.13nF)

If an *RC* low pass circuit with a time constant of 79 μs is attached to the op-amp output, sketch the overall frequency response of the circuit. (*The overall response is a close approximation to the equalisation characteristic necessary to get a flat response from a magnetic record player cartridge.*)

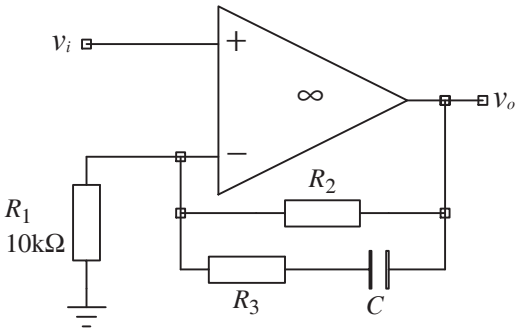


Figure 8

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Analogue and Digital Electronics Problem Sheet

Noise

In all questions the noise generated by a noisy resistor is $4kTR$ V^2 Hz^{-1} where $k = 1.38 \times 10^{-23}$ JK^{-1} and $T = 300$ K.

Q1 If the two resistors in the circuit of figure 1 are noise free,

(i) Find the rms noise voltage, v_{on}, in V $Hz^{-1/2}$. (19.4nV$Hz^{-1/2}$)

(ii) What is the total rms noise voltage, v_{on}, over a 20 kHz bandwidth ? (2.74μV)

(iii) If the circuit is represented by a Thevenin equivalent consisting of v_{on} and a resistance R_{Th}, find R_{Th}. (7.76 kΩ)

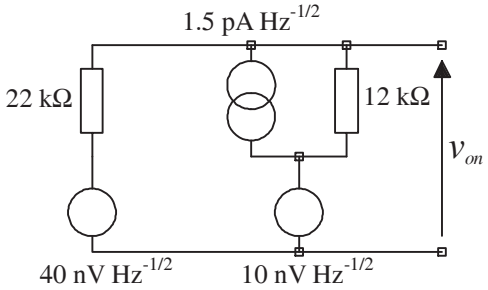


Figure 1

(iv) What is the noise temperature of the Thevenin equivalent resistance if it is assumed that this resistance is responsible for all the noise of part **(i)**? (880K)

Q2 In the circuit of figure 2, R_S is a noisy resistance of 10 kΩ, v_n is a noise source of 15 nV $Hz^{-1/2}$ and i_n is a noise source with a mean squared value of 2.25×10^{-24} A^2 Hz^{-1}. Find the rms output noise, v_{on}. (24.8 nV $Hz^{-1/2}$)

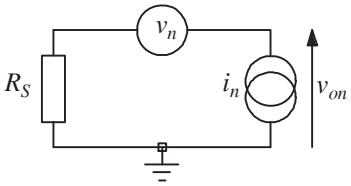


Figure 2

Q3 In the circuit of figure 3, only the 20 V source is noise free.

(i) What is the noise voltage across the diode in terms of V $Hz^{-1/2}$? (868pV$Hz^{-1/2}$)

(ii) What is the Thevenin equivalent resistance from which that noise comes ? (91Ω)

(iii) What is the effective noise temperature of the resistance calculated in part **(ii)**? (150K)

(iv) If the output is loaded by a 10 pF capacitor, what is the total rms noise voltage at the output? (14.4μV)

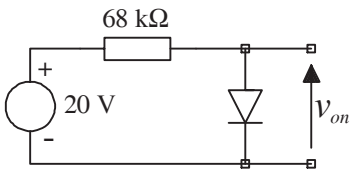


Figure 3

The noise generated by a diode is $2eI$ A^2 Hz^{-1} where $e = 1.6 \times 10^{-19}$ C. (***Hint:*** *Remember that the diode has a slope or incremental resistance* $r_d = kT/eI$ *where I is the dc bias current through the diode. This resistance will affect the noise but will not itself contribute to it*)

Q4 In the circuit of figure 4, $i_n = 6$ pA Hz$^{-1/2}$. Find the total rms noise voltage across C. (*This question involves quite a lot of careful circuit analysis so leave this it until you have done all the others.*) ()

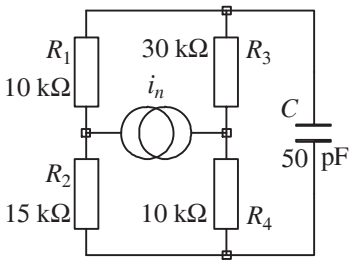


Figure 4

Q5 A particular amplifier has a noise free input resistance of 50kΩ and equivalent input noise voltage and current generators of 12 nV Hz$^{-1/2}$ and 0.6 pA Hz$^{-1/2}$ respectively. The amplifier gain is 100 V/V. The amplifier is fed from a signal source with a noisy Thevenin equivalent internal resistance of 20 kΩ.

(i) What is the output noise voltage in terms of V Hz$^{-1/2}$? (1.43μVHz$^{-1/2}$)

(ii) What is the signal to noise ratio at the amplifier output if the input signal level is 50 μV rms and the amplifier noise bandwidth is 10 kHz? (402 or 26 dB)

(iii) What is the noise factor of the amplifier? (1.87)

Q6 Your boss asks you to characterise the noise performance of a new amplifier with infinite input resistance and a gain of 50 V/V by using two equivalent input noise generators, v_n and i_n. When you connect a true rms voltmeter with a noise bandwidth of 5 kHz to the amplifier output you find that when the input is short circuited to ground the meter reads 30 μV and when the input is connected to ground via a 3 kΩ resistor, the meter reads 50 μV.

(i) Draw the noise equivalent circuit of the whole measurement system.

(ii) Calculate the values of v_n and i_n? (8.49 nV Hz$^{-1/2}$, 2.95 pA Hz$^{-1/2}$)

Q7 A wideband amplifier in a matched 50 Ω system is made from two thin film amplifier modules with gains of 25 dB and 15 dB and noise figures of 4.50 dB and 7.00 dB respectively such that the overall amplifier bandwidth, Δf, is 1000 MHz.

(i) What is the gain of the series combination? (40dB)

(ii) What is the noise factor of each amplifier module? (2.82 and 5.01)

(iii) What is the noise figure of the combination if the higher gain module is at the input end of the amplifier? (4.53dB)

(iv) What is the total added noise power delivered to the load? (76.2nW)

(v) What is the signal to noise ratio at the amplifier output if the input signal power is 10 pW? (-0.7dB)

(vi) What is the effective noise temperature of the 50 Ω source resistance? (851K)

The maximum available noise power is $kT\Delta f$ W where Δf is as defined in the question. This question uses the notation (noise figure) = 10 log (noise factor).

Handouts

(The Course Notes)



Transistor Characteristics

Introduction

Transistors are the most recent additions to a family of electronic current flow control devices. They differ from diodes in that the level of current that can flow through them is controlled by a control input (which unfortunately has different names in different devices) and in this sense they act like the control valves one might find in an hydraulic or pneumatic system. Indeed, the very first active devices consisted of systems of electrodes in an evacuated glass envelope and these were given the name "valves".

The detailed operation of these devices is not of interest in this module. Unlike water or gas which are fluids made of charge-neutral molecules, the moving particles (called electrons) that constitute an electric current carry an electric charge. In transistors and valves, control of flow is achieved by manipulating the electric field environment through which the electrons must travel in order to make it easier or harder for flow to occur. The devices are generally three terminal devices with one terminal common to the current flow path and the control input.

From an application point of view, transistors (and valves) are described by performance characteristics and there are two of these that are important in understanding device operation: The ***transconductance characteristic*** (the relationship between input control voltage and output (controlled) current) and the ***output characteristic*** (the relationship between output (controlled) current and the voltage across the current flow path terminals). After looking at transconductance and output characteristics in general terms, each of the three main transistor families will be introduced.

Transconductance characteristics

The transconductance characteristic of a transistor (or vacuum tube) is the relationship between the input (control) voltage to and the output (controlled) current through the device. It is a measure of the effectiveness of the control mechanisms within the device; a high value of transconductance means that small changes in the input (control) variable give rise to large changes in the output (controlled) variable.

Typical transconductance characteristics of a "bipolar junction transistor" (BJT), a "junction field effect transistor" (JFET) and an "enhancement mode MOSFET" are shown in figure 1a and relate to the circuits of figure 1b in which both the circuit symbol of each device and the variables used in figure 1a are given. I_C (I_D) is the controlled current and V_{BE} (V_{GS}) is the control voltage for the BJT (FET of either type). There are a few points to notice about the curves of figure 1a and the symbols of figure 1b.

(i) The transconductance curves are all basically the same shape - ie they all have some threshold after which the controlled current increases with increasing control voltage.

(ii) The BJT has a much steeper slope than the FETs - ie the control process is most effective with a BJT and least effective with a JFET.

(iii) The emitter (source) is the BJT (FET) terminal that is common to controlled current and control voltage.

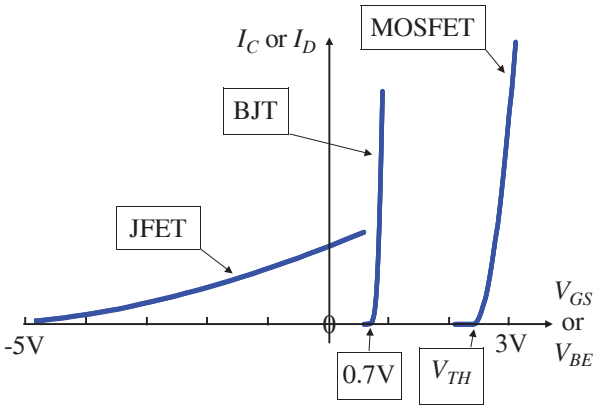


Figure 1a

Transconductance curves for a JFET, a BJT and a MOSFET.

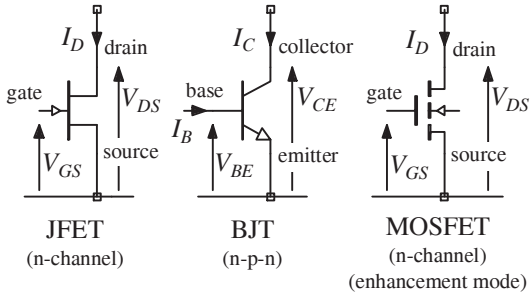


Figure 1b

The circuit symbols, terminal names and variable definitions for a JFET, a BJT and a MOSFET

(iv) The MOSFET has an extra terminal called the "substrate". In the majority of cases this is connected either to the source or to the most negative part of the circuit (ie the negative side of the power supply. Some MOSFETS, particularly power MOSFETS have source and substrate connected internally by the manufacturing process.

The slope of the transconductance characteristic is called the "transconductance" or "mutual conductance" of the device. It is given the symbol $\boldsymbol{g_m}$ and plays an important role in signal amplification.

Output Characteristics

The output characteristics are important because they indicate the degree of independence between output (controlled) current and the voltage difference imposed by the external circuit on the output terminals of the device. Transistors are often used as amplifiers or switches and in both applications a small input voltage change gives rise to a large change in voltage across the output terminals. Ideally the output (controlled) current will be determined entirely by the (control) input voltage.

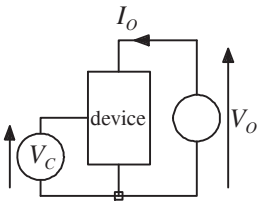


Figure 2a

definition of variables in the output characteristic of figure 2b.

Figure 2b shows an output characteristic typical of a transistor or vacuum tube labelled as "device" in figure 2a. The output characteristics usually take the form of a family of curves that show the V_O I_O relationship for a number of different control inputs, V_C. The slope of the output characteristic, $\Delta I_O/\Delta V_O$, is small and ideally zero; it depends mainly on device internal geometry. There is an obvious change in the behaviour at low values of V_O that arises because the insides of the device need a certain voltage across them before they start working as desired. The size of this low voltage

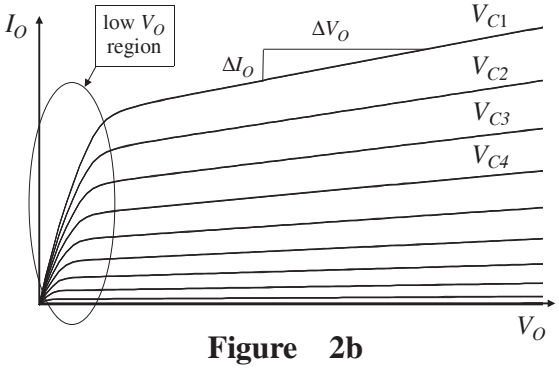


Figure 2b

A typical output characteristic. This one is for a JFET

region (which unfortunately has different names in different devices) is different for different device types and more detail is given in the discussion of each transistor type. There are a number of key points about output characteristics:

(i) The output characteristic curves are all basically the same shape - they all have a low voltage region after which the controlled current is substantially independent of V_O.

(ii) The BJT has a much smaller low voltage region than the FETs (a couple of hundred mV rather than a couple of V) and vacuum tubes.

(iii) The slope of the output characterisic at high V_O increases with increasing I_O.

About the transistors

Three transistor types have been included in figure 1b. There are actually many more types of transistor in existence but most of these are variations designed for relatively specialised applications. The three already mentioned cover most application areas.

BJTs

BJTs are the oldest of the transistors. First demonstrated in 1949 it is now a very mature technology. Early devices were made of germanium and had maximum operating frequencies of about 10kHz. The frequency was limited by the technology, not the material. Silicon became the material of choice in the 1960s and by the end of that decade devices that would work up to 5GHz were becoming available. Bipolar transistors can now operate at frequencies in excess of 100GHz. Small signal transistors are designed to operate at currents of mA and a few 10s of volts whilst some power transistors can cope with 1000s A at around 1000V. Some transistors are made from materials other than silicon but most BJTs are made from silicon.

There are two main types of BJT structure; n-p-n and p-n-p, the names indicating the ordering of semiconductor material polarities (n-type or p-type) that make up the device. The BJT in figure 1b is an n-p-n structure in which a thin layer of p-type material (the base) is sandwiched between two layers of n-type material called the emitter and collector. (The p-n-p structure consists of a thin n-type base sandwiched between a p-type emitter and a p-type collector.) There is a p-n junction between base and collector and base and emitter. The base-collector junction is usually reverse biassed whilst the base-emitter junction is usually forward biassed. It is between the base and emitter that the control voltage is applied and this means that V_{BE} is always in the region of 0.7V.

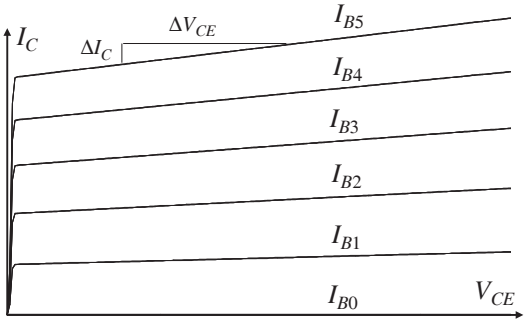


Figure 3
A BJT output characteristic.

The output characteristic of an n-p-n BJT is shown in figure 3. I_C is exponentially related to V_{BE} but is related to I_B by a constant, h_{FE}, called the "static current gain". Thus in output characteristic plots, base current (rather than base voltage) is increased in equal increments.

The thing to notice here is that the **collector current is mainly controlled by the base current (or base-emitter voltage)** although there is also a small dependence of I_C upon V_{CE}.

In other words as far as the circuit connected to the collector is concerned, the collector of

the transistor looks like a Norton equivalent circuit with a current source (whose magnitude is controlled by I_B or V_{BE}) in parallel with a resistance $\Delta V_{CE}/\Delta I_C$.

The characteristics of a p-n-p transistor are shown in figure 4. Notice that the shapes are the same as those for the n-p-n but the characteristics have been rotated by 180° about their origins. The characteristics of p-n-p devices are sometimes described as complementary to those of n-p-n devices and pairs of devices with matched characteristic shapes are sometimes called "complementary pairs".

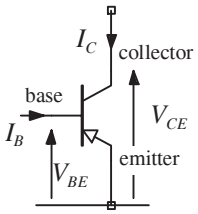


Figure 4a

The symbol for a p-n-p BJT. Note that the arrow on the emitter points towards the base.

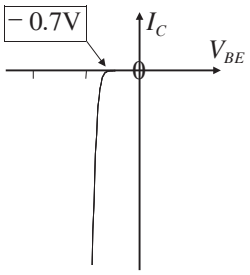


Figure 4b

The transconductance characteristic of a p-n-p BJT. Note that VBE is typically -0.7V

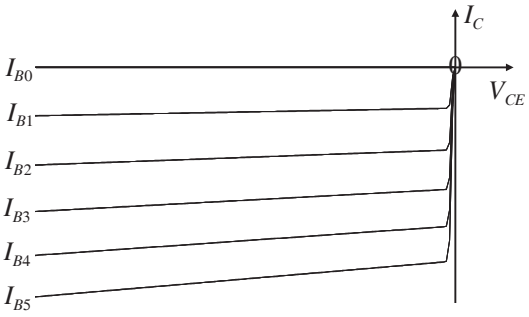


Figure 4c

The output characteristic of a p-n-p BJT. Note that I_{B1} to I_{B5} will be negative since I_B will be in a direction opposite to that shown in figure 4a.

The BJT differs from other transistors in that its transconductance characteristic is accurately defined by the behaviour of electrons in semiconductors and is relatively independent of device geometry. The relationship between I_C and V_{BE} is given by

$$I_C = I_{C0}\left(\exp\left(\frac{eV_{BE}}{kT}\right) - 1\right) \qquad \textbf{(1)}$$

For forward bias of the base emitter junction, the normal operating mode for amplifier applications, the exponential term is much larger than unity and equation **(1)** can be approximated by

$$I_C \approx I_{C0}\exp\left(\frac{eV_{BE}}{kT}\right). \qquad \textbf{(2)}$$

The dc or static current gain of the transistor is usually written symbolically as h_{FE} and is simply the ratio of collector to base current. h_{FE} is slightly dependent on I_C, being lower at the extremes of low and high I_C than it is for middle values of I_C. h_{FE} is very dependent on process variations and geometry (particularly the base layer thickness) and a range of 100 to 400 is not unusual in BJTs of the same nominal type designed for small signal amplifier applications. The relationship between I_C, I_B and h_{FE} is

$$h_{FE} = \frac{I_C}{I_B} \qquad \textbf{(3)}$$

Summing currents into the BJTs in both figures 1b and 4a leads to $I_B + I_C = I_E$ where I_E is the current flowing out of the emitter of the BJT. Since I_C is typically very much greater than I_B, this relationship can usually be approximated by $I_C \approx I_E$.

MOSFETS

MOSFETS (the name is an acronym made from Metal-Oxide-Semiconductor Field Effect Transistors) first appeared in the mid 1960s as small signal amplifiers and as small scale logic ICs but really took off at the end of the 1970s when the power MOSFET appeared. Power MOSFETS offered qualities that made them attractive alternatives to BJTs in many switching applications - especially in the 100s kHz range. Also in the late 1970s, MOSFETS entered the computer processor and memory arena in the form of large scale integrated circuits. They now dominate the computer arena.

The control electrode of a MOSFET is called the "gate", a metallised rectangle on the surface of the semiconductor that is insulated from it by a thin layer of insulator (usually silicon dioxide). This means that in principle no current is drawn through the control input and the device is a true field effect device. In practice there is always a tiny current, usually of the order of pA, flowing into the control input because no insulator is perfect. A conducting channel is induced on the surface of the semiconductor underneath the gate by applying a postive voltage to the gate with respect to the source, V_{GS}. One end of the gate overlaps the drain and the other overlaps the source and the channel, when formed, connects drain and source and forms the controlled current path. The channel begins to form at a particular V_{GS} known as the "threshold voltage" V_{TH}, and gets wider (more conductive) as V_{GS} increases above V_{TH}.

The output characteristics of MOSFETs are very similar in appearance to those of BJTs. They are usually plotted in the form of a family of curves of drain-source current, I_D, against drain-source voltage, V_{DS}, for a number of equal increments in the control input, V_{GS}, as shown in figure 5. The voltage increments have been added here to show the effect of threshold voltage - nothing happens in this particular MOSFET until V_{GS} gets somewhere between 2V and 2.5V. Other MOSFETS would have a different V_{TH} so activity would start at a different V_{GS}. The effect of V_{TH} can also be seen on the transconductance characteristic of figure 1a. The main difference between the characteristics of the BJT (figure 3) and the MOSFET (figure 5) is that in figure 5 the region at low V_{DS} where I_D is very dependent on V_{DS} extends over a couple of volts whereas in figure 3 this region extends typically over tens of mV to a couple of hundred mV.

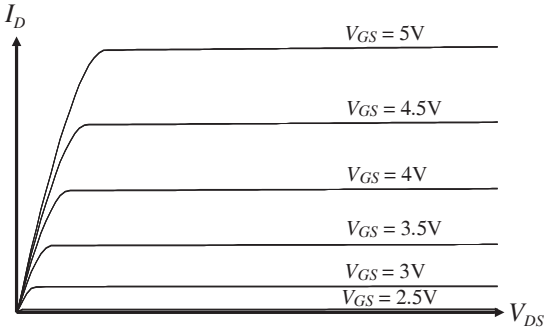


Figure 5

The output characteristics of a MOSFET

The slope of the characteristic at high V_{DS} is a function of the geometrical design of the MOSFET and a wide range of slopes can be observed from different devices. The Norton model of controlled current source in parallel with a large resistor that represents the behaviour of a BJT collector is also appropriate to model the behaviour of the drain of a MOSFET.

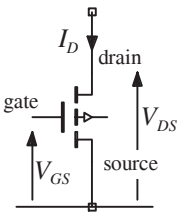


Figure 6

The symbol for a p-channel MOSFET.

As for BJTs, there are two main types of MOSFET; n-channel and p-channel. The p-channel device is the complement of the n-channel device and the relationship between the characteristics of n-channel and p-channel MOSFETS is similar to that between n-p-n (shown in figures 1a and 3) and p-n-p (shown in figures 4b and 4c) BJTs. The symbol for a p-channel MOSFET is shown in figure 6 - note that the arrowhead on the substrate

connection points away from the p-channel.

The MOSFET is governed by a square law transconductance equation rather than the exponential law that governs a BJT. The drain current is given by

$$I_D = a(V_{GS} - V_{TH})^2 \quad \textbf{(4)}$$

"a" is a constant set mainly by device geometry. The square law relationship of equation **(4)** is much less steep than the exponential relationship for a BJT and this is why the MOSFET has a lower transconductance per unit device area than the BJT. The notion of current gain is meaningless in the context of a MOSFET because input current is ideally zero. When the MOSFET is fully conducting and the drain source voltage is close to zero, the device behaves like a resistance, $r_{DS\,ON}$, whose value (which is specified by manufacturers for devices designed for switching applications) depends upon device geometry.

JFETs

Although JFETs (the name comes from Junction Field Effect Transistor) were conceived before BJTs, technological difficulties delayed their realisation for a decade after the invention of the BJT. The terminal names are the same for the JFET as for the MOSFET (except that JFETs would not normally have a substrate connection). The JFET consists of a layer of semiconductor (the channel) with drain at one end and source at the other. If the channel is n-type, the gate is a p-type deposition on the channel surface, placed between source and drain, and thus the gate-channel combination forms a p-n junction. A V_{GS} of zero, gives maximum channel conductivity and reverse biassing the gate with respect to the source reduces the channel conductivity.

The reverse biassed gate-source junction control modality gives the JFET a high gate source resistance. The transconductance is low (see figure 1a) so getting high circuit gains is difficult. Parameter spread between devices of the same type is large and this makes circuit design a relatively difficult process. As discrete devices JFETs are now only used in specialised applications but they are often used as the input transistors in IC amplifiers where their high input impedance and relative (to a MOSFET) insensitivity to static electricity are attractive.

The JFET is governed by a square law transconductance relationship similar in nature to the MOSFET but with a different constant. Its output characteristics are qualitatively similar to the MOSFET and the BJT and the drain can be modelled using a Norton circuit. As for MOSFETS, both p-channel and n-channel devices exist, the characteristics of the two types having the same relative properties as those of the two BJT or MOSFET polarities. The symbol for a p-channel JFET is the same as the n-channel one except that the arrowhead direction is reversed. Occasionally a JFET symbol in which the arrowhead is on the source lead is used. In such cases, the arrowhead points away from the gate for the n-channel device and towards the gate for the p-channel device.

Vacuum tubes

Vacuum tubes are now used only in very specialised areas; guitar amplifiers, high end audio systems, high power (10kW to MW) continuous wave and pulsed radio frequency and microwave sources for communications and long range RADAR systems. From a characteristic point of view the signal amplifying types used in audio applications behave in a very similar way to JFETs except that whereas JFETs require a supply voltage of around 10V to 20V, tubes require a couple of hundred volts.

Transistors As Amplifiers

This discussion will concentrate on bipolar junction transistors (BJTs) in amplifier applications because BJTs are by far the most commonly used amplifying device. Remember though that all amplifying devices operate in a similar way so the same principles that govern the way BJTs amplify govern the use of JFETs, MOSFETs and valves as amplifiers.

A Word About Amplifiers

The purpose of an amplifier is to increase the amplitude of a signal. If one thinks purely in terms either of voltage or of current then it is possible to change the amplitude of a signal by using a transformer. However a transformer offers no possibility of power gain – if a weak signal enters the primary of a transformer it will be at best equally weak when it emerges from the secondary. Imagine voltage is increased by a ratio of five to one. Current will be reduced by a similar ratio and the power of the signal entering the primary will be equal to the sum of the power of the signal leaving the secondary and any power lost in the transformer. The crucial factor about an amplifier is its ability to offer *power gain*. At low frequencies, one is usually more interested in the factor by which the signal (voltage or current) amplitude has been magnified than in the signal power gain which tends to be a more important parameter at higher frequencies (> 50 MHz). Several measures of gain are available:

Voltage Gain is the ratio of the output voltage amplitude and input voltage amplitude. It is used when the parameter of interest is the signal voltage amplitude. It is used at low frequencies (100 MHz or less). An ideal voltage amplifier has infinite input resistance (i.e. it draws zero current from the signal source driving it) and has zero output resistance (i.e. it can supply unlimited current to its load).

Current Gain is the ratio of the output current amplitude and input current amplitude. It is used when the parameter of interested in is the signal current amplitude. It is also used at low frequencies. An ideal current amplifier has zero input resistance (i.e. there is no signal voltage at the input) and infinite output resistance (i.e. it can supply unlimited voltage to its load).

Power Gain is the ratio of the output signal power to the input signal power. Power gain is used at high frequencies in "impedance matched" systems where the effects of electromagnetic propagation in the circuit cannot be ignored. In an impedance matched system all output impedances are equal to all impedances at a value known as the "characteristic impedance". $50\ \Omega$ is a common characteristic impedance in communications and radar applications, television systems use $75\ \Omega$.

Note that in an impedance matches system knowledge of any one of these three gains automatically defines the other two.

There are two other kinds of gain that are of interest in special applications; transconductance and transresistance. Transconductance is the ratio of the output signal current to the input signal voltage and is measured in Amps per Volt (or Siemens but occasionally written as Mhos as well). Transconductance is an important concept for all amplifying devices. Transresistance is the ratio of output voltage to input current and is measured in Volts per Amp or Ohms.

The Mechanism of Amplification

All amplifying devices can be regarded as circuit elements that have their output current controlled by an input voltage. The characteristic that describes this behaviour is known as the transconductance characteristic (or occasionally mutual characteristic) because it relates output current to input voltage. The transconductance characteristics for various devices are shown in Fig. 1. If a signal is regarded as a small change or "perturbation" around some average value (often zero), there are obvious problems with these characteristics from an amplification point of view. For example, a signal with an average value of zero applied to a BJT would cause no change in I_C for all signal voltages below 0.7 V. In other words the signal voltage below 0.7 V would effectively be lost. This is usually not an acceptable state of affairs and consequently the signal is added to a d.c. voltage, known as a bias voltage, to ensure that I_C can respond to the whole of the signal.

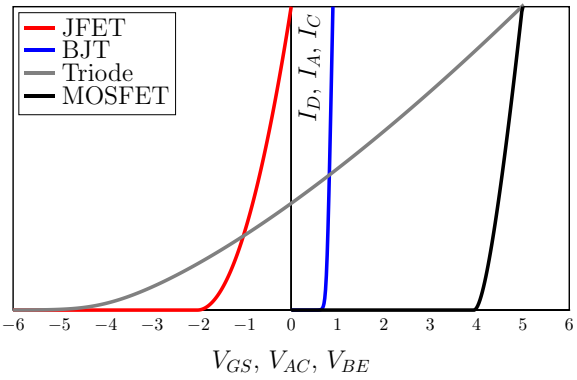


Figure 1: Example transconductance curves for, JFET (red), triode (grey), BJT (blue), MOSFET (black).

The situation is shown in the diagram of Fig. 2. If ΔV_{BE}, the signal, was applied with no bias, i.e. with its average value equal to zero there would be no change of I_C and so $\Delta I_C = 0$. If, on the other hand, a bias voltage, V_{BEB}, is added to the signal, there is a substantial change in I_C as a result of the signal. The same arguments hold for all the other devices although the best choice of bias voltage will be different for each.

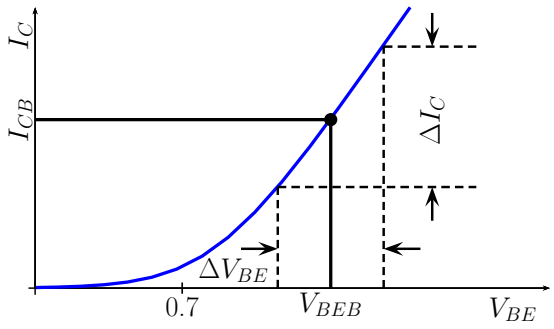


Figure 2: A BJT transconductance curve with quiescent (no siganl or d.c.) conditions shown (solid lines) and the extent of signal swing shown (dashed lines)

The relationship between ΔI_C and the signal that caused it, ΔV_{BE} is the "small signal transconductance", g_m, of the device being used. g_m is the slope of the transconductance characteristic at the bias point (V_{BEB}, I_{CB}). Since the transconductance characteristic is not a straight line, g_m, varies with V_{BEB} and indeed within ΔV_{BE} if ΔV_{BE} is not sufficiently small. It is usually assumed that ΔV_{BE} is sufficiently small for the transconductance characteristic to be approximated as a straight line over the range of V_{BE}.

In Fig. 3, the changes in collector current, ΔI_C, are converted into an output signal voltage using a resistor, R_L. An input voltage of (1),

$$V_{IN} = V_{BEB} \pm \frac{\Delta V_{BE}}{2} \tag{1}$$

will give a collector current change of (2),

$$I_C = I_{CB} \pm g_m \frac{\Delta V_{BE}}{2} \tag{2}$$

remember,

$$g_m \equiv \frac{\Delta I_C}{\Delta V_{BE}} \tag{3}$$

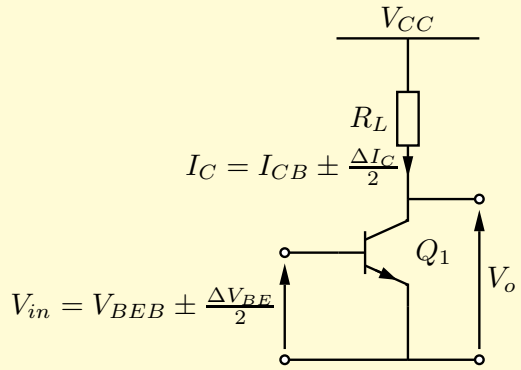


Figure 3: A one transistor amplifier including DC and AC voltages and currents.

for a BJT, and this will in turn give rise to a change in collector voltage of,

$$V_O = V_{CC} - I_C R_L \tag{4}$$

$$= V_{CC} - I_{CB} R_L \mp g_m R_L \frac{\Delta V_{BE}}{2} \tag{5}$$

$$\equiv V_{OB} \pm \frac{\Delta V_O}{2} \tag{6}$$

where V_{OB} is the output voltage obtained when the signal is zero,

$$V_{OB} = V_{CC} - I_{CB} R_L \tag{7}$$

and $\frac{\Delta V_O}{2}$ is the component of the output voltage due to the signal perturbation,

$$\frac{\Delta V_O}{2} = -g_m R_L \frac{\Delta V_{BE}}{2} \tag{8}$$

By using the relationship between ΔV_O and ΔV_{BE} it is possible to estimate the voltage gain of the amplifier,

$$\Delta V_O = -g_m R_L \Delta V_{BE} \tag{9}$$

or

$$\frac{\Delta V_O}{\Delta V_{BE}} = -g_m R_L = \text{gain} \tag{10}$$

Note that:

1. The bias conditions V_{BEB}, I_{CB} and V_{OB} do not explicitly appear in the expression for gain although it must be remembered that g_m is a function of V_{BEB}.

2. The gain is negative. This simply means that an increase in input voltage leads to a decrease in output voltage and vice versa. In signal terms it implies inversion of a 180° phase shift.

Point 1 above is very important because it suggests that the bias conditions and the signal conditions can be considered separately. Defining a stable set of bias condition is one of the primary objectives of amplifier circuit design.

BJT Biassing

BJTs are the odd ones out in the family of amplifying devices because they need to draw an input current in order to operate. A given collector current I_C will require a base current I_B to support it and the two are related by,

$$\frac{I_C}{I_B} = h_{FE} \tag{11}$$

see Fig. 4. h_{FE} is the large signal static current gain of the BJT. It is approximately independent of I_C but it varies with temperature and there is a large spread of values (typically a factor of five) from device to device of the same type. Control of the bias conditions must not therefore fall to the transistor but should be accomplished by well defined circuit elements such as resistors.

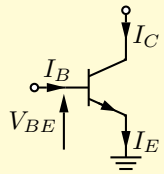
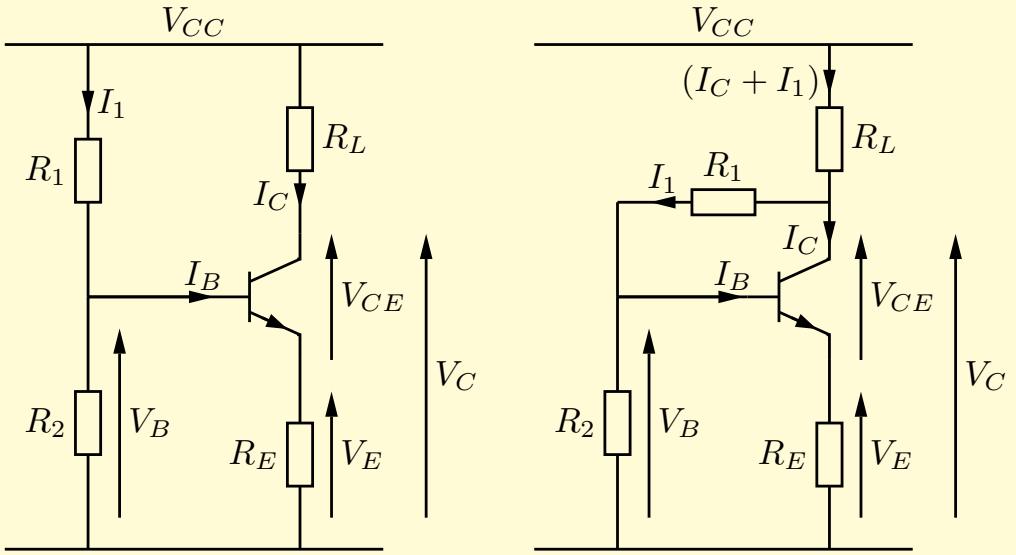


Figure 4: BJT terminal currents & voltages

Two types of bias circuit are suitable for single transistor BJT amplifiers (Fig. 5). The objective of both of these bias circuits is to control the collector current, I_C.

In both cases this control is achieved by negative feedback. In circuit 1 the voltage V_B defined by V_{CC}, $R_1 + R_2$, is made up of $V_E + V_{BE}$. If V_E is made large compared to changes expected in V_{BE} (either as a result of temperature changes or device to device variation) the V_E, and hence I_C is substantially constant. In circuit 2 R_E provides negative feedback as in circuit 1 but there is a second source of negative feedback from V_C via R_1 and R_2. I_C will tend to reduce V_C, hence reducing V_B and counteracting the increase in I_C. Circuit 1 will not operate satisfactorily with $R_E = 0$ because under such a condition, all negative feedback has been removed. Circuit 2 will operate with $R_E = 0$ because there still remains the negative feedback path from V_C via R_1 and R_2. It is usual in the analysis of both circuit 1 and circuit 2 to assume that I_B is negligible and it is usual in design to make sure that the assumption is valid.



(a) Circuit 1 (b) Circuit 2

Figure 5: Two one transistor amplifiers, showing components important for DC opperation.

Working Out the Bias Conditions

Circuit 1 – Assume I_B is negligible, $V_{BE} \approx 0.7$ V and $h_{FE} >> 1$ (i.e. $I_C \approx I_E$).

$$V_B = \frac{V_{CC}\, R_2}{R_1 + R_2} \text{ by potential division} \tag{12}$$

$$V_B = V_E + 0.7 = V_E + V_{BE} \text{ by Kirchhoff's Voltage Law} \tag{13}$$

$$I_E \approx I_C = \frac{V_E}{R_E} = \frac{V_B - 0.7}{R_E} = \frac{1}{R_E}\left[\frac{V_{CC}\, R_2}{R_1 + R_2} - 0.7\right] \tag{14}$$

$$V_C = V_{CC} - I_C\, R_L \text{ by } \mathbf{K}\text{irchhoff's } \mathbf{V}\text{oltage } \mathbf{L}\text{aw (K.V.L)} \tag{15}$$

Circuit 2 – Assume I_B is negligible, $V_{BE} \approx 0.7$ V and $h_{FE} >> 1$ (i.e. $I_C \approx I_E$).

$$I_1\, R_2 + I_1\, R_1 + (I_1 + I_C)\; R_L = V_{CC} \text{ (K.V.L)} \tag{16}$$

$$\text{or } V_{CC} = I_C\, R_L + I_1\, (R_L + R_1 + R_2) \tag{17}$$

$$I_1\, R_2 = V_E + V_{BE} = V_E + 0.7 \text{ (K.V.L)} \tag{18}$$

$$\text{or } I_1\, R_2 = I_C\, R_E + 0.7 \tag{19}$$

either I_1 or I_C may be eliminated from (17) using (19) for example, eliminating I_1 gives,

$$V_{CC} = I_C\, R_L + \frac{I_C\, R_E + 0.7}{R_2}\,(R_L + R_1 + R_2) \tag{20}$$

$$\text{or } I_C = \frac{V_{CC} - \dfrac{0.7\ (R_L + R_1 + R_2)}{R_2}}{R_L + \dfrac{R_E\,(R_L + R_1 + R_2)}{R_2}} \tag{21}$$

This result for I_C can be used in (19) to find I_1. V_C is found using,

$$V_C = V_{CC} - (I_C + I_1)\ R_L \tag{22}$$

Notes

- It is not the results that are important, but the application of the basic circuit rules that lead to them.
- The only transistor voltage drop that should appear in equations is V_{BE}. V_{CB} and V_{CE} do not and should not appear in equations for amplifiers.
- The assumption "I_B is negligible" really says that the existence of I_B does not disturb the potential at the transistor base significantly.
- Always check that the solution to equations (17) and (19) in circuit 2 is self consistent.

Design of Bias Circuits

The design process for single transistor amplifiers involves choosing one of the two circuits and deciding on appropriate values of node voltages and transistor collector current and then working out sensible component values. The choice of circuit depends to some extent on the application area. For low frequency applications, either circuit 1 or circuit 2 can be used. For high frequency applications, circuit 2 with $R_E = 0$ tends to be used.

The value of I_B must be considered during the design process to ensure that the design will satisfy the criterion "I_B is negligible". The case most likely to violate the criterion is *smallest* h_{FE}. Remember that the manufacturer will specify a maximum and minimum value of h_{FE} for a particular transistor. Remember also that the purpose of the bias circuit is to control I_C. Thus, $I_{B_{max}} = \frac{I_C}{h_{FE_{min}}}$

and $I_{B_{max}}$ is usually taken to be negligible if I_1, the current at the top of the biasing chain $\geq 10\, I_{B_{max}}$.

The value of I_C, V_C, V_E and V_B are a little more complicated to decide on because they will affect the signal properties of the amplifier. A few of the compromises are:

1. The value of collector voltage will affect the output voltage swing available. For example in cirucit 1, V_C can lie anywhere between V_{CC} and V_E. To maximise output voltage swing for a symmetrical signal like a sinusoid, V_C should be placed halfway between V_{CC} and V_E. i.e.

$$V_C = \frac{V_{CC} + V_E}{2} \text{ for max symmetrical swing} \tag{23}$$

2. Clearly both V_{CC} and V_E will affect the max symmetrical swing, which is $V_{CC} - V_E$. V_{CC} is usually set by what is available within the rest of the system, V_E can be chosen.

3. Larger V_E gives more precise control of I_C. For a BJT it is unwise to let V_E fall below 1 V in a circuit such as number 1.

4. I_C is chosen by considering the nature of the load, but it also affects the effective input resistance of the transistor[1] and output resistance of the amplifier. In general one would aim for a condition $R_L << $ [input resistance of the next stage].

5. R_1 and R_2 should be as large as possible consistent with the maintenance of the appropriate relationship between $I_{B_{max}}$ and I_1.

To visualise how the supply voltage will be divided up between the various parts of the circuit, it is helpful to draw a chart such as Fig. 6. This makes it clear that increasing V_E reduces the range of voltage that can be occupied by V_C and that the best position for V_C with symmetrical signals is halfway through the available range. Note that in this chart the minimum available value of V_C is V_B whereas in the comments above it is V_E. Most amplifier transistors will work satisfactorily with V_C as low as a few hundred mV above V_E but there are good reasons for saying that ideally V_C should not fall below V_B.

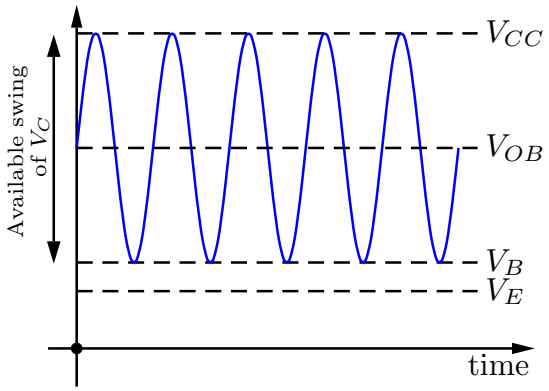


Figure 6: The transistor electrode voltages in the one transistor amplifier circuits.

[1] because I_C controls g_m via $g_m = (e\, I_C)/(k\, T)$ and $r_{be} = \beta/g_m$ so r_{be} and I_C are linked.

Notes

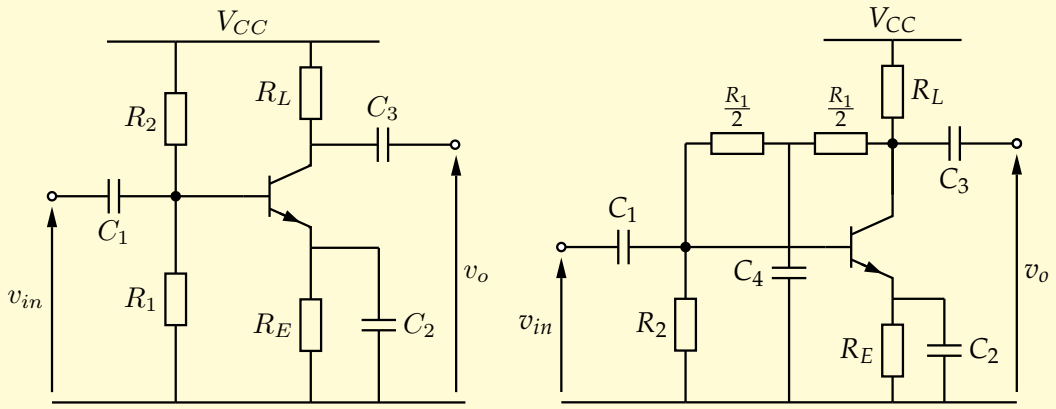
1. The design process is a compromise.
2. No two designers would make identical decisions.
3. Never specify component values more tightly than is necessary.
4. Use "preferred" (E12, E24 etc.) values.

Coupling and Decoupling

Transmitting signals from one place to another in a circuit is called "coupling". Removing signals from nodes in the circuit is called "decoupling". Capacitors or transformers can be used for coupling leading to so called "R-C" and "transformer coupled" amplifiers. Amplifiers that are required to amplify d.c. signals, such as strain gauge amplifiers or thermocouple amplifiers, cannot use transformers or capacitors – instead they must be "direct coupled" or "d.c." coupled. Direct coupled amplifiers use many transistors and will not be considered further at this point. Transformer coupling is attractive at high frequencies or in tuned amplifiers where resonant circuits are used. Capacitor coupling is used at lower frequencies. For example, an audio amplifier will be a combination of d.c. and capacitor coupling; a radio or TV I.F. amplifier will be transformer coupled.

Circuits 1 and 2 are shown in Fig. 7 with coupling and decoupling capacitors included. For the purposes of this discussion, a capacitor may be regarded as an open circuit (infinite impedance) to d.c. and a short circuit (zero impedance) to signals. Note that in Fig. 7 the signal voltage, v_{in} and v_o are in lower case v whereas the bias conditions are in upper case V. In both cases,

- C_1 couples the signal from the signal source to the transistor base without allowing the source to affect the bias conditions or the bias conditions to affect the source.
- C_2 decouples the emitter node of the transistor. In other words C_2 short circuits the emitter node of the transistor to ground as far as signals are concerned. This prevents R_E having the same stabilising effect on the signals as it has on the d.c. conditions. by removing the negative feedback caused by R_E. The circuit voltage gain $\frac{v_o}{v_i}$ is much larger if C_2 is incuded in the circuit than it would be if R_E was not bypassed by a capacitor.
- C_3 couples the signal from the output (collector node) to the load without allowing disturbance of the bias conditions or the imposition of a d.c. voltage accross the load.



(a) Circuit 1 (b) Circuit 2

Figure 7: Two one transistor amplifiers.

In circuit 2,

- C_4 decouples the mid point of R_1. Since R_1 is also a negative feedback path it will reduce the circuit gain if a.c. as well as d.c. voltages can be transmitted via R_1 to the base. C_4 short circuits the mid point of R_1 to ground as far as a.c. (signal) voltages are concerned hence eliminating any effects of the negative feedback via R_1 on circuit gain.

How the Transistor Interacts with Signals

The transistor is characterised by non-linear characteristic curves (see notes on characteristics). The rest of the amplifier circuit consists of standard circuit elements such as resistors and capacitors so it is convenient to represent the behaviour of the transistor towards the signal in standard circuit terms. A circuit representation of how the transistor behaves towards a signal is called a "small signal model" – it assumes that the signal represents only a small deviation from the bias conditions. All amplifying devices can be represented by a small signal model.

A Small Signal BJT Model

The underlying process of amplification involves the device "transconductance" – i.e. the amplifying device can be considered as a current source whose magnitude is controlled by the input voltage. For small signals it is the slope of the transconductance characteristic at the bias point which is of interest (see Fig. 8). For a BJT,

$$I_C = I_{CO}\left(\exp\left(\frac{e\,V_{BE}}{k\,T}\right) - 1\right) \qquad (24)$$

and the slope at the bias point is,

$$\frac{\mathrm{d}I_{CB}}{\mathrm{d}V_{BEB}} = I_{CO}\,\frac{e}{k\,T}\,\exp\left(\frac{e\,V_{BE}}{k\,T}\right) = g_m \qquad (25)$$

for a conducting diode,

$$\exp\left(\frac{e\,V_{BE}}{k\,T}\right) >> 1 \qquad (26)$$

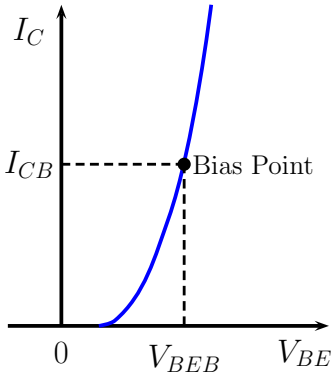


Figure 8: A BJT transfer characteristic showing the bias or quiescent point. The characteristic (blue line) is expressed by (24).

so

$$I_C = I_{CO}\left(\exp\left(\frac{e\,V_{BE}}{k\,T}\right) - 1\right) \approx I_{CO}\exp\left(\frac{e\,V_{BE}}{k\,T}\right) \qquad (27)$$

substituting,

$$\therefore \frac{\mathrm{d}I_C}{\mathrm{d}V_{BE}} = I_{CO}\,\frac{e}{k\,T}\,\exp\left(\frac{e\,V_{BE}}{k\,T}\right) = \frac{e\,I_C}{k\,T} = g_m \qquad (28)$$

$g_m = \frac{e\,I_C}{k\,T}$ where I_C is the quiescent or d.c. collector current. It is one of the fundamental BJT relationships and should be remembered. At room temperature, $\frac{e}{k\,T} \approx 40$ This transconductance consideration leads to the simplest BJT model, shown in Fig. 9. It is a good low frequency model for JFETs, MOSFETs and valves (although these devices and the BJT would probably have a resistor in parallel with the current source to take account of the slope on the output characteristics).

The BJT, however, is unique in having an input resistance that can rarely be ignored. The input resistance if found by working out the slope of the input characteristic, at the operating or quiescent point, in an indirect way,

$$r_{be} = \frac{\mathrm{d}V_{BE}}{\mathrm{d}I_B} = \frac{\mathrm{d}I_C}{\mathrm{d}I_B}\cdot\frac{\mathrm{d}V_{BE}}{\mathrm{d}I_C} \qquad (29)$$

$$\frac{\mathrm{d}I_C}{\mathrm{d}I_B} = \beta = \text{ small signal current gain} \qquad (30)$$

$$\frac{\mathrm{d}V_{BE}}{\mathrm{d}I_C} = \frac{1}{g_m} \text{ from (28)} \qquad (31)$$

$$\therefore r_{be} = \frac{\beta}{g_m} \qquad (32)$$

another vital BJT relationship.

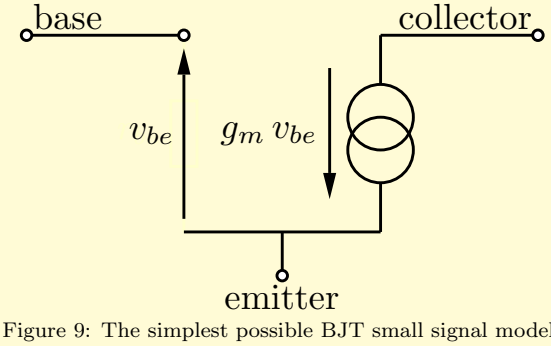


Figure 9: The simplest possible BJT small signal model.

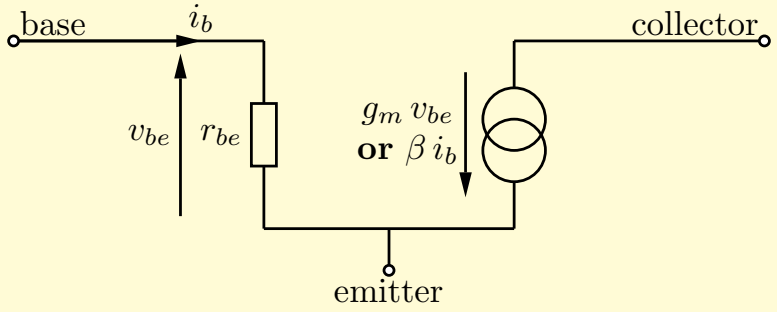


Figure 10: A simple BJT smal signal model including r_{be}.

Note that $\mathrm{d}V_{BE}$, $\mathrm{d}I_B$, $\mathrm{d}I_C$ are the small changes to the bias conditions and could be represented at small signal quantities v_{be}, i_b and i_c,

$$r_{be} = \frac{\beta}{g_m} = \frac{\mathrm{d}V_{BE}}{\mathrm{d}I_B} = \frac{v_{be}}{i_b} \tag{33}$$

$$\text{so } g_m\, v_{be} = \beta\, i_b \tag{34}$$

This is an interesting result because it says that the output current generator in the BJT model may be thought of as being controlled by the current through r_{be} or by the voltage across r_{be}. People get very worked up over the question "is a BJT a current or transconductance amplifier?" The answer really is that it doesn't matter – use whichever is more convenient for any particular problem. The discussion of the BJT in transconductance terms is helpul because the transconductance viewpoint is common to all three terminal amplification devices. No other device can be looked at as a current amplifier. Including r_{be} in the model leads to Fig. 10.

Notes

- Usually $\beta \neq h_{FE}$. β is a small signal parameter and h_{FE} is a large signal parameter.
- β is sometime given as h_{fe}. h_{fe} is derived from a different modelling system and except at high frequencies they can be taken as equal.
- There are other elements one could add to this model to explain details of behaviour. One example is a resistor in parallel with the current generator to model the slope on the output characteristic. The simple model in Fig. 10 consisting of input resistance and output current source is reasonable for a wider range of applications and will be used for the rest of this course.

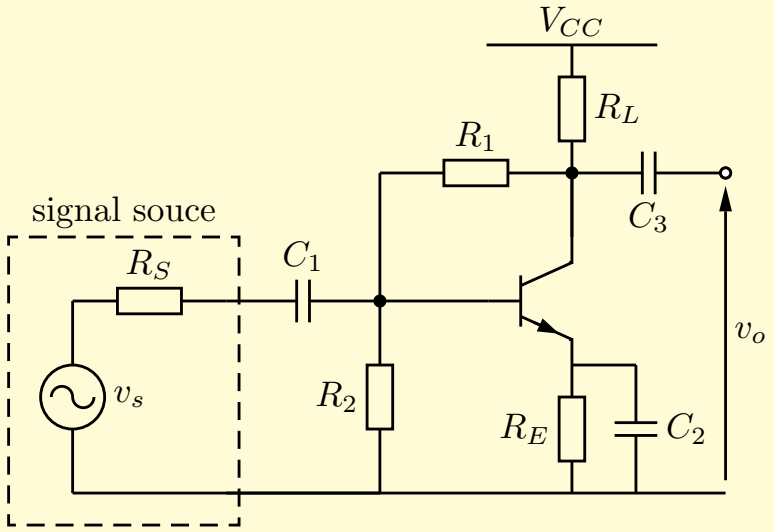


Figure 11: Circuit 1 with AC and DC feedback via R_1 and DC feedback via R_E.

The Small Signal Equivalent Circuit

In principle this is a straightforward task – it is a matter of drawing a circuit which describes what a signal in the circuit would experience, so it is necessary to look at the circuit from the signal's point of view. There are two important consequences of being interested only in the signal's interaction with the circuit.

1. All d.c. voltage sources (such as power supplies are replaced by their Thévenin equivalent impedance (i.e. 0 Ω – a short circuit).

2. All d.c. current sources are replaced by their Thévenin equivalent impedance, i.e. ∞ Ω – an open circuit.

In addition, since for the purposes of this course capacitors are considered as open circuit at d.c. adn short circuits to a.c., all capacitors are replaced by short circuits. The transistor is replaced terminal for terminal by its small signal model. Consider circuit 2, without decoupling R_1, which has the circuit diagram shown in Fig. 11. This circuit has the small signal model shown in Fig. 12. This small signal model can be tidied up to form Fig. 13.

Note that the small signal equivalent circuit will vary according to the circuit it is derived from. Do not attempt to learn the result – attempt instead to acquire the skill of deriving the small signal model for any circuit.

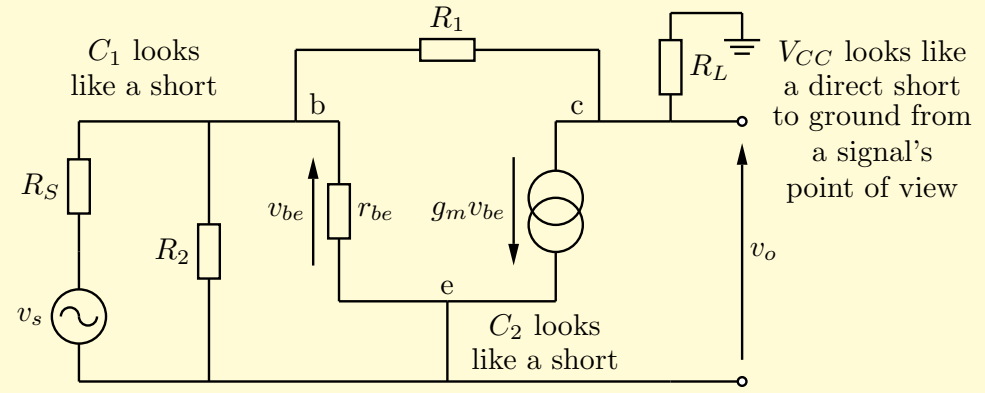


Figure 12: A "terminal for terminal" small signal model of the circuit in Fig. 11

Once the equivalent circuit is obtained, normal circuit analysis methods can be used to evaluate performance. For example, to obtain the overall voltage gain, $\frac{v_o}{v_s}$, one would begin by summing the currents (applying Kirchhoff's current law) at the output note,

$$\frac{v_o}{R_L} + \frac{(v_o - v_{be})}{R_1} + g_m\, v_{be} = 0 \tag{35}$$

summing currents (K.C.L) at the input node,

$$\frac{(v_s - v_{be})}{R_S} + \frac{(v_o - v_{be})}{R_1} = \frac{v_{be}}{R_2} + \frac{v_{be}}{r_{be}} \tag{36}$$

Equations (35) and (36) can be transposed to yield respecively,

$$v_{be} = -\frac{v_o\,(R_1 + R_L)}{g_m\, R_1\, R_L - R_L} \approx -\frac{v_o}{g_m\, R_1 // R_L} \tag{37}$$

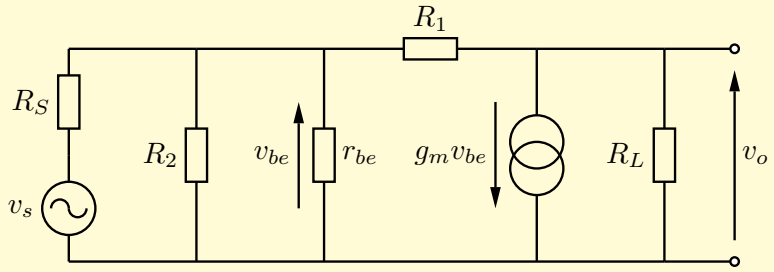


Figure 13: A tidied up version of small signal circuit diagram in Fig. 12

and

$$v_{be} = -\frac{\dfrac{v_s}{R_S} + \dfrac{v_o}{R_1}}{\dfrac{1}{R_2} + \dfrac{1}{r_{be}} + \dfrac{1}{R_s} + \dfrac{1}{R_1}} \tag{38}$$

$$= \frac{v_s\,(R_2//r_{be}//R_S//R_1)}{R_S} + \frac{v_o\,(R_2//r_{be}//R_S//R_1)}{R_S} \tag{39}$$

Eliminating v_{be} and transposing to obtain the voltage gain, $\frac{v_o}{v_s}$, required gives,

$$\frac{v_o}{v_s} = -\frac{R_1}{R_S} \cdot \frac{1}{1 + \dfrac{R_1}{g_m\,R_L\,(R_2//r_{be}//R_S)}} \tag{40}$$

and since R_1 is very large the $R_1\,/\,(g_m\,R_L\,(R_2//r_{be}//R_S))$ term will dominate the denominator giving,

$$\frac{v_o}{v_s} = -\frac{R_1}{R_S} \cdot \frac{1}{\dfrac{R_1}{g_m\,R_L\,(R_2//r_{be}//R_S)}} = -g_m\,R_L \cdot \frac{R_2//r_{be}}{R_S + R_2//r_{be}} \tag{41}$$

This expression consists of a gain term, $g_m\,R_L$ and an input potential division $(R_2//r_{be})/(R_S + R_2//r_{be})$. Note that the circuit gain is now directly dependent on the transistor parameters g_m and r_{be}; the negative feedback effects of R_1 have been eliminated. In removing R_1, the circuit is being changed from a small signal point of view, from circuit 2 in to circuit 1 with the emitter decoupled. The R_1 in circuit 1, which is necessary for correct biasing of the transistor, appears in small signal terms in parallel with R_2, hence altering the effective value of R_2 but not the form of the result.

Each circuit shape will produce its own result for gain and other performance measures so memorising this result would be unhelpful. The desirable outcome is for the student to practice the skill of deriving small signal circuit diagrams and equations until they can do it for any circuit and then to be able to interpret the results of their analysis.

Op-Amp Anatomy

Basic op-amp circuit

Introduction

Figure 1 shows a circuit that contains the basic elements of an op-amp. The elements are the simplest circuits that will perform the required basic function and so are not optimised to give

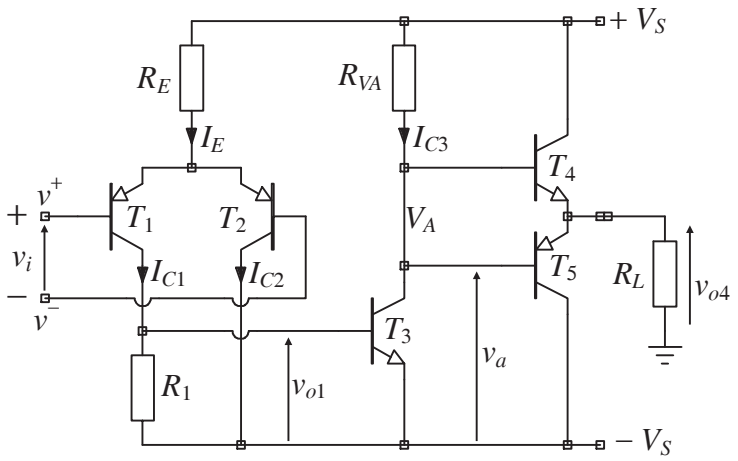


Figure 1

a good op-amp performance. The treatment that follows looks first at this basic circuit from a dc condition point of view and then explores the way the circuit responds to signals which can be regarded as small changes superimposed on the dc conditions. The study of the response of the circuit to small changes in dc conditions is called "small-signal" (ss) analysis. In principle ss analysis yields results that are frequency dependent but here we assume that frequencies are sufficiently low that no reactive effects are significant.

After identifying the problems associated with the basic circuit of figure 1, refinements are added to the circuit that increase complexity but also make the design perform more effectively as an op-amp.

Evaluating dc conditions

There are some key ideas about op-amps that must be bourne in mind when working out dc conditions:

- No op-amp will work properly without feedback. The feedback controls the gain of the circuit but also performs a crucial role in defining the circuit dc conditions. The feedback will alter the dc value of v_i in order to achieve the internal voltage drops required for proper operation. This means that if $v_o = 0$, v_i will be at the value it needs to have in order to make $v_o = 0$ and in a good op-amp this value will be very small.
- The "differential input voltage", v_i in figure 1, is the difference $v^+ - v^-$.

- The "common mode input voltage" is the average of v^+ and v^-, ie, $(v^+ + v^-)/2$

In the circuit of figure 1 the common mode input voltage will affect the internal amplifier currents so the assumption will be made here that $v^+ \approx v^- \approx 0$. It is not difficult to apply the process below to a case where common mode voltage is non-zero. Whatever the common mode voltage, $v^+ \approx v^-$ will be a valid assumption.

If $v^+ \approx v^- \approx 0$, V_{E1} and $V_{E2} \approx 0.7$ so $I_E \approx (V_S - 0.7)/R_E$. I_E splits between T_1 and T_2 to form I_{C1} and I_{C2}. I_{C1} has two functions; it must create a voltage drop of 0.7 V across R_1 in order to bias T_3 into conduction and it must provide the necessary base current for T_3. This means that I_{C1} will be $0.7/R_1 + I_{C3}/h_{FE3}$. The value of I_{C3} varies with V_A and hence with V_O but assuming $V_A = 0$, $I_{C3} = V_S/R_{VA}$. I_{C2} is returned directly to the negative supply. In the case where $v^+ \approx v^- \neq 0$, there is a common mode input voltage, v_{cm}, and $I_E \approx (V_S - v_{cm})/R_E$. The rest of the process is as just described.

The biggest problem with this simple circuit is that a small value of I_E is desirable to give the op-amp a high input resistance and for keeping noise to a minimum. It is desirable to have an equal split of I_E between I_{C1} and I_{C2} in order to minimise input stage imbalance which causes offset problems. I_{C1} supplies both I_{b3} and I_{R1} and although I_{R1} is reasonably predictable, I_{b3} depends upon h_{FE3} which may vary from one op-amp to another. This variation can lead to relatively large imbalances between I_{C1} and I_{C2}. A remedy for this problem will be described later in the "refinements" section.

Evaluating signal related behaviour

The behaviour of the circuit towards signals is evaluated with the help of ss models of the circuit. Since even the simple circuit of figure 1 contains several transistors it is most useful to look at the behaviour of each stage in turn. The objective of the analysis is to identify which circuit components are important players in key performance factors such as voltage gain. We will start the consideration of signal related effects by reviewing the ss behaviour of standard transistor connections.

Small signal review

The common emitter (CE) connection

The common emitter connection is a connection that gives a large voltage gain. It can be configured using either n-p-n or p-n-p transistors as shown in figure 2. Both the n-p-n and p-n-p versions have the same small signal equivalent circuit shown in figure 3. The resistors R_S are the Thevenin equivalent resistance feeding the base and it is assumed that the bias circuit is included within R_S. R_L represents the total resistance between the collector node and signal ground - it is often called the "collector load resistance".

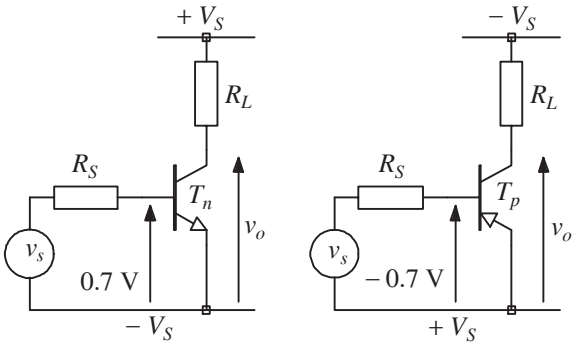


Figure 2

An n-p-n (left) and a p-n-p (right) common emitter circuit. Note the difference in power supply polarity in the two cases.

The small signal circuit of a CE amplifier is shown in figure 3. R_L usually con-

sists of three parallel components; the collector load required locally for biassing, the effective collector-emitter resistance, r_{ce}, of the transistor and the input resistance of the external load that is being driven by the amplifier. r_{ce} is often sufficiently large to make a negligible difference to this parallel combination and under such circumstances it can be ignored.

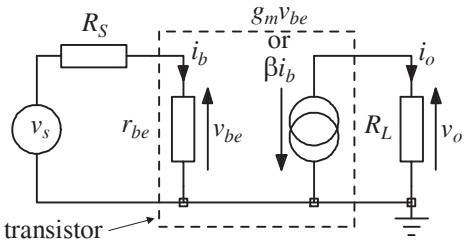


Figure 3

The small signal representation of both the circuits in figure 2

The absence of feedback in the circuit makes it straightforward to find the circuit gain.

At the output, $v_o = i_o R_L = -g_m v_{be} R_L$ since $i_o = -g_m v_{be}$ **(1)**

At the input, $v_{be} = v_s \dfrac{r_{be}}{R_S + r_{be}}$ **(2)**

using **(2)** to substite for v_{be} in **(1)** gives $\dfrac{v_o}{v_s} = -g_m R_L \dfrac{r_{be}}{R_S + r_{be}}$ **(3)**

The important conclusions are

- the gain is inverting (the "–" sign tells us this).
- gain is proportional to g_m (so large g_ms are attractive).
- gain is proprtional to R_L (so large R_Ls are attractive).
- $r_{be} \gg R_S$ must be satisfied to avoid significant input circuit attenuation.

The other parameter of interest for this transistor connection is its input resistance, r_i, looking into the transistor base terminal - that is, the effective resistance between the base terminal and ground. A quick glance at figure 3 will reveal that

$r_i = r_{be}$. **(4)**

The common emitter connection with emitter degeneration

Sometimes CE circuits have a small value of resistance - typically 10s of Ω to low kΩ - between the emitter terminal and ground as shown in figure 4. This resistance is called an "emitter degeneration" resistance. The effect that emitter degeneration has on the shape of the small signal equivalent circuit is simply to add a resistor R_E between the emitter node and ground as shown in figure 5. Unfortunately this addition significantly complicates the small signal analysis, especially if r_{ce} is included in the analisis, because R_E couples the output circuit to the input circuit. In the analysis that follows we will assume that r_{ce} has a negligible effect.

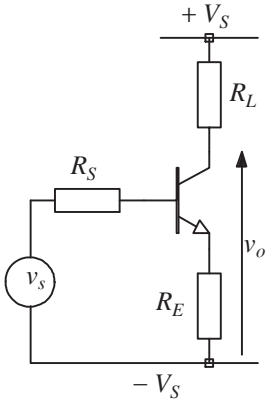


Figure 4

A common emitter amplifier with emitter degeneration

Summing currents at the emitter node in figure 5

$$i_b + g_m v_{be} = i_e \text{ or } \frac{v_{be}}{r_{be}} + g_m v_{be} = \frac{v_e}{R_E} \qquad \textbf{(5)}$$

we need to express v_e in terms of v_s, v_o, v_{be} and the circuit components. Rearranging **(5)** gives

$$v_e = v_{be} R_E \left(\frac{1}{r_{be}} + g_m \right) \approx v_{be} R_E g_m \qquad \textbf{(6)}$$

the simplification is justified since $1/r_{be} = g_m/\beta$ and $\beta \gg 1$

A second equation can be obtained by summing voltages around the input loop

$$v_s = i_b R_S + v_{be} + v_e$$

Recognising that $i_b = v_{be}/r_{be}$ and using **(6)** for v_e this becomes

$$v_s = v_{be} \left(1 + \frac{R_S}{r_{be}} + g_m R_E \right) \qquad \textbf{(7)}$$

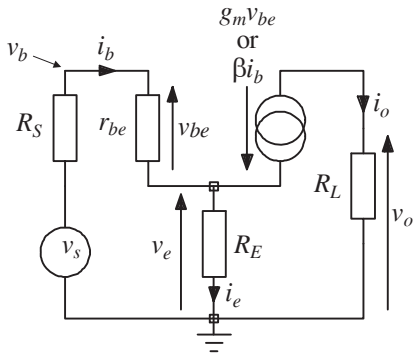


Figure 5
CE circuit with emitter degeneration

At the output side of the circuit, $v_o = i_o R_L$ and $i_o = -g_m v_{be}$. Thus, using **(7)**

$$v_o = -g_m R_L v_{be} = -\frac{g_m R_L v_s}{\left(1 + \frac{R_S}{r_{be}} + g_m R_E \right)}$$

and $$\frac{v_o}{v_s} = -\frac{g_m R_L}{\left(1 + \frac{R_S}{r_{be}} + g_m R_E \right)} = -\frac{R_L}{\left(r_e + \frac{R_S}{\beta} + R_E \right)} \quad \text{where } r_e = 1/g_m \,. \qquad \textbf{(8)}$$

The important conclusions are

- the gain is inverting
- the gain is proportional to R_L
- R_E reduces the gain
- If $R_E \gg 1/g_m$ and R_S/β, gain $\approx -R_L/R_E$

[Note that although R_E is quite commonly found in low frequency amplifiers, for high frequency (10s MHz or higher) amplifier circuits, R_E is almost always undersirable. Indeed one of the big design challenges in RF circuit design is to ensure a low impedance connection between signal ground and transistor emitter. Any impedance in the R_E position interacts with the frequency dependent aspects of the transistor's equivalent circuit in such a way as to encourage instability in the amplifier. Instability in this context means a tendency to oscillate - ie produce an output with no input - at a high frequency, always an undesirable characteristic in an amplifier.]

The presence of R_E also affects the input resistance of the circuit looking into the transistor base terminal. The input resistance is defined by v_b/i_b where v_b is the signal voltage at the base terminal with respect to signal ground.

Summing voltages and using the unsimplified form of **(6)** to express v_e in terms of v_{be}

$$v_b = v_{be} + v_e = v_{be} + v_{be} R_E \left(\frac{1}{r_{be}} + g_m \right) = v_{be} \left(1 + R_E \left(\frac{1}{r_{be}} + g_m \right) \right)$$

and since $v_{be} = i_b r_{be}$ and $g_m r_{be} = \beta$, the input resistance can be written

$$r_i = \frac{v_b}{i_b} = r_{be} + (\beta + 1) R_E \qquad \textbf{(9)}$$

- The input resistance has been increased by an amount $(1+\beta)R_E$ compared to the non R_E case of **(4)**. If $\beta = 300$, say, a typical value for an amplifier transistor, a small R_E can have a significant effect on input resistance.

The "common collector" or "emitter follower" connection

The common collector circuit is one of a class of circuits known as voltage follower circuits. The name arises because the output voltage follows closely the input voltage; the gain is very close to but always less than unity. The common collector circuit can be realised using n-p-n or p-n-p transistors; the n-p-n version is shown in figure 6. As with figures 2 and 4, it is assumed that the effective bias circuit resistance is included in R_S. Notice the similarity to the common emitter with emitter degeneration circuit of figure 4 - the only difference between that and figure 6 is that in figure 6 there is no R_L and the output is taken across R_E.

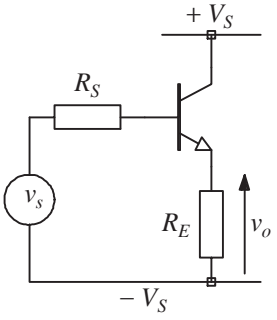


Figure 6

The emitter follower circuit

The small signal equivalent circuit of the emitter follower is shown in figure 7 which has similarities with figure 5. The analysis is very similar to that associated with figure 5 except that v_e has become v_o and does not now need to be eliminated. The analysis begins by summing currents at the emitter node, the same process that led to **(5)** and **(6)**. **(6)** is repeated below with v_e replaced by its name in this analysis, v_o.

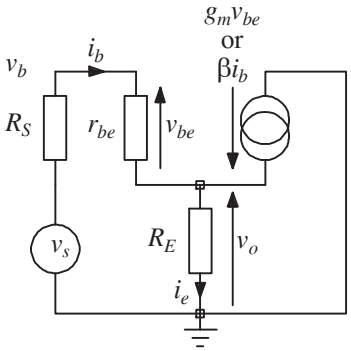


Figure 7

Small signal equivalent circuit of an emitter follower

$$v_o = v_{be} R_E \left(\frac{1}{r_{be}} + g_m \right) \approx v_{be} R_E g_m \qquad \textbf{(10)}$$

A second equation relating v_{be}, v_s and v_o is obtained by summing voltages around the input loop

$$v_s = i_b R_S + v_{be} + v_o = v_{be} \left(1 + \frac{R_S}{r_{be}} \right) + v_o \qquad \textbf{(11)}$$

and using the approximate result of **(10)** to eliminate v_{be} from **(11)** gives

$$\frac{v_o}{v_s} = \frac{r_{be} g_m R_E}{\left(r_{be} g_m R_E + R_S + r_{be} \right)} = \frac{R_E}{\left(r_e + \frac{R_S}{\beta} + R_E \right)} \quad \text{where } r_e = 1/g_m \,. \qquad \textbf{(12)}$$

The important conclusions are

- the gain is non-inverting
- the gain is very close to unity if $R_E \gg R_S/\beta$ and $1/g_m$, conditions that are usually satisfied.

The input resistance looking into the base terminal is as described for the common emitter with emitter degeneration in the analysis leading to **(9)**. The result is repeated here

$$r_i = \frac{v_b}{i_b} = r_{be} + (\beta + 1) R_E \qquad \textbf{(13)}$$

- the input resistance is dominated by the $(\beta + 1)R_E$ term.

The common base connection

Although sometimes used on its own, the common base connection is most commonly used in combination with other circuits - ie, as part of a multi transistor sub-circuit block. The circuit of a common base connected n-p-n device is shown in figure 8 and once again there is a p-n-p version of this circuit. It is assumed that any biassing resistances are included in R_S. Since I_C is large compared to I_B and $I_E = I_C + I_B$, the approximation $I_C \approx I_B$ is usually valid.

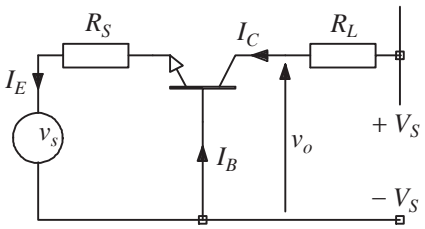


Figure 8

A common base circuit. The bias circuit is part of the thevenin resistance R_S.

The ss equivalent circuit is shown in figure 9. The effects of r_{ce} are neglected. The analytical process follows a similar pattern to the previous examples although the results are different. Start by summing currents at the emitter node,

$$i_s + i_b + g_m v_{be} = 0$$

or $$\frac{v_s - v_e}{R_S} + \frac{v_{be}}{r_{be}} + g_m v_{be} = 0 \qquad \textbf{(14)}$$

Note that $v_e + v_{be} = 0$ so $v_e = -v_{be}$ and this allows **(14)** to be rearranged to give v_{be} in terms of v_s,

$$v_{be} = -\frac{v_s}{R_S\left(\frac{1}{R_S} + \frac{1}{r_{be}} + g_m\right)} \approx -\frac{v_s}{1 + g_m R_S} \qquad \textbf{(15)}$$

since $1/r_{be} = g_m/\beta$ and $\beta \gg 1$.

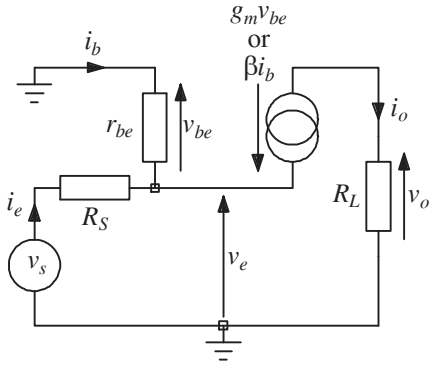


Figure 9

The small signal model of the circuit of figure 8. Note that r_{ce} is omitted from the model

At the output side

$v_o = i_o R_L = -g_m v_{be} R_L$ and combining this with **(15)** to eliminate v_{be} gives

$$\frac{v_o}{v_s} = \frac{g_m R_L}{1 + g_m R_S} = \frac{R_L}{r_e + R_S} \text{ where } r_e = 1/g_m. \qquad \textbf{(16)}$$

The important conclusions are

- the gain is non-inverting.
- gain is proprtional to R_L .
- If $R_S \gg r_e$ the gain is controlled by the ratio R_L/R_S.

The input resistance looking into the emitter of the transistor is given by

$$r_i = \frac{v_e}{i_e} = \frac{v_e}{\frac{-v_{be}}{r_{be}} - g_m v_{be}} \text{ but since } v_e = -v_{be} \text{ and } g_m \gg 1/r_{be} \text{ this reduces to}$$

$$r_i \approx \frac{1}{g_m} = r_e \text{ , a relatively low value (10s to 100s of Ohms).} \qquad \textbf{(17)}$$

Back to the simple op-amp of figure 1 . . . .

The parameters that we will work out here are overall gain and input resistance. The input resistance of the op-amp is essentially the first stage input resistance. The voltage gain of the op-amp is the voltage gain of the differential input stage multiplied by the voltage gain of the voltage amplification stage multiplied by the voltage gain of the output stage.

The input stage

The input stage circuitry is shown in figure 10. We must consider the effects of three transistors. T_1 and T_2 are the input differential pair and must be considered together and T_3 must be considered because its input resistance forms part of T_1's collector load resistance. If the input signal is regarded as v_{bT1} with respect to v_{bT2} (ie, v_{bT2} is taken as a signal ground), T_2 looks like a common base connection as far as T_1 is concerned and can be represented by its common base input resistance given by **(17)** as r_{e2} (= $1/g_{m2}$). The collector current of T_1 sees two resistors in parallel, R_1 and the input resistance of T_3. T_3 is a common emitter connection and its input resistance is given by **(4)** as r_{be3}.

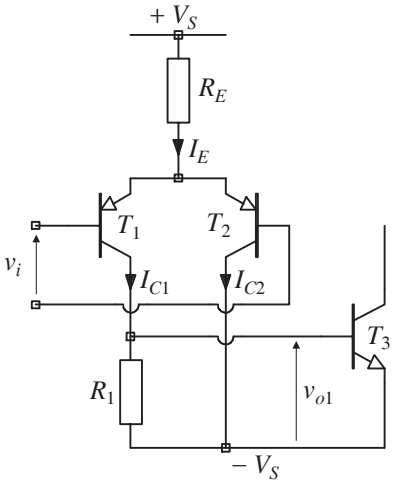


Figure 10

The circuit diagram of the input stage in the basic op-amp of figure 1.

A small signal equivalent circuit that embodies these representations of T_2 and T_3 is shown in figure 11. The circuit of figure 11 is the same as that of figure 5 with the exceptions that $R_S = 0$ and R_E and R_L become the parallel combinations $R_E//r_{e2}$ and $R_1//r_{be3}$ respectively. Since in figure 11 $R_E \gg r_{e2}$, the parallel combination $R_E//r_{e2} \approx r_{e2}$. Including these variable changes in **(8)**, the gain expression for figure 5, the voltage gain of the circuit of figure 11 is

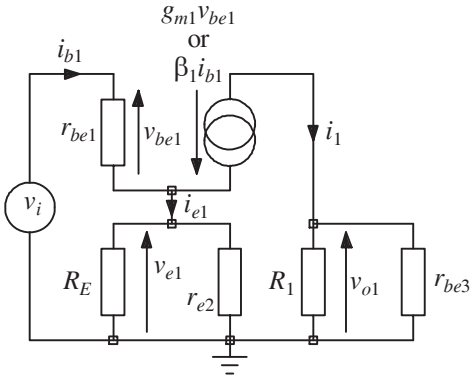


Figure 11

The small signal equivalent of figure 10. Note that T_2 has been replaced by its common base input resistance r_{e2} and that r_{be3} is in parallel with R_1.

$$\frac{v_{o1}}{v_i} \approx -\frac{R_1//r_{be3}}{r_{e1} + r_{e2}} \qquad \textbf{(18)}$$

- to maximise the gain of this circuit we need to make both R_1 and r_{be3} as large as possible.

It is tempting to think that we might also aim to reduce the $r_{e1} + r_{e2}$ term but remember that $r_e = 1/g_m$ and $g_m = eI_C/kT$. This means that to reduce r_e one must increase I_C. Since dc conditions demand $I_{C1}R_1 = 0.7$ V, an increase in I_{C1} would have to be accompanied by a decrease in R_1giving no net gain advantage. Input bias currents (I_{B1} and I_{B2}) would also be adversely affected.

The input resistance of the circuit of figure 11 is given by **(9)** remembering that in this case R_E must be replaced by r_{e2}

$$r_i = r_{be1} + (\beta_1 + 1)r_{e2} \qquad \textbf{(19)}$$

and if $I_{C1} \approx I_{C2}$ and $\beta_1 \approx \beta_2$, i.e., T_1 and T_2 are balanced and identical, $r_i \approx 2r_{be1}$.

The remaining stages are standard circuit shapes. The T_3 circuit is the standard common emitter circuit of figure 2. The base voltage is v_{o1} which was calculated (in terms of v_i) in the input section considerations that led to **(18)**. This means that $R_S = 0$ (because its effects were taken into account in the calculation of v_{o1}. The effective R_L is R_{VA} in parallel with r_{ce} of T_3, r_i of T_4 and r_i of T_5. In the circuit of figure 1, R_{VA} will be much smaller than r_{ce3}, r_{i4} and r_{i5} so the parallel combination $\approx R_{VA}$. The T_3 stage gain will thus be (from **(3)** with $R_S = 0$)

$$\frac{v_a}{v_{o1}} \approx - g_m R_{VA} \qquad \textbf{(20)}$$

The output stage, T_4 and T_5 are emitter follower circuits connected together in what is known as a double ended or push-pull arrangement. T_4 is an n-p-n transistor and is active during positive half cycles when current must flow from the positive power supply via T_4 to the load. T_5 is a p-n-p transistor and is active during negative half cycles when current flows from ground throught the load and T_5 to the negative supply. The emitter follower gain is very close to unity as shown by **(12)** and this leads to an overall amplifier gain

$$\frac{v_{o4}}{v_i} = \frac{v_{o4}}{v_a} \text{ x } \frac{v_a}{v_{o1}} \text{ x } \frac{v_{o1}}{v_i} = \frac{R_1 // r_{be3}}{r_{e1} + r_{e2}} g_m R_{VA} \qquad \textbf{(21)}$$

and for an amplifier circuit such as figure 1 this gain will be in the low thousands. A general purpose commercial op-amp will have a gain larger than this figure by a factor of two to three orders of magnitude. The next section looks at how the basic circuit of figure 1 can be refined to improve the gain and other parameters.

Refinements to the basic op-amp circuit of figure 1

Problems with the circuit of figure 1

Input stage

1 In the input stage, half the signal is wasted because the collector of T_2 is connected directly to the negative supply rail.

2 There is also a potential problem with collector current imbalance between T_1 and T_2 which will give rise to offset errors.

3 The input bias current is high and the input resistance is low in comparison with commercial general purpose op-amps.

4 The effective R_L of the first stage is relatively low leading to a very low gain.

T_3 stage

5 R_{VA} cannot have a large value because of the constraints imposed by dc conditions but a large value is desirable to maximise signal gain.

Output (T_4 and T_5) stage

6 the input resistance of T_4 and T_5 is dependent on the external op-amp load (effectively the R_E of the emitter follower of figure 6) and this has a direct bearing on voltage amplification stage gain.

7 The output resistance of the emitter follower is dependent on its source resistance.

8 The output transistors in figure 1 will give rise to severe crossover distortion. Crossover

distortion is distortion to the shape of the signal that occurs when conduction transfers from one output transistor to the other.

Solutions

Problems 1, 2, 3 and 4

Problems 1 and 2 are usually solved by introducing a circuit called a current mirror to form an active load for T_1 and T_2. There is a number of different current mirror circuits that have been devised but the one shown in figure 12 is the simplest and therefore the easiest to understand. The more complicated ones were devised to correct deficiencies in the basic circuit of figure 12. We will first look at the behaviour of current mirrors before looking at the current mirror - differential pair combination.

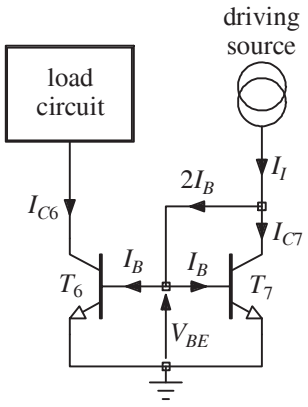


Figure 12
A current mirror circuit

T_6 and T_7 are assumed to be identical. The aim of the circuit is to draw from the load circuit the same current that is being driven into T_7 by the driving source. In other words, The circuit will ideally make $I_{C6} = I_I$. Notice that the collector and base of T_7 have been connected together and that the bases of the two transistors are connected together, as are the emitters. Thus V_{BE} will be the same for each transistor. I_I will set up a V_{BE} that is sufficient to make T_7 conduct a collector current $I_{C7} = I_I - 2I_B$.

$$I_I = I_{C7} + 2I_B = I_{C7}\left(1 + \frac{2}{h_{FE}}\right) \text{ or } I_{C7} = I_I \frac{h_{FE}}{2 + h_{FE}} \qquad \textbf{(22)}$$

Since V_{BE} is the same for both transistors, $I_{C6} = I_{C7}$ so **(22)** describes the relationship between input and mirrored current-s. Even with identical transistors the accuracy of the mirroring evidently depends upon the magnitude of h_{FE}. Note that in reality there will also be an error due to mismatch between the transistors but we will not pursue that error further here.

[The effect of finite h_{FE} can be reduced by adding a third transistor as shown in figure 13. This is sometimes called an h_{FE} helper transistor (or in some circles a β helper transistor). If we assume that all three transistors have the same h_{FE},

$$I_{BH} = \frac{2I_B}{h_{FE}} \text{ so } I_I = I_{C7} + I_{BH} = I_{C7} + \frac{2I_B}{h_{FE}} = I_{C7}\left(\frac{h_{FE}^2 + 2}{h_{FE}^2}\right), \qquad \textbf{(23)}$$

a much smaller error than that described by **(22)**.]

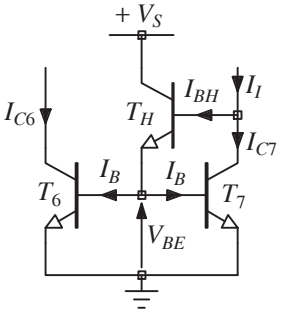


Figure 13
The current mirror of figure 12 with a helper transistor

The small-signal behaviour of the circuit of figure 12 is almost the same as the dc behaviour described by **(22)**. The differences are that for small-signal, h_{FE} is replaced by β and r_{ce}, the small signal resistance between collector and emitter, of T_7 will conduct a very small fraction of i_i, the small-signal equivalent of I_I, to ground. We will ignore this small loss of current. As far as the load is concerned T_6 looks like a current source in parallel with r_{ce6}.

Figure 14 shows the circuit diagram of the improved input stage circuit. The voltage amplification stage has been included because it has a significant effect on first stage gain. The

main cause of imbalance between I_{C1} and I_{C2} in figure 1 is the relatively high value of I_{B3}. In figure 14 T_8 is added to reduce this current which becomes I_{B8}. The combination of T_8 and T_3 is called a "Darlington pair". Most of I_3 flows through T_3 so $I_{B3} = I_3/h_{FE3}$ as before. I_{B3} forms the emitter current of T_8 so $I_{B8} \approx I_{B3}/h_{FE8}$. If the h_{FE}s of T_3 and T_8 are of the order of hundreds, the addition of T_8 reduces the bias current requirement of the voltage amplification stage by at least two orders of magnitude and I_{C1} is much closer to I_{C2} as a result.

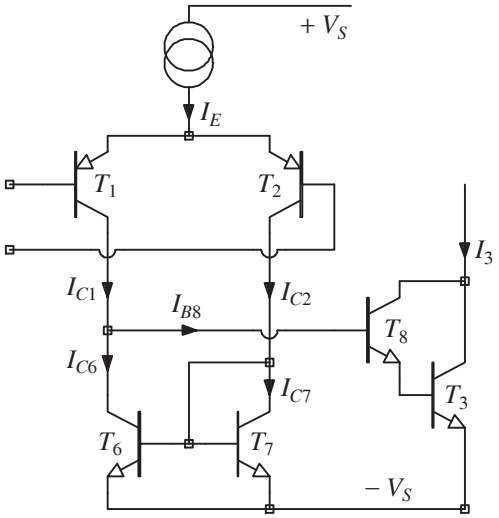


Figure 14
An improved input stage incorporating a current mirror and a Darlington pair

The Darlington pair of T_8 and T_3 also increases the input resistance of the voltage amplification stage. T_8 is an emitter follower connection with an effective R_E equal to the input resistance of T_3, r_{be3}. **(13)** gives the input resistance of an emitter follower and if the terms are modified for the circuit of figure 14, the input resistance looking into the base of T_8 is

$$r_{i8} = r_{be8} + (\beta_8 + 1)r_{be3} \qquad \textbf{(24)}$$

If the small-signal current gain of T_8 is in the hundreds, r_{i8} will be at least two orders of magnitude bigger than r_{be3}.

The addition of T_8 therefore helps to alleviate problems 2 and 3 and contributes to alleviating problem 4.

The current mirror also plays an important role in the input stage bias current balance and is also important from a signal point of view because the mirroring action works on ss changes as well as the static dc conditions. Consider the behaviour of the circuit of figure 14 when the voltage between the bases of T_1 and T_2 is zero. I_E splits between T_1 and T_2 to give collector currents of I_{C1} and I_{C2} respectively. The current I_{C2} instead of being returned directly to the negative supply as it is in figure 10 is now mirrored such that $I_{C6} \approx I_{C2}$. Assuming that the mirror is perfect, i.e, that $I_{C2} = I_{C6}$, a current sum at the collector node of T_1 gives

$$I_{C1} - I_{C6} = I_{C1} - I_{C2} = I_{B8} \qquad \textbf{(25)}$$

and assuming negligible base currents in T_1 and T_2

$$I_{C1} + I_{C2} = I_E \qquad \textbf{(26)}$$

Adding **(25)** and **(26)** gives

$$I_{C1} = \frac{I_E}{2} + \frac{I_{B8}}{2} \qquad \textbf{(27)}$$

and subtracting **(26)** from **(25)** gives

$$I_{C2} = \frac{I_E}{2} - \frac{I_{B8}}{2} \qquad \textbf{(28)}$$

Thus the collector currents of T_1 and T_2 are as balanced as they can be and if I_{B8} is small compared to I_{C1} and I_{C2} the mirror maintains an excellent balance.

When a signal is present at the input the split of I_E between T_1 and T_2 is modulated by the signal. Consider an instant when $V_{BT1} > V_{BT2}$. This will set up the conditions such that ΔI is taken from I_{C1} and added to I_{C2} to give

$$I_{C1} \rightarrow I_{C1} - \Delta I \quad \textbf{(29)}$$

$$I_{C2} \rightarrow I_{C2} + \Delta I \quad \textbf{(30)}$$

Using the I_{C1} and I_{C2} in **(27)** and **(28)** with the added current modulation of **(29)** and **(30)**, the modulated I_{B8} can be found by subtracting I_{C6} ($= I_{C2}$) from I_{C1}

$$I_{C1} - I_{C6} = \frac{I_E}{2} + \frac{I_{B8}}{2} - \Delta I - \frac{I_E}{2} + \frac{I_{B8}}{2} - \Delta I = I_{B8} - 2\Delta I \quad \textbf{(31)}$$

The mirror circuit has transferred all the collector current modulation in the differential input pair into a modulated I_{B8}. In addition, the effective load resistance seen by this node is a parallel combination of r_{i8} , r_{ce1} and r_{ce6}. r_{i8} has been shown to be large in **(24)** and r_{ce1} and r_{ce6} are intrinsically large. Together, the improvements offered by T_8 and the mirror improve the gain of the input stage by a factor of between 20 and 50 when compared with the circuit of figure 1. The inclusion of the mirror has contributed to problems 1, 2 and 4.

Problems 5 and 6

Problems 5 and 6 are related in the effect they have on the voltage amplification stage. The common emitter transistor, T_3, has a gain that is directly proportional both to its transconductance and to the load resistance seen between the collector node of T_3 and ground. In figure 1 this resistance consists of three main components:

- the collector emitter resistance of T_3, r_{ce3},
- the resistor R_{VA} and
- the input resistance of T_4 and T_5

The first of these is large and is difficult (though not impossible) to make larger. The second, R_{VA} is the most serious problem. The value of R_{VA} is determined by the dc condition requirements of the voltage amplification stage and this limits its value to a few 10s of kΩ. The difficulty is usually overcome by replacing R_{VA} by a current source, a strategy that raises the effective value of R_{VA} to the output resistance of the current source which usually approximates to the r_{ce} of the current source transistor. (The tail resistor, R_E, of the differential pair is also usually replaced by a current source so that I_E is largely independent of common mode input voltage.) The input resistance of T_4 and T_5 is affected by the external load connected to the op-amp and this tends to make overall gain a function of external load. This effect can be significantly reduced by the inclusion of an extra transistor, T_9, which is an emitter follower forming a Darlington connected pair with whichever of T_4 or T_5 is conducting. These modifications can be seen in figure 15. The input resistance of T_9 can be estimated by repeated use of **(13)** so assuming that T_4 is conducting its input resistance will be

$$r_{i4} = r_{be4} + (\beta_4 + 1)R_{L\,EXT} \quad \textbf{(32)}$$

where $R_{L\,EXT}$ is the op-amp's external load resistance. The input resistance of T_9 is then

$$r_{i9} = r_{be9} + (\beta_9 + 1)r_{i4} \quad \textbf{(33)}$$

The inclusion of the current souce load and T_9 will increase the voltage stage gain by at least an order of magnitude.

Problems 7 and 8

The problem caused by the input resistance that T_4 presented to the collector node of T_3 is also a problem from an output resistance point of view. If the output resistance of the emitter follower connected transistor of figure 6 is worked out, the result is

$$r_o = \frac{r_{be}}{\beta} + \frac{R_S}{\beta} = r_e + \frac{R_S}{\beta} \qquad \textbf{(34)}$$

Without T_9, the R_S for T_4 is the collector load for T_3 which has been made as large as possible to maximise gain. This would increase the output resistance of the amplifier. Including T_9 serves two purposes - it allows the input resistance of the output stage (T_9, T_4 and T_5) to be large and the output resistance of the output stage to be small thus simultaneously solving problems 6 and 7.

Problem 8 arises because T_4 will not start conducting until its base voltage ≈ 0.7 V and T_5 will not start conducting until its base voltage falls to ≈ -0.7 V. In figure 1 where the bases of T_4 and T_5 are connected together this leaves a region of signal between -0.7V and $+0.7$ V that is permanently lost. This problem is usually dealt with by the components R_9, R_{10} and T_{10} that have been added to figure 15. The effect of this circuit is to insert a fixed voltage source of 1.4 V between the bases of T_4 and T_5 so that when, for a rising signal, T_5 is about to stop conducting ($V_{B5} = -0.7$ V and $V_O = 0$V, T_4 is ready to take over conduction because at that point $V_{B4} = 0.7$ V. The R_9, R_{10}, T_{10} combination is maintained in a conducting state by I_4 which must be a few times larger than the peak current demanded by the base of T_5. The current through R_{10} can be worked out because there is 0.7 V across it. If the base current of T_{10} is negligible, the same current flows through R_9 so the voltage across the combination can be estimated.

Figure 15 shows the improved version of figure 1. The current sources I_{S1}, I_{S2} and I_{S3} exist to set up dc conditions by defining currents and this approach has the advantages described earlier. These current sources would normally be in the form of connected current mirrors with circuitry modified to allow the creation of well defined current ratios between the various sources. I_{S1} would typically be in a range 10 to 50 μA, I_{S2} in the range 100 to 200 μA and I_{S3} would be typically 1 to 5 mA.

The overall differential mode gain of figure 15 will be between two and three orders of magnitude larger than that of figure 1.

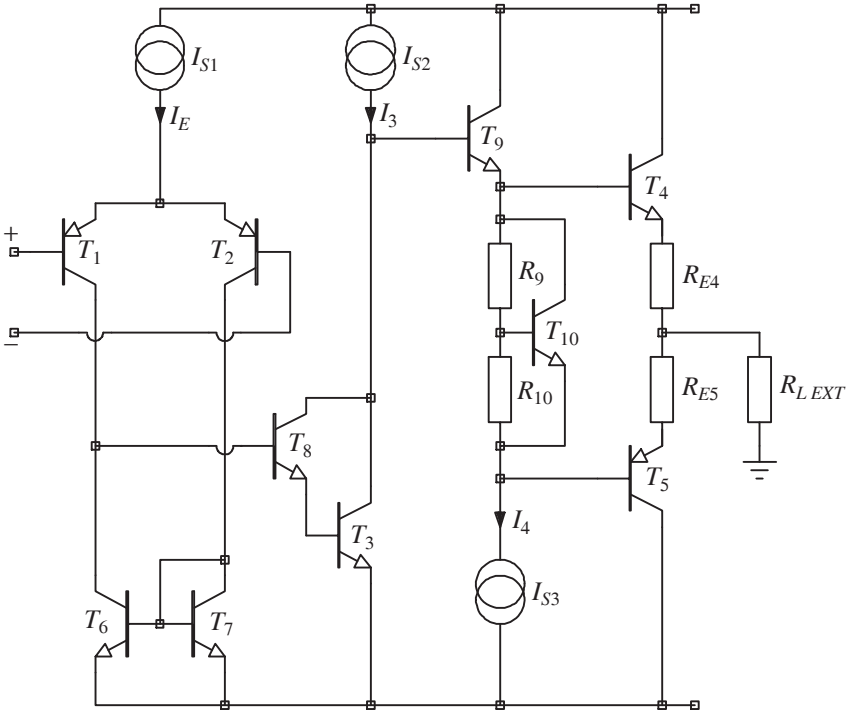


Figure 15

The circuit of figure 1 with improvements added. These improvements will increase the circuit gain be between two and three orders of magnitude

First Order Circuits

1 Introduction

There are two forms of first order frequency response, low-pass and high-pass. There is also a third hybrid form which is a linear sum of the low-pass and high-pass cases; this is not really a separate type of response in its own right. The terms high-pass and low-pass relate to the way the circuit gain changes as frequency is varied. A low-pass circuit tends to pass frequencies below a critical value but attenuates increasingly as frequency exceeds this critical value. The high-pass circuit, on the other hand, passes frequencies above some critical value and attenuates increasingly as frequency falls below this critical value. The critical value is usually called the **corner frequency** or the **3dB frequency**. In working out transfer functions it is important to keep j and ω together and replacing $j\omega$ with s is a convenient way of achieving this objective. s is actually the Laplace complex frequency variable which reduces to $j\omega$ for steady state frequency response considerations.

The two forms of first order response can be represented by standard forms and although the hybrid form is a sum of low-pass and high-pass, it is usually convenient to treat it as a third standard form. All first order circuits can be interpreted by forcing their transfer functions into the shape of a standard form and then extracting the relevant parameters by inspection.

2 First order standard forms

A general transfer function will have a **denominator** of the form $a_0 + a_1 s + a_2 s^2 + a_3 s^3 + \ldots$. A transfer function is first order if only the a_0 and $a_1 s$ terms exist. From a frequency response point of view, $s \Rightarrow j\omega$.

The two basic forms of first order transfer function are;

The low-pass
$$\frac{v_o}{v_i} = k \cdot \frac{1}{1 + s\tau} = k \cdot \frac{1}{1 + j\dfrac{\omega}{\omega_o}} = k \cdot \frac{1}{1 + j\dfrac{f}{f_o}} \qquad \textbf{(2.1)}$$

The high-pass
$$\frac{v_o}{v_i} = k \cdot \frac{s\tau}{1 + s\tau} = k \cdot \frac{j\dfrac{\omega}{\omega_o}}{1 + j\dfrac{\omega}{\omega_o}} = k \cdot \frac{j\dfrac{f}{f_o}}{1 + j\dfrac{f}{f_o}} \qquad \textbf{(2.2)}$$

The third form, which is a linear sum of **(2.1)** and **(2.2)**, is often called a "pole-zero" or "lead lag" function.

$$\frac{v_o}{v_i} = k \cdot \frac{1 + s\tau_1}{1 + s\tau_2} = k \cdot \frac{1 + j\dfrac{\omega}{\omega_1}}{1 + j\dfrac{\omega}{\omega_2}} = k \cdot \frac{1 + j\dfrac{f}{f_1}}{1 + j\dfrac{f}{f_2}} \qquad \textbf{(2.3)}$$

The key points about these standard forms are

(i) The denominator is always complex

(ii) Whatever multiplies $j\omega$ **in the denominator** is the system time constant. In frequency domain expressions it is very common to see time constant expressed in terms of a frequency domain constant as in **(2.1)**, **(2.2)** and **(2.3)**.

(ii) The denominator has a real part of unity in all cases.

(iii) The numerator may be real (constant) as in **(2.1)**, imaginary as in **(2.2)** or complex as in **(2.3)**.

(iv) Where the numerator is purely imaginary, the coeficcient of $j\omega$ in the top line should be made to be the same as that of the imaginary part of the denomiator.

(v) Where the numerator is complex, its real part should be forced to unity.

(vi) The form of the numerator indicates the type of first order response -

purely real	$\Rightarrow$	low-pass (or simple integrator)
purely imaginary	$\Rightarrow$	high-pass (or simple differentiator)
complex	$\Rightarrow$	"pole-zero" or "lead-lag" circuit - a linear sum of low-pass and high-pass, each with different k.

3 Getting the transfer function

The transfer function will often be a suitably manipulated potential divider relationship. In order to end up with a result that is easily interpretable, it is desirable to express the transfer function in a particular way. An outline of the steps necessary is as follows with the circuit of figure 1 used as an example.

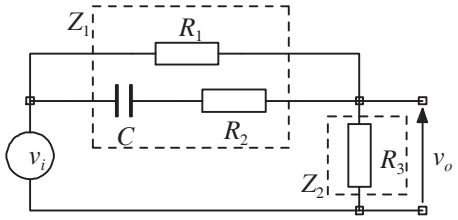


Figure 1

An example first order RC circuit

(i) Work out the impedances Z_1 and Z_2 remembering to keep $(j\omega)$ together. For figure 1 and using s for $j\omega$ they are

$$Z_1 = R_1 \,//\, (R_2 + X_C)$$

$$= \frac{R_1\left(R_2 + \dfrac{1}{sC}\right)}{R_1 + R_2 + \dfrac{1}{sC}} = \frac{R_1(1 + sCR_2)}{1 + sC(R_1 + R_2)} \qquad \textbf{(3.1)}$$

$$Z_2 = R_3 \qquad \textbf{(3.2)}$$

(ii) Write down the potential division relationship. For the circuit of figure 1 it is

$$\frac{v_o}{v_i} = \frac{Z_2}{Z_2 + Z_1} = \frac{R_3}{R_3 + \dfrac{R_1\,(1 + sCR_2)}{1 + sC\,(R_1 + R_2)}} \qquad \textbf{(3.3)}$$

(iii) Manipulate the potential division relationship to end up with a ratio of two polynomials in s. Note that in general the numerator polynomial may be completely real, completely imaginary or complex; the denominator will be complex with a real and an s term. For the circuit of figure 1,

$$\frac{v_o}{v_i} = \frac{R_3\,(1 + sC\,(R_1 + R_2))}{R_3\,(1 + sC\,(R_1 + R_2)) + R_1\,(1 + sCR_2)}$$

$$= \frac{R_3\,(1 + sC\,(R_1 + R_2))}{R_3 + R_1 + sC\,(R_1R_3 + R_2R_3 + R_1R_2)} \qquad \textbf{(3.4)}$$

(iv) Take out factors to force the real parts of the numerator and denominator to unity. This will often result in having to divide the s term in the denominator by the real part of the denominator. The numerator often naturally occurs in the right form (as in this example). For the circuit of figure 1 R_3 is obviously a factor in the numerator. $(R_1 + R_3)$ is the factor that must be removed from the denominator to give a denominator real part of unity. These two factors form a dimensionless frequency independent ratio that multiplies the complex part of the expression.

$$\frac{v_o}{v_i} = \frac{R_3}{R_1 + R_3} \cdot \frac{1 + sC\,(R_1 + R_2)}{1 + sC\,\dfrac{R_1R_2 + R_2R_3 + R_1R_3}{R_1 + R_3}} \qquad \textbf{(3.5)}$$

At each stage of this process you should get into the habit of checking that your equations are dimensionally consistent. It is easy to check dimensions and although dimensional checks will not reveal all errors, they will reveal a significant number.

4 Interpreting the transfer function

Having obtained the transfer function and manipulated it so that it has the shape of a standard form, the next step is to compare the transfer function with the standard form of the same type. Again, using the circuit of figure 1 as an example and comparing **(3.5)** with **(2.1)**, **(2.2)** and **(2.3)**, it is clear that **(3.5)** is of the form of **(2.3)** - the hybrid form - and by comparison of coefficients,

$$k = \frac{R_3}{R_1 + R_3}\,,\ \omega_1 = \frac{1}{C\,(R_1 + R_2)} \text{ and } \omega_2 = \frac{R_1 + R_3}{C\,(R_1R_2 + R_1R_3 + R_2R_3)} \qquad \textbf{(4.1)}$$

Knowledge of these three parameters and the the type of response ((2.1), (2.2), or (2.3)) specifies the shape of the amplitude and phase responses of the circuit as shown in section 5. It is also possible to use the transfer function to identify system gain as frequency approaches very low or very high values - the low frequency gain and the high frequency gain. To do this one must consider how the modulus of the transfer function behaves as frequency becomes very small or very large. Taking the hybrid standard form of **(2.3)**,

$$\left|\frac{v_o}{v_i}\right| = k\,.\left|\frac{1 + j\dfrac{\omega}{\omega_1}}{1 + j\dfrac{\omega}{\omega_2}}\right| = k\,.\left(\frac{1 + \dfrac{\omega^2}{\omega_1^2}}{1 + \dfrac{\omega^2}{\omega_2^2}}\right)^{\frac{1}{2}} \qquad \textbf{(4.2)}$$

At low frequencies, $\omega << \omega_1$ and $\omega << \omega_2$ so both $\dfrac{\omega^2}{\omega_1^2}$ and $\dfrac{\omega^2}{\omega_2^2}$ are $<< 1$ and $\left|\dfrac{v_o}{v_i}\right| \approx k\,.$ **(4.3)**

At high frequencies, $\omega >> \omega_1$ and $\omega >> \omega_2$ so both $\dfrac{\omega^2}{\omega_1^2}$ and $\dfrac{\omega^2}{\omega_2^2}$ are $>> 1$ and $\left|\dfrac{v_o}{v_i}\right| \approx k\ \dfrac{\omega_2}{\omega_1}.$ **(4.4)**

5 Response shapes

There are three response shapes that correspond to the three standard forms of **(2.1)**, **(2.2)** and **(2.3)**. **All** first order transfer functions will fall into one of these three categories. Amplitude responses are usually plotted with gain in dB; phase is usually plotted on a linear scale. Both amplitude and phase are usually plotted with a logarithmic frequency axis.

5.1 Low-Pass

(a) Amplitude response

The low-pass amplitude response shape can be worked out by considering the modulus of **(2.1)** for frequencies well below, well above and in the region of, ω_0.

$$\left|\frac{v_o}{v_i}\right| = k\,.\,\left|\frac{1}{1+j\dfrac{\omega}{\omega_0}}\right| = k\,.\left(\frac{1}{1+\dfrac{\omega^2}{\omega_0^2}}\right)^{\frac{1}{2}}$$

(i) $\omega << \omega_0$

Under this condition $\dfrac{\omega^2}{\omega_0^2}$ is much smaller than unity so $\left|\dfrac{v_o}{v_i}\right| \approx k\,.$ $(\equiv 20\log k$ dB)

(ii) $\omega = \omega_0$

Under this condition $\dfrac{\omega^2}{\omega_0^2} = 1$ so $\left|\dfrac{v_o}{v_i}\right| \approx \dfrac{k}{\sqrt{2}}\,.$ $(\equiv 20\log k$ dB $- 3$dB)

(iii) $\omega >> \omega_0$

Under this condition $\dfrac{\omega^2}{\omega_0^2}$ is much larger than unity so $\left|\dfrac{v_o}{v_i}\right| \approx k\,\dfrac{\omega_0}{\omega}$. Thus the circuit gain is inversely proportional to frequency; if ω increases by a factor of 10, gain decreases by a factor of 10. A factor of 10 reduction in gain is a reduction of 20 dB so the slope of the amplitude response in this frequency region will approach −20dB for every decade increase in frequency.

A good approximation to the amplitude response (known as the Bode approximation) draws the response as two straight lines - a horizontal line at the low frequency gain from 0Hz to ω_0 and a -20dB per decade line from ω_0 upwards. The low-pass amplitude response is shown in figure 2.

(b) Phase response

The phase of the low-pass response of **(2.1)** is calculated from $\varphi = -\tan^{-1}\dfrac{\omega}{\omega_0}$ and as in the amplitude case, its shape can be deduced by considering three frequency conditions,

(i) $\omega << \omega_0$

Under this condition, as $\omega \Rightarrow 0$, $\varphi \Rightarrow 0^o$.

(ii) $\omega = \omega_0$

Under this condition, $\varphi = -\tan^{-1}\dfrac{\omega}{\omega_0} = -\tan^{-1} 1 = -45^o$

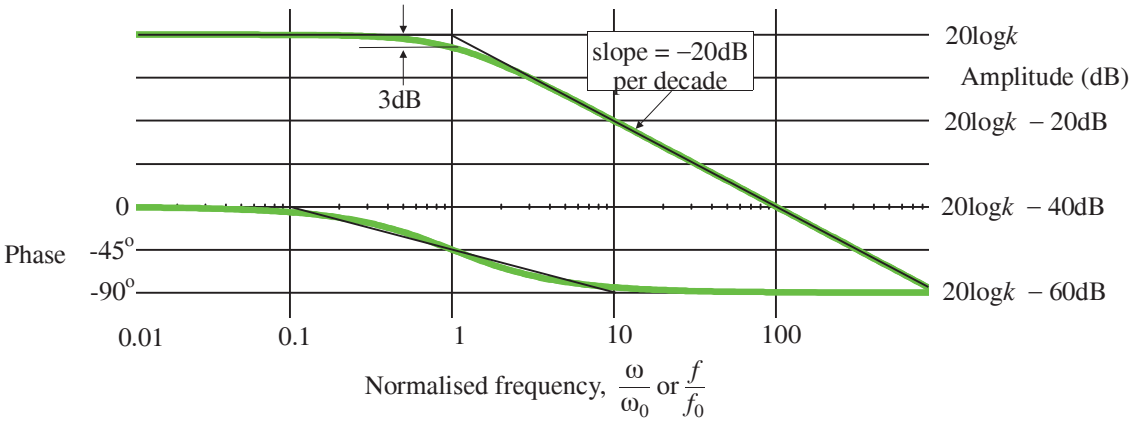
(iii) $\omega >> \omega_0$

Under this condition, $\varphi = -\tan^{-1}\dfrac{\omega}{\omega_0} \Rightarrow -\tan^{-1}[\text{a large number}] \Rightarrow -90^{\circ}$

The Bode approximation for the phase response is a straight line starting from 0° at $\omega = 0.1\omega_0$, going through -45° at $\omega = \omega_0$ and reaching -90° at $\omega = 10\ \omega_0$. Its slope is therefore -45° per decade. The phase response is shown in figure 2.

Figure 2

Low-pass amplitude and phase response



5.2 High-Pass

(a) Amplitude response

The high-pass transfer function of **(2.2)** has a magnitude response that is a mirror image of the low-pass response about the vertical line $\omega/\omega_0 = 1$. The response plot for high-pass function can be written as

$$20\log\left|\frac{v_o}{v_i}\right| = 20\log\left(k\,.\left|\frac{j\dfrac{\omega}{\omega_0}}{1+j\dfrac{\omega}{\omega_0}}\right|\right) = 20\log k + 20\log\left|j\frac{\omega}{\omega_0}\right| + 20\log\left|\frac{1}{1+j\dfrac{\omega}{\omega_0}}\right|$$

and this makes it clear that on a logarithmic amplitude plot, the response consists of a sum of three components.

$20\log k$ is a constant.

$20\log\left|j\dfrac{\omega}{\omega_0}\right|$ is a straight line with a slope of +20 dB per decade that goes through 0 dB when $\omega = \omega_0$

$20\log\left|\dfrac{1}{1+j\dfrac{\omega}{\omega_0}}\right|$ is the low pass response shape, without the k, considered in section 5.1.

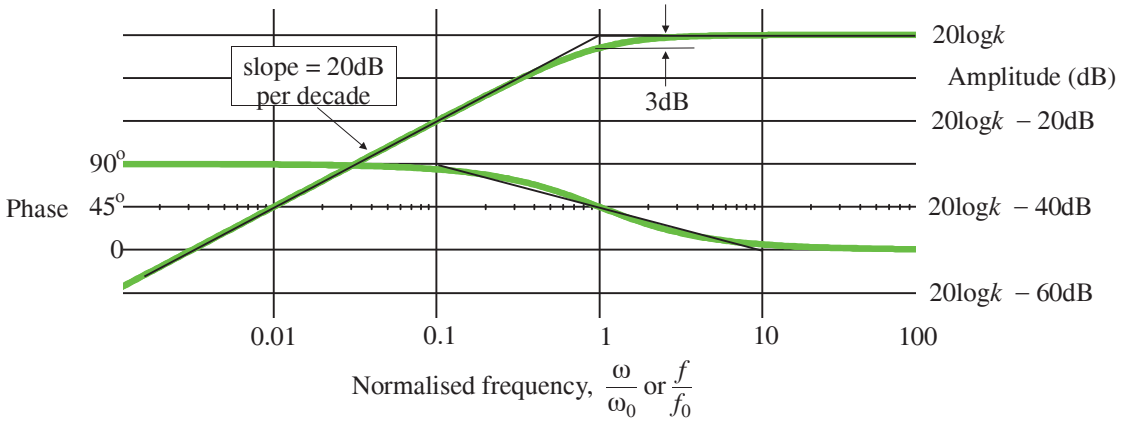
The high-pass amplitude response is shown in figure 3.

(b) Phase response

The phase response of the high-pass function is the same shape as that of the low-pass function but at all frequencies the high-pass phase is 90° higher than the low-pass phase. The difference arises because there is a j term but no real term in the numerator and that j term acts as a 90° phase shift operator. The phase response of the high-pass function is shown in figure 3.

Figure 3

High- pass amplitude and phase response



5.3 Pole-Zero or Lead-Lag

(a) Amplitude response

Using the same approach as in section 5.2, the log of the modulus of **(2.3)** can be expressed as the sum of simpler logarithmic components

$$20\log\left|\frac{v_o}{v_i}\right| = 20\log\left(k\,.\left|\frac{1+j\dfrac{\omega}{\omega_1}}{1+j\dfrac{\omega}{\omega_2}}\right|\right) \text{ or}$$

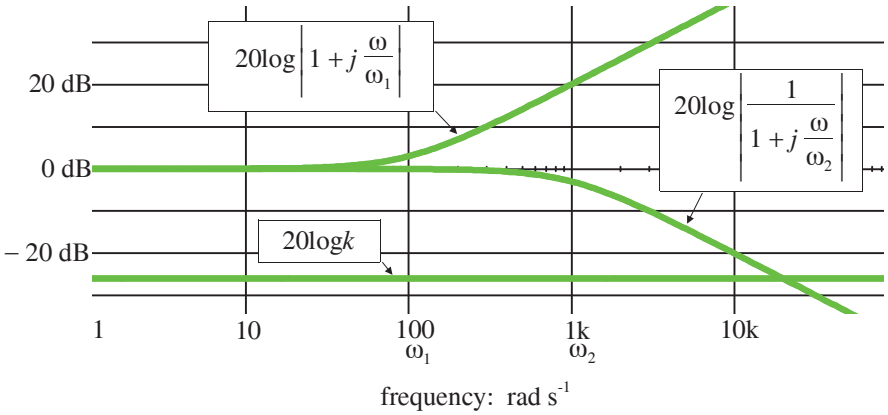
$$20\log\left|\frac{v_o}{v_i}\right| = 20\log k + 20\log\left|1+j\frac{\omega}{\omega_1}\right| + 20\log\left|\frac{1}{1+j\dfrac{\omega}{\omega_2}}\right| \qquad \textbf{(5.1)}$$

The only new part here is the second term. Since $20\log\left|1+j\dfrac{\omega}{\omega_1}\right| = -20\log\left|\dfrac{1}{1+j\dfrac{\omega}{\omega_1}}\right|$, the response of the second term is the inverse of the first order low pass response of section 5.1. In other words for the second term, the gain is 0 dB at 0 Hz, rises to + 3 dB at $\omega = \omega_1$ and rises at 20 dB per decade for frequencies greater than ω_1.

If $\omega_1 < \omega_2$, the overall gain rises as frequency increases between ω_1 and ω_2 before flattening off when $\omega > \omega_2$. If $\omega_1 > \omega_2$, the overall gain falls as frequency increases between ω_2 and ω_1 before flattening off when $\omega > \omega_1$. Figure 4a shows the gain components of **(5.1)** and figure 4c shows the overall sum of those components, together with the overall phase response.

Figure 4a

The three log magnitude components of ***(5.1)****. In this example,* ω_1 *is 100 rad* s^{-1} *and* ω_2 *is 1000 rad* s^{-1}*.*



(b) Phase response

For a function such as **(2.3)** the phase is given by

$$\varphi = \tan^{-1}\frac{\omega}{\omega_1} - \tan^{-1}\frac{\omega}{\omega_2} \qquad \textbf{(5.2)}$$

There is no phase shift associated with the constant k. Both parts of the phase expression have a phase that approaches 0^o at low frequencies and approaches 90^o for high frequencies. Since the two subtract, the high frequency phase shift will also be zero. In the region of ω_1 and ω_2, the phase will be a positive going or negative going hump depending upon whether $\omega_1 < \omega_2$ or vice versa. Figure 4b shows the contribution to phase made by each of the components of **(5.2)** and figure 4c shows the sum of these components.

Figure 4b

The three phase components of ***(5.2)****. In this example,* ω_1 *is 100 rad* s^{-1} *and* ω_2 *is 1000 rad* s^{-1}*.*

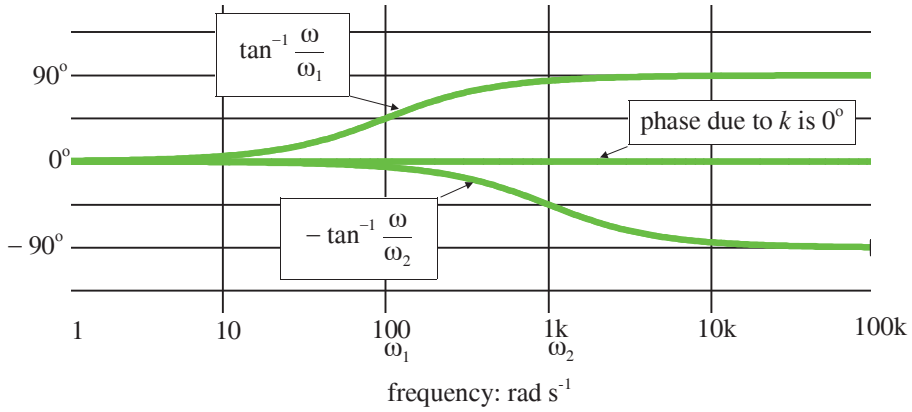
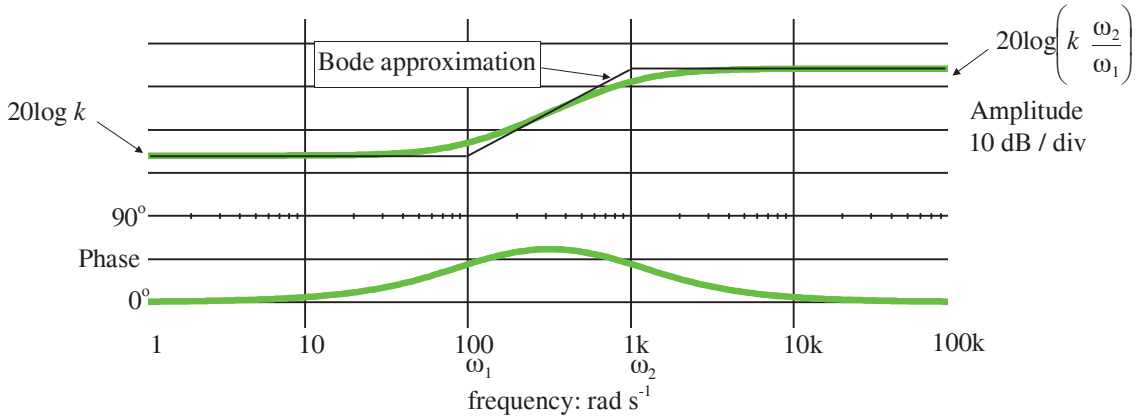


Figure 4c

Overall response of a pole-zero circuit such as ***(2.3)*** *with* $\omega_1 = 100$ *rad* s^{-1} *and* $\omega_2 = 1000$ *rad* s^{-1}. *The amplitude response is the sum of the components of shown in figure 4a and the phase response is the sum of the components shown in figure 4b.*



Note that in general ω_1 can be smaller than or larger than ω_2. The response shown here is for ω_1 smaller than ω_2. If ω_2 had been smaller than ω_1, gain and phase would have started falling because of the effects of ω_2 before they flattened out because of the effects of ω_1. The phase response would then be a downwards going hump and the amplitude response would have a higher value at low frequencies than at high frequencies.

For the circuit of figure 1, ω_1 is lower than ω_2 for all possible component value combinations.

6 Checking by inspection

It is quite easy to identify high frequency gain, low frequency gain and time constant by inspection. Identifying these parameters is a useful check on the accuracy of your algebraic manipulations; if the time constant is different depending on how you calculated it, there is an error somewhere. The following section outlines the steps in the checking process using the circuit of figure 1 as an example.

(i) Low frequency (l.f.) gain

The low frequency gain is the gain that is approached as $f \Rightarrow 0$. To work it out, replace capacitors with a very high impedance. Capacitors then dominate the impedance of series *RC* combinations but are of negligible effect in parallel *RC* combinations. In most cases the capacitors are simply removed from the circuit. Thus the low frequency equivalent circuit of figure 1 is given in figure 5 and the gain is easily written down as

$$\frac{v_o}{v_i} = \frac{R_3}{R_1 + R_3}$$

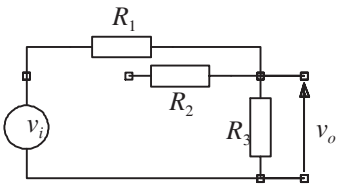


Figure 5

The low-frequency equivalent circuit of figure 1. Note that C has been replaced by an open circuit.

(ii) High frequency (h.f.) gain

The high frequency gain is the gain that is approached as $f \Rightarrow \infty$. In this case capacitors have a very low reactance so the impedance of series *RC* combinations is dominated by *R* and that of parallel combinations is dominated by *C*. The high frequency equivalent circuit of figure 1 is

shown in figure 6. Again, the gain can be easily written down as

$$\frac{v_o}{v_i} = \frac{R_3}{R_1 // R_2 + R_3} = \frac{R_3\,(R_1 + R_2)}{R_1R_2 + R_1R_3 + R_2R_3}$$

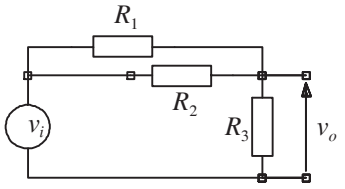


Figure 6

A high frequency equivalent circuit of figure 1. Note that C has been replaced by a short circuit.

(iii) Time constant

To identify the system time constant one must look at the circuit from the capacitor's point of view. First replace all sources by their Thevenin equivalent impedances - 0Ω for a voltage source and ∞Ω for a current source. Then imagine that you can inject some charge into the capacitor and ask yourself what is the resistance of the discharge path. C multiplied by the discharge path resistance is the system time constant and this should be the same as the coefficient of $j\omega$ in the denominator of the transfer function.

Figure 7 shows figure 1 with v_i replaced by a short circuit. Charge in C must flow through R_2. After passing through R_2, the current is faced with R_1 and R_3 in parallel giving a time constant

$$\tau = C\,(R_2 + R_1 // R_3) = C\,\frac{R_1R_2 + R_1R_3 + R_2R_3}{R_1 + R_3}$$

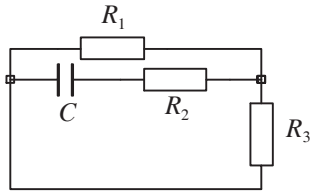


Figure 7

Equivalent circuit of figure 1 for identifying time constant

7 Step response

A step input is an instantaneous change in input voltage from one voltage to another. The instant at which the change occurs is usually taken as $t = 0$ although it doesn't have to be there. A unit step input is a change from 0V to 1V.

Step inputs are very useful test signals because many circuit applications deal with signals that change state suddenly from one value to another. The step response of a circuit, ie the output that arises as a result of a step at the input is therefore a useful response to be able to predict.

For first order circuits, the step response will in general consist of a step followed by an exponential. The magnitude of the step can be calcuated from the gain terms and the exponential can be written

$$V(t) = (V_{START} - V_{FINISH})\,e^{-t/\tau} + V_{FINISH} \qquad \textbf{(7.1)}$$

The numbers needed to define V_{START}, V_{FINISH} and τ can be found from the input step magnitude, the low frequency ($f \Rightarrow 0$) gain, the high frequency ($f \Rightarrow \infty$) gain and the system time constant - all these can be found by inspection as described in section 6 and they apply here as follows.

- The high frequency gain operates on the instantaneous step
- The low frequency gain operates on the dc voltage that exists before the step occurs - this is often 0V - and defines the voltage that will be reached as $t \Rightarrow \infty$

As an example, consider the circuit of figure 1, redrawn for convenience as figure 8 with component values added and a step input going from –2 V to + 8 V at $t = 0$.

The low frequency gain of the circuit is

$$A_{LF} = \frac{1\text{k}\Omega}{1\text{k}\Omega + 10\text{k}\Omega} = 90.9\text{x}10^{-3}$$

This defines the voltage from which any step on the output begins - in this case it is

$$-2\text{V}\text{x}90.9\text{x}10^{-3} = -0.18\text{V}$$

and also the voltage aimed for as $t \Rightarrow \infty$ which is

$$8\text{V}\text{x}90.9\text{x}10^{-3} = 0.73\text{V}$$

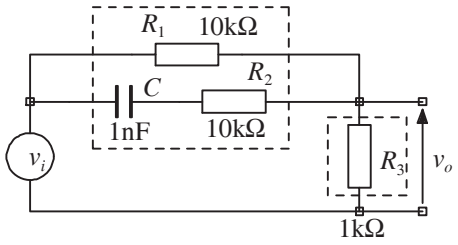


Figure 8

The first order RC circuit of figure 1 with values added. v_i is a step defined by $v_i = -2V$ for $t < 0$ and $v_i = 8V$ for $t > 0$

The high frequency gain of the circuit is

$$A_{HF} = \frac{1\text{k}\Omega}{10\text{k}\Omega//10\text{k}\Omega + 1\text{k}\Omega} = 0.167$$

and this, when multiplied by the height of the input step defines the height of the output step as

$$0.167\text{x}(8\text{V} - (-2\text{V})) = 1.67\text{V}$$

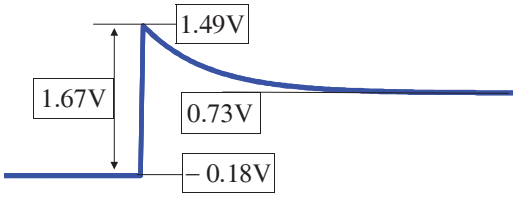


Figure 9

The step response associated with figure 8

The overall response is shown in figure 9 with the key voltages labelled. The exponential decay has $V_{START} = 1.49\text{V}$, $V_{FINISH} = 0.73\text{V}$ and $\tau = 10.9\mu\text{s}$ so using **(7.1)**, the exponential part of the response is $V(t) = (1.49 - 0.73)\, e^{-t/10.9\text{x}10^{-6}} + 0.73$.

8 An example

Identify the behaviour of the circuit of figure 10.

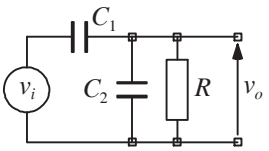


Figure 10

An example circuit

(i) By inspection

At low frequency the reactance of C_1 is much larger than the impedance of the C_2R combination so in the limit of $f \Rightarrow 0$, l.f. gain = 0

At high frequency the reactances of both capacitors are small compared with R and C_2 dominates the C_2R combination. As $f \Rightarrow \infty$, the gain is determined by the capacitive potential division between C_1 and C_2 so h.f. gain is

$$\frac{\dfrac{1}{j\omega C_2}}{\dfrac{1}{j\omega C_1} + \dfrac{1}{j\omega C_2}} = \frac{C_1}{C_1 + C_2} \qquad \textbf{(8.1)}$$

The time constant will be $R(C_1 // C_2)$ which is $R\,(C_1 + C_2)$ **(8.2)**

(ii) By analysis

The transfer function is a potential division between C_1 and the parallel combination C_2R.

$$\frac{v_o}{v_i} = \frac{\dfrac{\dfrac{R}{j\omega C_2}}{R + \dfrac{1}{j\omega C_2}}}{\dfrac{1}{j\omega C_1} + \dfrac{\dfrac{R}{j\omega C_2}}{R + \dfrac{1}{j\omega C_2}}} = \frac{\dfrac{R}{1 + j\omega C_2 R}}{\dfrac{1}{j\omega C_1} + \dfrac{R}{1 + j\omega C_2 R}} = \frac{j\omega C_1 R}{1 + j\omega C_2 R + j\omega C_1 R}$$

$$= \frac{j\omega C_1 R}{1 + j\omega (C_2 + C_1) R} = \frac{C_1}{C_1 + C_2} \cdot \frac{j\omega (C_1 + C_2) R}{1 + j\omega (C_2 + C_1) R} \equiv k \cdot \frac{j\dfrac{\omega}{\omega_c}}{1 + j\dfrac{\omega}{\omega_c}} \qquad \textbf{(8.3)}$$

The analysis of **(8.3)** has five steps. Step 1 is the raw potential divider expression that is successively simplified to step 4. Step 4 is clearly a high pass response because of the purely imaginary numerator but the standard form of **(2.2)** (repeated as a sixth term in **(8.3)**) requires that the coefficient of $j\omega$ in the numerator is forced to that in the denominator. This can be easily achieved at the expense of introducing a constant multiplier term consisting here of a capacitive potential divider. The l.f. gain, h.f. gain and time constant obtained from **(8.3)** are consistent with those obtained by inspection in section 6.

(iii) Step response

Assume an input step from 0 V to V_1 V at $t = 0$

The l.f. gain $\Rightarrow$ 0 as $\omega \Rightarrow 0$ rad s^{-1} so as $t \Rightarrow \infty$, $v_o \Rightarrow 0$.

The h.f. gain $\Rightarrow \dfrac{C_1}{C_1 + C_2}$ as $f \Rightarrow \infty$ so the step size is $V_1 \times \dfrac{C_1}{C_1 + C_2}$

The output waveshape is therefore a voltage step from 0 V to $V_1 \times \dfrac{C_1}{C_1 + C_2}$ V followed by an exponential of the form $V(t) = (V_1 \times \dfrac{C_1}{C_1 + C_2})\, e^{-t/\tau}$ where $\tau = R\,(C_1 + C_2)$.

Remember that the start voltage for the exponential is always the voltage at the end of any step arising at the output because of the transient change of input. Low-pass transfer functions (i.e., those of the same shape as **(2.1)**) do not have an output step in their step response whereas high-pass and pole-zero responses (i.e, **(2.2)** and **(2.3)**) always do.

9 Concluding comments

All the discussion here has been in terms of passive *RC* circuits. First order behaviour is also exhibited by *LR* circuits and by active circuits such as op-amp based amplifiers. The three standard forms apply to all manifestations of first order frequency dependent behaviour.

RCT 9/07

Frequency Dependent Aspects of Op-amps

Frequency dependent feedback circuits

The arguments that lead to expressions describing the circuit gain of inverting and non-inverting amplifier circuits with resistive feedback apply also to the more general case of a feedback network made of impedances.

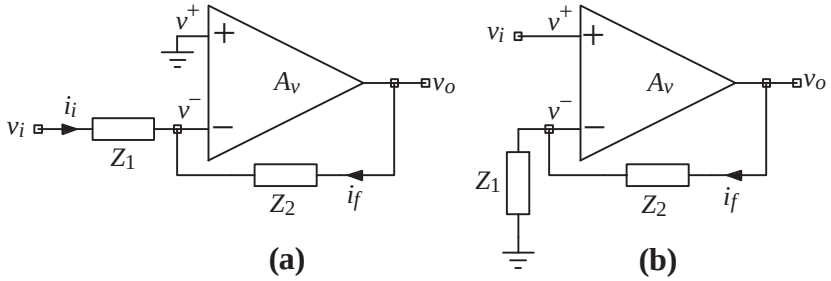


Figure 1
Op-amp circuits with complex impedance in the feedback circuit

For the inverting circuit of figure 1a, summing currents at the v^- node (assuming that the op-amp draws no input current) gives

$$i_i + i_f = 0 \text{ or } \frac{v_i - v^-}{Z_1} = \frac{v_o - v^-}{Z_2}$$

Since $A_v \Rightarrow \infty$, $v^- \approx v^+$ and since $v^+ = 0$, the circuit gain reduces to $\frac{v_o}{v_i} = -\frac{Z_2}{Z_1}$. **(1)**

For the non-inverting circuit of figure 1b, v^- is the potential division of v_o by Z_2 and Z_1 (again assuming that the op-amp draws no input current) and so

$$v^- = v_o \frac{Z_1}{Z_1 + Z_2}$$

Since $A_v \Rightarrow \infty$, $v^- \approx v^+$ and since $v^+ = v_i$, the circuit gain reduces to $\frac{v_o}{v_i} = \frac{Z_1 + Z_2}{Z_1}$. **(2)**

Although these results assume a perfect amplifier, they are valid for real amplifiers providing that the amplifier gain at the frequencies of interest is sufficiently high. In other words, as with resistive feedback, the circuit gain must be controlled by the feedback elements and not by the amplifier itself (to any significant extent) if the circuit is to be useful.

Notice that no restriction has been placed on the *Z*s - that simply means that the analytical approach to analysis does not put restrictions on the nature of *Z*. It does not imply that one can use any old *Z*; frequency dependent *Z* has the potential to cause instability. The rest of this section looks at a number of standard frequency dependent circuits.

The Integrator

The integrator was the workhorse circuit of analogue computers - it was central to the process of solving differential equations. These days it is its frequency dependent behaviour that is of

interest. Integrators are used in filtering circuits and in instrumentation circuits. The circuit diagram of an integrator circuit is shown in figure 2. There are two ways of deriving a relationship between input and output of this circuit; one is a frequency domain analysis and the other is a time domain analysis. The current and voltage variables shown in figure 2 are appropriate for the frequency domain analysis. For the time domain analysis, upper case versions of the symbols are used - eg, i_i for the frequency domain becomes I_I for the time domain.

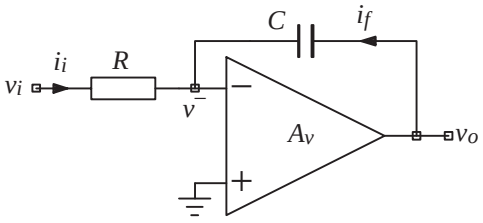


Figure 2

The op-amp integrator

Frequency domain analysis of an integrator

The circuit of figure 2 has the same shape as that of figure 1a. Z_2 is the impedance of C and Z_1 is simply R. The same same approximations regarding A_v that were used to derive equation **(1)** must be valid if the integrator is to be useful so the gain of the circuit is as described by equation **(1)**,

$$\frac{v_o}{v_i} = -\frac{\left(\frac{1}{j\omega C}\right)}{R} = -\frac{1}{j\omega CR}$$

It is quite common for the j and ω to be kept together and given the symbol s. Thus

$$\frac{v_o}{v_i} = -\frac{1}{j\omega CR} = -\frac{1}{sCR} \qquad \textbf{(3)}$$

The frequency response of the integrator in both magnitude and phase is shown in figure 3. The horizontal axis is a logarithmic frequency scale normalised to the frequency $\omega = 1/CR$. The ideal responses that describe equation **(3)** are the black lines. Since equation **(3)** suggests that

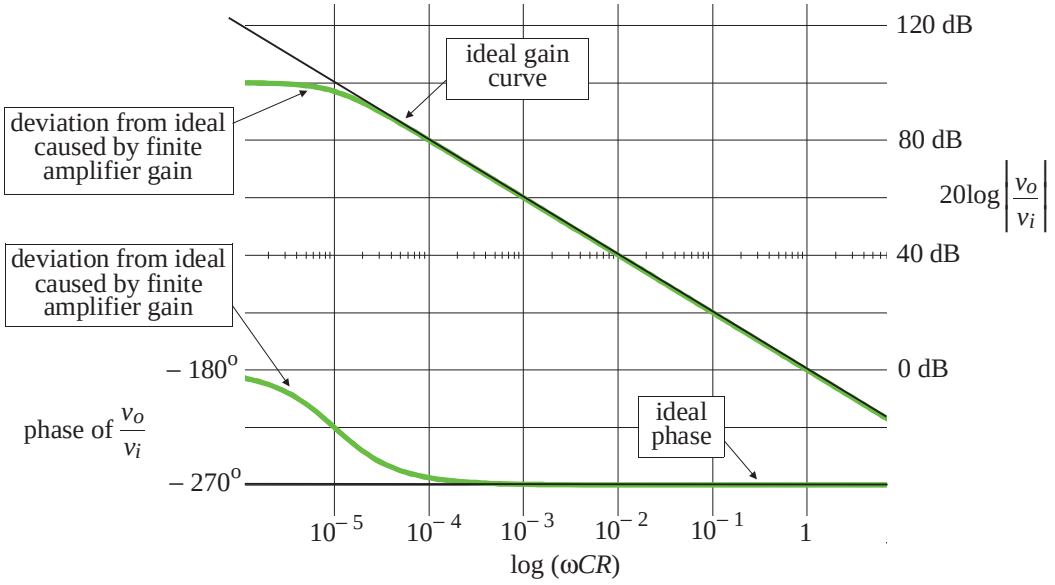


Figure 3

Amplitude and phase response of an ideal and a real integrator

as ω approaches zero, gain approaches infinity there must be some frequency at which the finite gain of real amplifiers affects performance. This is shown by the slightly lighter coloured curves that deviate from the ideal straight lines in the region of 10^{-4} to 10^{-6} on the normalised frequency scale. The integrator must be used in a frequency range where the magnitude and phase errors due to finite gain effects are negligible - for example, 10^{-3} or greater in the case of figure 3.

Time domain analysis of an integrator

For the time domain treatment of the integrator, current is again summed at the inverting input,

$$I_I + I_F = \frac{V_I - V^-}{R} + C\frac{d\,(V_O - V^-)}{dt} = 0 \qquad \textbf{(4)}$$

where $V_O - V^-$ is the voltage across the capacitor. Assuming (as for the frequency domain case) that $V^- \approx 0$, equation **(4)** simplifies to

$$\frac{V_I}{R\,C} = -\frac{dV_O}{dt} \qquad \textbf{(5)}$$

We want to find V_O in terms of V_I. Integrating both sides of equation **(5)** gives

$$V_O = -\frac{1}{C\,R}\int V_I\,dt + A \qquad \textbf{(6)}$$

where A is a constant of integration that represents the voltage across the capacitor due to its initial charge - the charge in the capacitor at the start of the integration interval.

Problems with integrators

The biggest problem with the integrator circuit arises because of its lack of dc feedback. Any small residual dc input, which may arise in the signal source or may exist at the op-amp input as an equivalent offset generator, will be integrated until the output magnitude is limited by the power supply voltage; in other words, the output saturates at one or other of the power supply voltages in the absence of dc feedback.

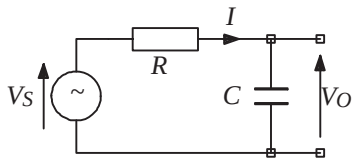


Figure 4

A simple RC circuit

In some applications the integrator forms part of a larger analogue system such that the rest of the system provides the dc feedback that the integrator needs. An example of this is using the integrator to emulate the behaviour of a first order *RC* circuit such as that of figure 4. V_O and I are given by

$$V_O = \frac{1}{C}\int I\,dt \quad \text{and} \quad I = \frac{V_S - V_O}{R}$$

and these two relationships can be combined to give

$$V_O = \frac{1}{CR}\int (V_S - V_O)\,dt = -\frac{1}{CR}\int (V_O - V_S)\,dt \qquad \textbf{(7)}$$

Equation **(7)** can be "solved" by the circuit of figure 5. Start by assuming that V_O exists. If it exists, it must be the result of integrating the difference between V_O and V_S. The difference is performed symbolically as shown. The summing amplifier in this case could be an op-amp

subtracting circuit with a gain of 1. Dc feedback is built in to the loop from the integrator output to the summing amplifier input. This approach to realising differential equation solutions formed the basis of analogue computers

Some dc feedback can be added to the basic integrator circuit by adding a resistor in parallel with C as shown in figure 6. This is an effective strategy in terms of stabilising the dc conditions in the circuit but it has an undesirable effect on the integration function. The dc gain of the integrator is effectively reduced from the open loop dc gain of the op-amp, $-A_0$, to a lower value, $-R_F/R$. The effect of this gain lowering is to move the deviations to gain and phase caused by finite amplifier gain (shown in figure 3) upwards in frequency thereby reducing the range of frequencies over which the integrator is useful.

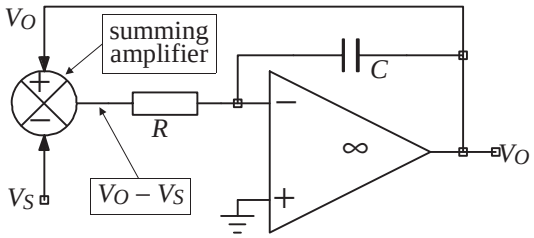


Figure 5

An integrator based system for solving a first order differential equation

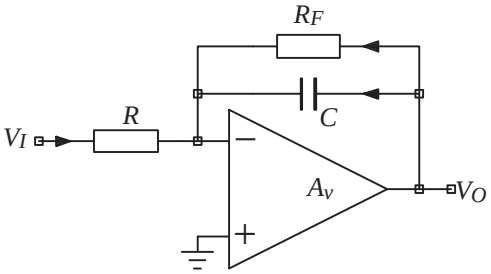


Figure 6

An integrator circuit with a feedback resistor to provide dc feedback

The Differentiator

If integration is possible with the help of an op-amp, it is reasonable to assume that differentiation is also possible. Consider the circuit of figure 7. The analytical process is the same as for the integrator except that the two key components have been interchanged. Using the same approximations and assumptions as were used for the integrator, the frequency domain approach leads to

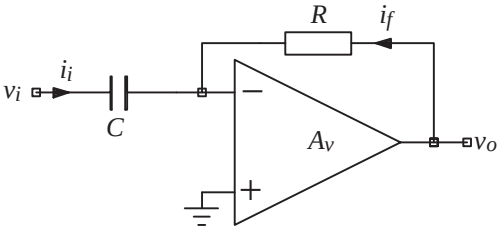


Figure 7

An op-amp differentiator circuit

$$\frac{v_o}{v_i} = -j\omega CR = -sCR \qquad \textbf{(8)}$$

and for the time domain $$V_O = CR\,\frac{dV_i}{dt} \qquad \textbf{(9)}$$

Although the differentiator looks attractive on the basis of this simple analysis, in fact the feedback components interact with the internal frequency response of the op-amp (which will be dealt with later) to form an underdamped second order (resonant) system. This interaction makes the differentiator virtually useless over a very wide range of operating frequency. Figure 8 shows the transient response of a typical op-amp differentiator to a triangular input signal. The output should be a rectangular waveform but notice how each change of slope is followed on the output trace by a lightly damped sinusoid. The circuit is stable but seriously underdamped.

It is possible to control the circuit damping by adding a resistor in series with C or a capacitor

in parallel with R but in controlling the damping the circuit becomes ineffective as a differentiator.

Differentiators also have a reputation for being noisy circuits - a slightly unfair reputation. White noise, the most common form of noise, has a constant power per unit bandwidth so any system that has a gain that increases with frequency will be subject to the same "noisy" problem.

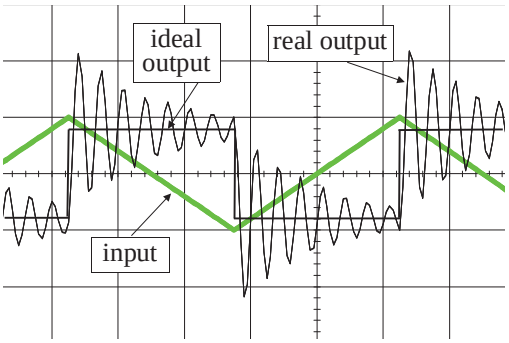


Figure 8

Ideal and real integrator output waveforms

Pole-zero (or lead-lag or lead-lag) circuits

These circuits are commonly used to manipulate the frequency or the phase response of electronic systems. The basic amplifier circuits of figure 1 are repeated here as figure 9 for convenience. The impedances Z_1 and Z_2 may be real or complex but there will only be one capacitor in the circuit and one of Z_1 and Z_2 will be real (ie, purely resistive). A couple of examples are given below.

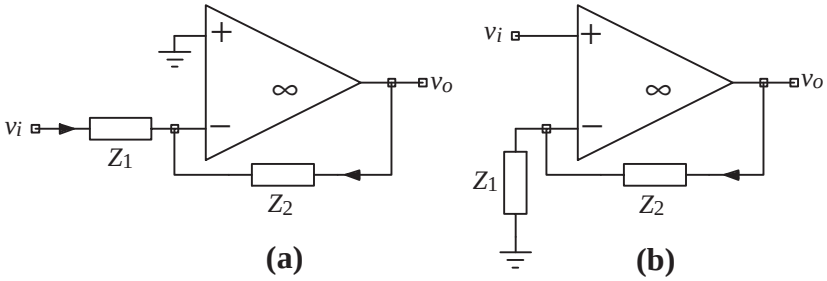


Figure 9

Op-amp circuits with complex impedance in the feedback circuit

Example 1

The circuit of figure 10 shows a non-inverting amplifier with frequency dependent feedback. Notice that the gain of the amplifier is assumed to approach infinity so the circuit behaviour is controlled by the feedback components. The gain of the non-inverting amplifier is given by equation **(2)** as

$$\frac{v_o}{v_i} = \frac{Z_1 + Z_2}{Z_1}$$

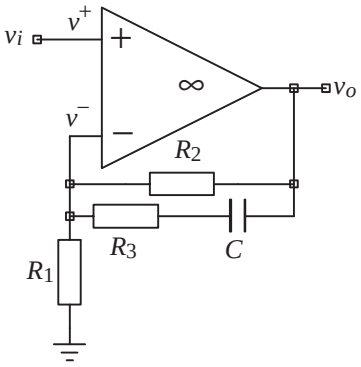


Figure 10

A non-inverting pole-zero circuit

In this circuit $Z_1 = R_1$ and $Z_2 = R_2 \,//\, (R_3 + Z_C)$ so

$$\frac{v_o}{v_i} = \frac{R_1 + \dfrac{R_2\left(R_3 + \dfrac{1}{j\omega C}\right)}{R_2 + R_3 + \dfrac{1}{j\omega C}}}{R_1} = \frac{R_1 + \dfrac{R_2(j\omega C R_3 + 1)}{j\omega C(R_2 + R_3) + 1}}{R_1} \qquad \textbf{(10)}$$

The aim is to reduce the gain expression to a ratio of two polynomials in $j\omega$. It is important to

keep j and ω together in this process. Simplifying further and collecting real and imaginary terms gives

$$\frac{v_o}{v_i} = \frac{R_1 + R_2 + j\omega C(R_1R_2 + R_1R_3 + R_2R_3)}{R_1(j\omega C(R_2 + R_3) + 1)} = \frac{R_1 + R_2}{R_1} \frac{1 + j\omega C\left(\frac{R_1R_2 + R_1R_3 + R_2R_3}{R_1 + R_3}\right)}{1 + j\omega C(R_2 + R_3)} \quad \textbf{(11)}$$

In equation **(11)**, a complex number of the form $a + jb$ has been modified to $a(1 + jb/a)$. This apparently pointless manipulation makes the frequency dependent function easier to interpret. If the time $C\frac{R_1R_2 + R_1R_3 + R_2R_3}{R_1 + R_2}$ is written as a frequency domain constant $\frac{1}{\omega_1}$ and the time $C(R_2 + R_3)$ is written as a frequency domain constant $\frac{1}{\omega_0}$, equation **(11)** can be rewritten as

$$\frac{v_o}{v_i} = k \frac{1 + j\frac{\omega}{\omega_1}}{1 + j\frac{\omega}{\omega_0}} = k \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_0}} \quad \textbf{(12)}$$

Equation **(12)** is in a first order "standard form". To interpret this transfer function we need to look at the basic behaviour of first order standard forms.

First order standard forms

First order transfer functions fall into one of the three standard forms:

low pass $$\frac{v_o}{v_i} = k \frac{1}{1 + j\frac{\omega}{\omega_0}} \quad \textbf{(13)}$$

high pass $$\frac{v_o}{v_i} = k \frac{j\frac{\omega}{\omega_0}}{1 + j\frac{\omega}{\omega_0}} \quad \textbf{(14)}$$

pole-zero $$\frac{v_o}{v_i} = k \frac{1 + j\frac{\omega}{\omega_1}}{1 + j\frac{\omega}{\omega_0}} \quad \textbf{(15)}$$

Equation **(15)** is the sum of a low pass, equation **(13)**, and a high pass, equation **(14)**, response with different frequency independent gains. The frequency responses for equations **(13)**, **(14)** and **(15)** are shown in figures 11, 13 and 15. The corresponding transient responses are shown in figures 12, 14 and 15.

In first order low pass and high pass circuits, the angular frequency ω_0, which is the reciprocal of time constant, is called the corner frequency - a brief inspection of figures **11** and **13** will reveal why. The pass band gain is given by $20\log k$ dB. Notice how good the straight line approximations (also known as Bode approximations) are to both the amplitude and phase responses. **Once the transfer function has been reduced to a standard form, ω_0, k and the response type completely specify the response shape.**

Low Pass

Frequency response :-

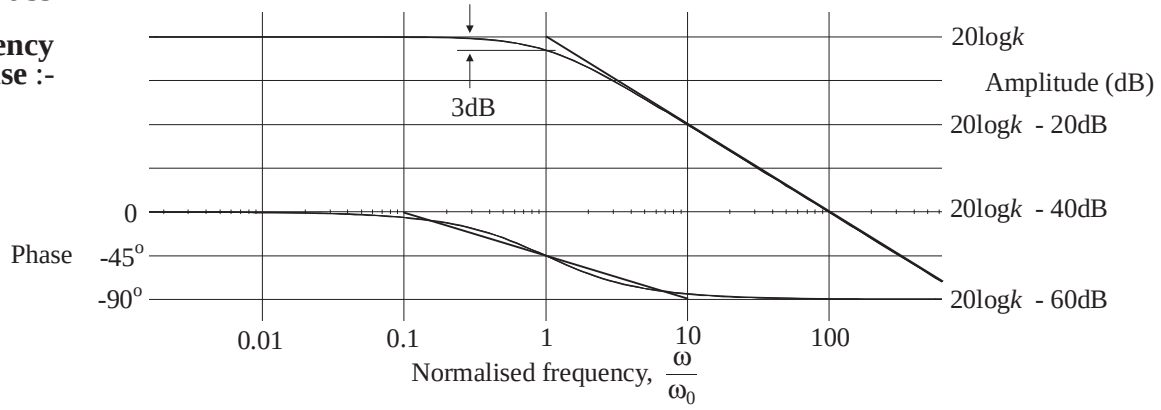


Figure 11

Frequency response of a first order low pass circuit. The corner frequency and gain, k, completely specify the response. The curves of gain magnitude and phase are real responses and the straight line approximations to them are called Bode approximations.

Transient response :-

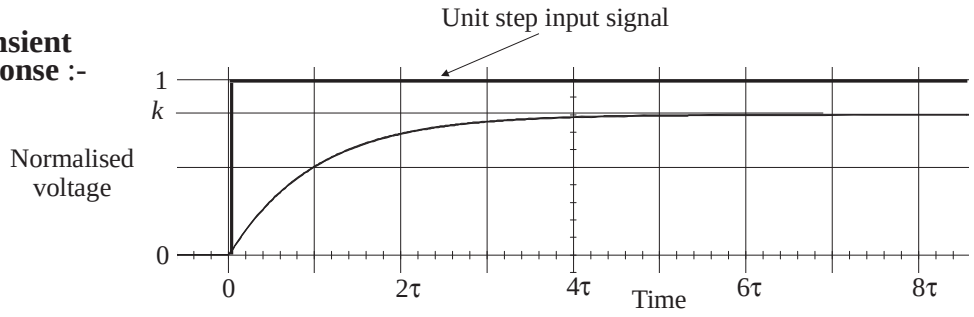


Figure 12

Step response of a first order low pass circuit. The two pieces of information that completely specify the response are step amplitude and circuit time constant.

High Pass

Frequency response :-

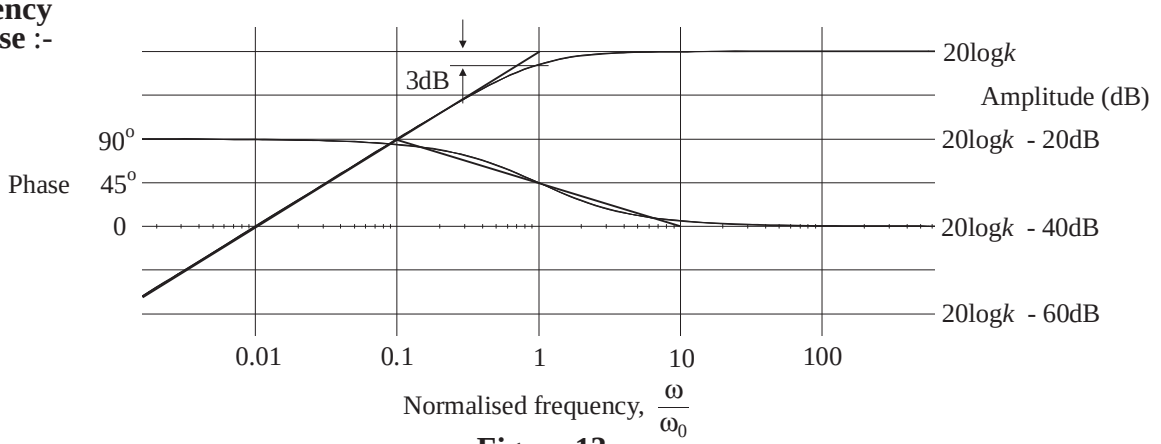


Figure 13

Frequency response of a first order high pass circuit. Again the high-pass response is completely specified by knowledge of corner frequency and k. The Bode approximations are shown on the graphs.

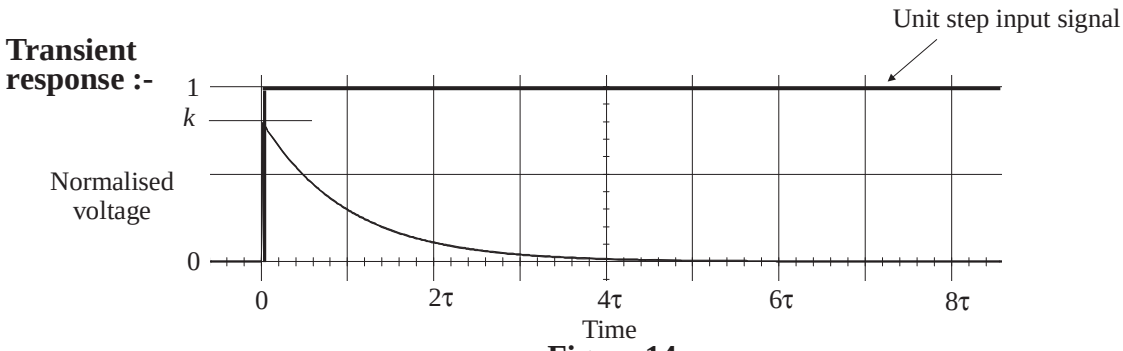


Figure 14

Step response of a high pass circuit. The response is completely specified by k and time constant or corner frequency.

The transient responses are easily drawn once the response type (high pass or low pass) has been identified. A circuit described by a low pass transfer function will always have a unit step (transient) response of the form $v(t) = k\,(1 - \exp(-t/\tau))$ whereas one described by a high pass transfer function will always have a unit step response of the form $v(t) = k \exp(-t/\tau)$. In both cases $\tau = 1/\omega_0$. In the low pass case the frequency independent gain k determines the aiming level of the exponential rise while in the high pass case k determines the initial height of the exponential waveshape. If the amplitude of the input step is V_S, the initial height and aiming levels become kV_S instead of k.

Pole - Zero

The pole-zero standard form is a linear sum of high pass and low pass forms, each being multiplied by a different frequency independent gain. Equation **(15)** can be expanded as follows:

$$\frac{v_o}{v_i} = k\,\frac{1+j\,\frac{\omega}{\omega_1}}{1+j\,\frac{\omega}{\omega_0}} = k\,\frac{1}{1+j\,\frac{\omega}{\omega_0}} + k\,\frac{j\,\frac{\omega}{\omega_1}}{1+j\,\frac{\omega}{\omega_0}} = k\,\frac{1}{1+j\,\frac{\omega}{\omega_0}} + \frac{k\,\omega_0}{\omega_1}\,\frac{j\,\frac{\omega}{\omega_0}}{1+j\,\frac{\omega}{\omega_0}} \qquad \textbf{(16)}$$

The form of equation **(15)** is most useful from the point of view of frequency responses but the final form of equation **(16)** is most useful from the point of view of transient responses. The gain multiplying the low pass part of equation **(16)** - the low frequency gain - can in general be larger than or smaller than the gain multiplying the high pass part of equation **(16)** - the high frequency gain. In some cases one is always higher than the other.

The pole-zero response of figure 15 is drawn for a circuit where the low frequency gain is lower than the high frequency gain or, in other words, in terms of equation **(15)**, $\omega_1 < \omega_0$. The high frequency gain, k_H, is $k_L\omega_0/\omega_1$ as in the final form of equation **(16)**. Notice the parts ω_0, ω_1, k_L and k_H play in the response shapes - once again they provide the coordinates needed for a straight line approximation to the real curve and define the initial and aiming levels of the transient response.

The phase response appears here as a positive going hump. It gets close to 90^o only if ω_0 and ω_1 are widely spaced (say two orders of magnitude or more). It is not easy to make an accurate sketch of the phase response for pole-zero circuits without evaluating some points on the phase-frequency graph. This shape of phase response is useful as compensation to ensure stability in feedback systems and is commonly used in such applications.

The step response moves exponentially from its initial value to its aiming level with a time

constant of $1/\omega_0$. **Notice that it is always the denominator of the transfer function that gives the circuit time constant.**

If $\omega_0 < \omega_1$ the high frequency gain is lower than the low frequency gain, so the gain falls between ω_0 and ω_1. The phase is a negative going hump - essentially an upside down version of the shape shown. The transient response becomes a rising exponential starting with an initial step of k_H (for a unit step input) and aiming for a level of k_L with a time constant of $1/\omega_0$.

Frequency response :-

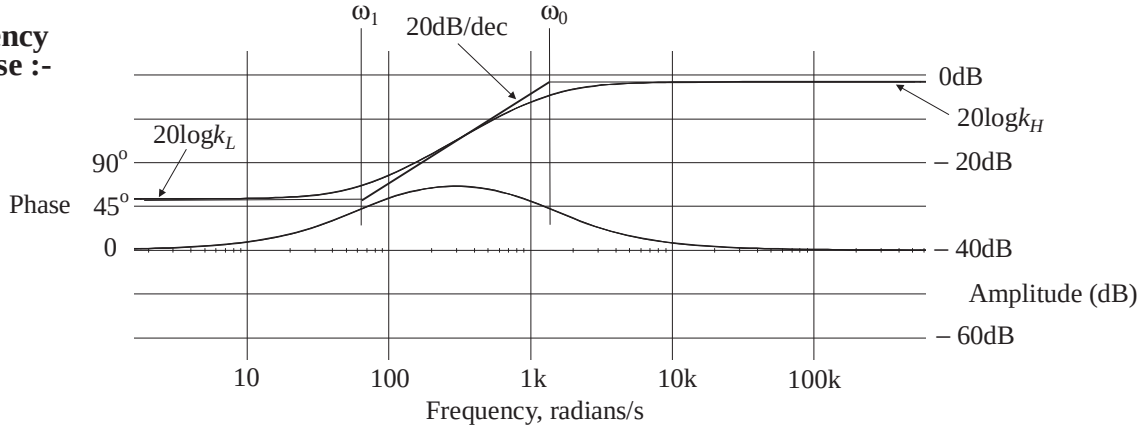


Figure 15

A pole-zero response for a circuit where low frequency gain is lower than high frequency gain. Notice that the gain approaches steady values at low frequencies and at high frequencies

Transient response :-

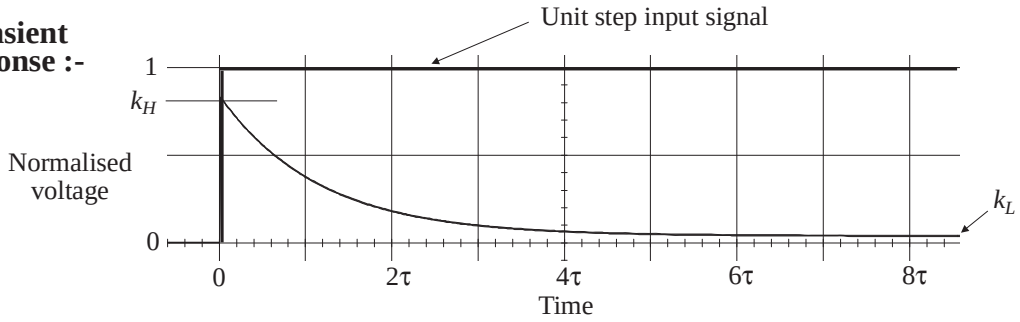


Figure 16

The step response of a pole-zero circuit. Notice that the gain of the low pass part of the circuit determines the aiming level whilst the initial step height is controlled by the high-pass gain. All amplitude values are proportional to the step height.

Returning to example 1 of figure 10 . . . .

The response can be identified as a pole-zero response by comparing the transfer function of equation **(12)** with the three standard forms of equations **(13)**, **(14)** and **(15)**. In the circuit of figure 10 the high frequency (h.f.) gain is lower than the low frequency (l.f.) gain. This fact can be deduced as follows:

At high frequencies, the reactance of C is much less than the resistances in the circuit so C can be regarded as a short circuit. This leads to a feedback path with an effective resistance of $R_2//R_3$. The h.f. gain is thus $\frac{v_o}{v_i} = \frac{R_1 + (R_2//R_3)}{R_1} = 1 + \frac{R_2//R_3}{R_1}$. The l.f. gain can be found by

letting the capacitive reactance become much larger than the surrounding resistors. The feedback path now has an effective resistance of R_2 and the gain becomes $\frac{v_o}{v_i} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$. Since $R_2//R_3$ must be smaller than R_2, the h.f. gain must be smaller than the l.f. gain. It is always worth performing this quick estimate of high and low frequency gains as a check of your analysis.

It is also possible to find the h.f. and l.f. gain from equation **(12)** by letting ω approach zero for l.f. and infinity for h.f.. The modulus of equation **(12)** is

$$\left|\frac{v_o}{v_i}\right| = k\left[\frac{1+\frac{\omega^2}{\omega_1^2}}{1+\frac{\omega^2}{\omega_0^2}}\right]^{\frac{1}{2}} \qquad \textbf{(17)}$$

If $\omega \ll \omega_1$ and $\omega \ll \omega_0$ then the circuit gain approaches k and this is the l.f. gain. If $\omega \gg \omega_1$ and $\omega \gg \omega_0$ then the circuit gain approaches $k\,\omega_0/\omega_1$ and this is the h.f. gain.

Example 2

The circuit of figure 17 is an inverting amplifier. Making the assumption that A_V approaches infinity, v_o/v_i is given by equation **(1)**,

$$\frac{v_o}{v_i} = -\frac{Z_2}{Z_1}$$

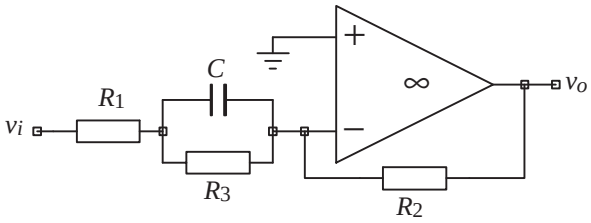


Figure 17
A inverting pole-zero circuit

In this circuit, $Z_1 = R_1 + (R_3//C)$ and $Z_2 = R_2$. Thus

$$Z_1 = R_1 + \frac{\frac{R_3}{j\omega C}}{R_3 + \frac{1}{j\omega C}} = R_1 + \frac{R_3}{1 + j\omega C R_3}$$

and circuit gain is given by

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1 + \frac{R_3}{1+j\omega C R_3}} = -\frac{R_2\,(1+j\omega C R_3)}{R_1 + j\omega C R_1 R_3 + R_3}$$

$$= -\frac{R_2\,(1+j\omega C R_3)}{R_1 + j\omega C R_1 R_3 + R_3} = -\frac{R_2\,(1+j\omega C R_3)}{(R_1+R_3)\left(1+j\omega C\frac{R_1 R_3}{R_1+R_3}\right)} = -k\,\frac{1+j\frac{\omega}{\omega_1}}{1+j\frac{\omega}{\omega_0}} \qquad \textbf{(18)}$$

where $k = \frac{R_2}{R_1+R_3}$, $\omega_1 = \frac{1}{CR_3}$ and $\omega_0 = \frac{R_1+R_3}{C\,R_1 R_3}$

Once again the transfer function can be expressed in the standard form given by equation **(15)** which allows figure 17 to be identified as a pole-zero circuit. By inspection the l.f. gain (when C looks like an open circuit) is $-R_2/(R_1+R_3)$ and the h.f. gain (when C looks like a short circuit)

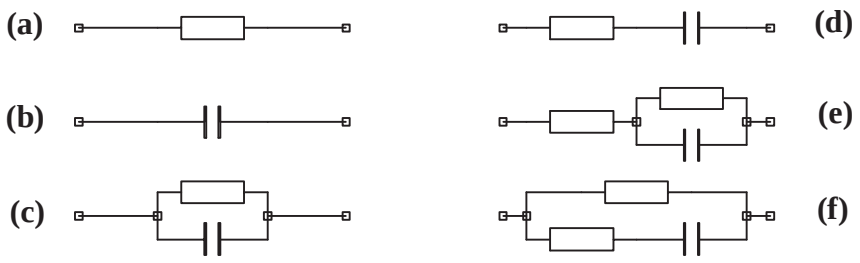


Figure 18

Commonly used networks for Z_1 and Z_2. Networks (b) and (d) are not suitable for Z_2 in single op-amp applications because they do not permit dc feedback.

is $-R_2/R_1$ and these values can be used to check the analytical result of equation **(18)**. The h.f. gain is larger than the l.f. in this case and the response will resemble that of figure 16.

There is a wide range of feedback circuits that one might come across in pole-zero applications. A selection of these is shown in figure 18. In general the feedback element, Z_2, will have to allow dc feedback, the exception being where dc feedback is provided by some other path such as the system shown in figure 5. In all the pole-zero applications, either Z_1 or Z_2 will be a simple resistor - ie, figure 18 (a).

Intrinsic linear frequency response of the op-amp

The op-amp itself is not perfect in terms of frequency response; it has a limited bandwidth. Figure 19 shows the frequency response associated with A_v - the open loop gain - for a typical op-amp. Also shown in figure 19 are two closed loop gain responses for different closed loop gains. Only one of the closed loop phase responses has been shown in order to avoid clutter on the diagram. Key points are

- all the roll-offs follow the open loop curve
- each of the three responses shown exhibit first order behaviour.
- for the open loop response the product of dc gain and -3 dBbandwidth - 300,000 x 10 Hz in this case - is equal to the product of gain and frequency at f_1 - the point where gain is unity (1 x 3 MHz in this case).
- for the closed loop gain cases, the product of dc gain (ie. the gain at a frequency low enough such that gain is independent of frequency) and the - 3dB frequency is a constant equal to the unity gain frequency of the open loop response.

This leads to the important idea

dc gain x -3dB bandwidth = constant = open loop unity gain frequency

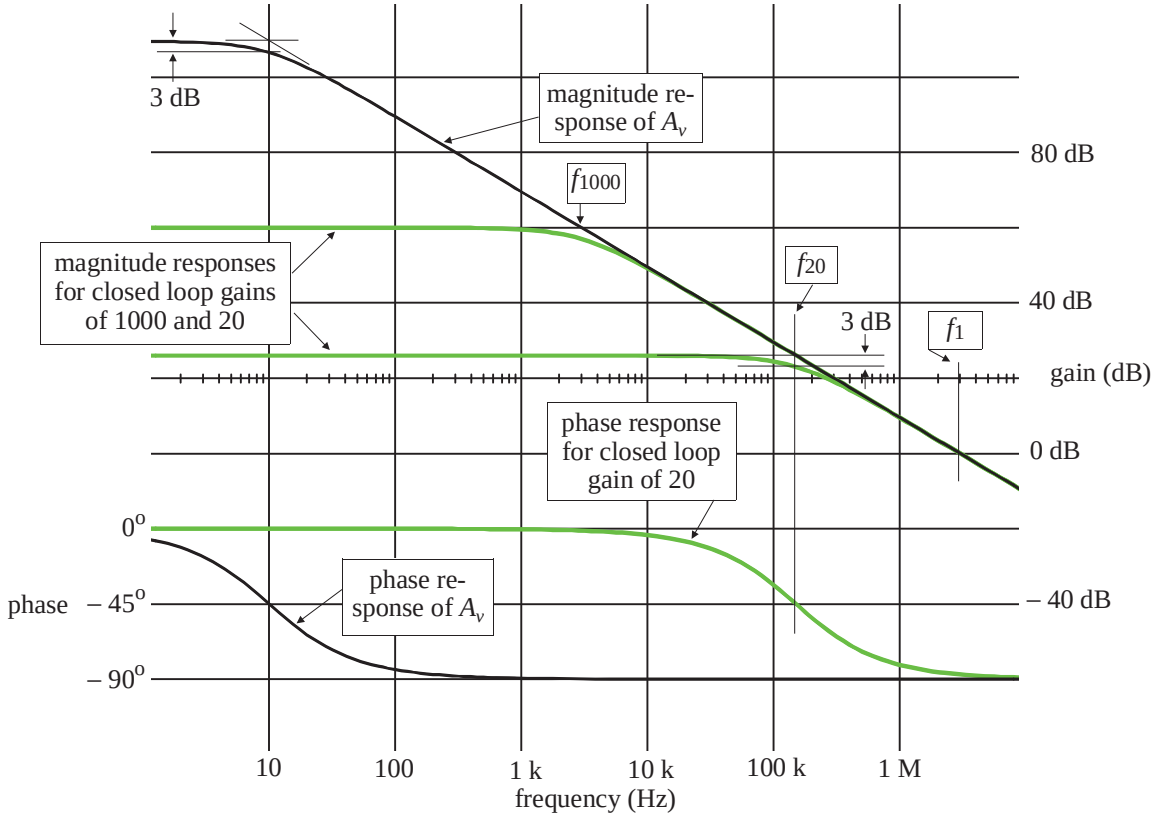


Figure 19

The open loop response of a typical op-amp with two closed loop responses on the same graph. Only one of the closed loop phase responses has been shown.

The ***only*** information provided by manufacturers to describe the linear frequency response behaviour is the "gain - bandwidth" product (*GBP*) or "unity gain frequency". Because the amplifier behaves as a first order system, this parameter and knowledge of circuit gain is all that is required to work out any aspect of linear frequency or time dependent behaviour. For circuits with frequency dependent feedback, the gain-bandwidth product idea can be used when the phase shift due to the feedback circuit is close to zero at the frequency where the circuit high frequency gain meets the op-amp's open loop response. If feedback phase is significant at this point, the circuit must be treated as a second order system (and they will not be dealt with in this module).

Knowing *GBP* (or unity gain frequency) and required circuit gain, the circuit bandwidth can be evaluated. Manufacturers usually quote unity gain frequency in Hz but in circuit design situations it may be necessary to convert this to radians per second. Since the op-amp and op-amp circuits with resistive feedback behave like first order systems, knowledge of frequency domain behaviour also gives knowledge of time domain behaviour.

The key first order relationships of the op-amp itself are between gain and frequency and time and frequency

$$A_v = \frac{A_0}{1 + j\dfrac{\omega}{\omega_0}} \qquad \textbf{(19)}$$

$$\tau = \frac{1}{\omega_0} = \frac{1}{2\pi f_0} \qquad \text{or} \qquad f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\,\tau} \qquad \textbf{(20)}$$

where A_v is the amplifier gain. A_0 its dc (0 Hz) gain, τ is the system time constant, f_0 is the cyclic open loop corner frequency (in Hz) and ω_0 is the angular open loop corner frequency (in radians per second). For a non-inverting amplifier with feedback that behaves resistively

$$K_v = \frac{K_0}{1 + j\dfrac{\omega}{\omega_K}} \text{ where } \omega_K = \frac{GBP}{K_0} \text{ and } \tau_K = \frac{1}{\omega_K} \qquad \textbf{(21)}$$

In equation **(21)** *GBP* must be in radians per second. Equation **(21)** could be written in terms of cyclic frequency by changing all ω_K to f_K and using the ω - f relationships of equation **(20)**.

The "gain x bandwidth = constant" rule is true for all non-inverting amplifier circuits built using amplifiers that are described by manufacturers as "unity gain compensated". The intrinsic response of the amplifier is usually not first order - in fact most amplifiers have three first order responses in series, one for each of input stage, voltage gain stage (VAS) and output stage. This is not a problem if over the range of frequency where $|A_v| > 1$, the behaviour is governed by one of the three first order behaviours - usually that associated with the VAS. In a unity gain compensated amplifier, a category that encompasses almost all general purpose amplifiers, the manufacturers deliberately ensure that the VAS response dominates the amplifier response for all $|A_v| > 1$. They do this by deliberately increasing the collector - base capacitance of the VAS transistor to a value of between 10 pF and 30 pF as necessary. The effect of this capacitor is magnified as far as the base circuit of the VAS is concened by an effect known as Miller multiplication.

Miller multiplication is an effect that can be explained by the Miller Transform, a circuit transformation that represents feedback elements connected between input and output of an amplifier as equivalent shunt elements between input and ground and output and ground.

Consider figure 20. In figure 20(a) an amplifier with a parallel *RC* feedback circuit is shown. The amplifier has a terminal voltage gain *A*. The Miller Transformation identifies the effective values of the feedback elements *R* and *C* from the point of view of the source circuit (ie, the circuit that produces v_i) and the load circuit. Effectively this process aims to model the circuit of figure 20(a) with that of figure 20(b) and the Miller transformation finds the C_{iM} and R_{iM} that give the same ratio v_i/i_i for both parts of figure 20.

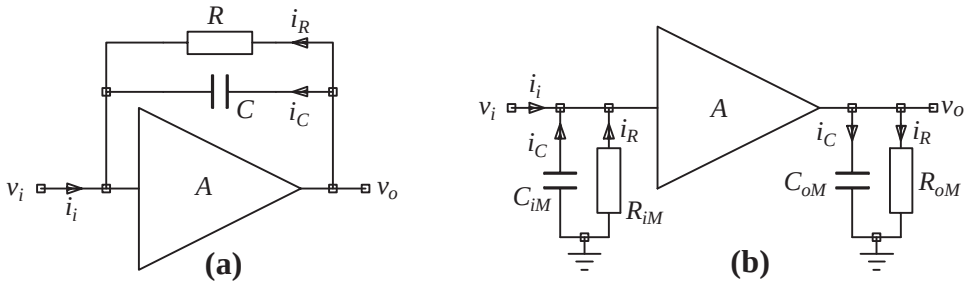


Figure 20

*An amplifier circuit **(a)** with its Miller transformed feedback components **(b)***

In figure 20(a), i_R and i_C are given by

$$i_R = \frac{v_o - v_i}{R} \text{ and } i_C = (v_o - v_i)j\omega C .$$

In figure 20(b), i_R and i_C are given by

$$i_R = \frac{0 - v_i}{R_{iM}} = \frac{-v_i}{R_{iM}} \text{ and } i_C = -v_i\, j\omega C .$$

For the two circuits to be the same from the source point of view i_R and i_C in figure 20(a) must be the same as the i_R and i_C in figure 20(b). Thus

$$i_R = \frac{v_o - v_i}{R} = -\frac{v_i}{R_{iM}} \qquad \text{or} \qquad \frac{Av_i - v_i}{R} = -\frac{v_i}{R_{iM}}$$

$$\text{so } R_{iM} = \frac{R}{1-A} \tag{22}$$

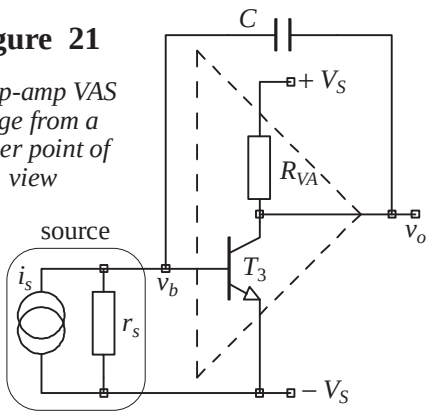
and $$i_C = (v_o - v_i)j\omega C = -v_i\, j\omega C_{iM} \qquad \text{or} \qquad (Av_i - v_i)j\omega C = -v_i\, j\omega C_{iM}$$

$$\text{so } C_{iM} = C\,(1-A) \tag{23}$$

This means that as far as the amplifier's signal source is concerned, the feedback impedance is a factor of $(1-A)$ times lower than the component face value. Thus, the effective capacitance seen by the signal source is $(1-A)$ times the actual value of feedback capacitance and this effect is known as Miller multiplication. In the case of the VAS stage, the effective circuit is shown in figure 21. *C* is the total capacitance between collector and base nodes (sometimes called the Miller capacitance). The gain $v_o/v_b \equiv A = -g_{m3}R_{VA}$ which

Figure 21

An op-amp VAS stage from a Miller point of view



is usually a large negative number (typically – 500 to – 50,000). Thus the equivalent circuit seen by the source is as shown in figure 22. If T_3 is a Darlington connected pair, r_{be3} could be several hundred kΩ so the large τ caused by the large effective C gives rise to a low corner frequency.

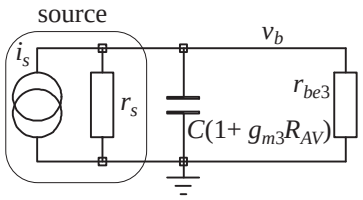


Figure 22

The equivalent circuit seen by the output of the differential input stage (the source) as it looks into the input of the VAS stage

There are also components C_{oM} and R_{oM} between the amplifier output and ground and for completeness these shoul;d be mentioned. These tell us what the feedback elements look like from the amplifier output's point of view. If A is large and negative, these components have effective values that are close to the actual feedback component values. Using an approach similar to that used for the input Miller transformed feedback elements the output elements are

$$R_{oM} = R\frac{A}{A-1} \text{ and } C_{oM} = C\frac{A-1}{A}$$

Note that no conditions have been imposed upon A in the foregoing considerations. A could be positive or complex. A moment's thought will reveal that this opens up some interesting possibilities. We assume here that A is real, negative and large. Note also that R_{oM} and C_{oM} represent the impedance of the feedback components as seen by the op-amp output; they do not represent the output impedance of the whole circuit.

[Where a feedback resistance exists, its effective value from a source point of view is its actual value divided by the factor $(1-A)$. One example of this effect is a simple op-amp inverting amplifier circuit. In such a circuit there is a feedback resistor, R_F, but usually no capacitor. The feedback resistor is connected between the output and the inverting input. From the point of view of the signal source the input impedance of the circuit is usually taken as the resistor, R_1, between the source and the inverting input - but this assumes infinite op-amp gain. As far as the input circuit is concerned, R_F appears as a resistor between inverting input and ground with a value of $R_F/(1-A)$. For typical values of A and R_F - say 3×10^5 and 100 kΩ - $R_F/(1-A) = 0.3$ Ω, a very low value. This is another way of looking at the notion of a virtual earth.]

Non-linear effects - slew rate limiting

A second frequency dependent effect that is of some importance in applications where a big output voltage swing at high frequencies is required is known as "slew rate limiting". Slew rate limiting is a process that limits the maximum rate of change of voltage that the op-amp can support at its output and is usually specified by manufacturers in terms of V μs^{-1}. Slew rate limiting is a non-linear process - its effect depends on the magnitude of the signal as well as on the frequency of the signal. Slew rate limiting is non linear because when it occurs, the ratio $\Delta v_o/\Delta v_i$ is a function of v_i - ie, gain depends upon signal level - a classic sign of a non-linear process.

Slew rate limiting is caused by the interaction between the collector - base capacitance, C_{cb}, of the voltage gain (VAS) transistor and the current sources that drive the collector and base nodes of that transistor. The fact that manufacturers artificially increase the value of C_{cb} of the VAS transistor in compensated amplifiers makes slew rate limiting more of a problem for them. Generally speaking, the less compensation an amplifier has, the better will be its slew rate capabilities . . . . but it might have stability problems in low gain applications. These two competing effects provide a good example of an engineering design tradeoff; one desirable

system property wants a parameter to be large, another wants it to be small.

From an application circuit design point of view one would usually specify a minimum slew rate requirement for any amplifiers in the design based on knowledge of the worst case signal the amplifier must handle. From a slew rate point of view the worst case is the largest rate of change of voltage that will ever occur in the signal at the op-amp output.

Rectangular waveshapes

Rectangular waveshapes with ideal (instantaneous) rising and falling edges applied to the op-amp input will produce exponential responses at the output because of the op-amp's first order frequency response behaviour. If the rising and falling edges of the input waveform are not ideal the output response will have a lower maximum rate of change than it would for an ideal input so the ideal input provides a good working worst case estimate. A positive going step input to an amplifier circuit described by equation **(21)** would yield an output response of the form

$$v_o(t) = v_{span}\left(1 - e^{-\frac{t}{\tau_K}}\right)$$

where v_{span} is the difference between starting and aiming levels of the rising exponential. The maximum rate of change of this function is v_{span}/τ_K and occurs at the start of the exponential shape. This maximum rate of change of v_o is a function of τ_K and hence of K_0.

Sinusoidal waveshapes

A sinusoid at the output of an amplifier circuit is

$$v_o(t) = v_P \sin \omega t$$

where v_P is the amplitude of the sinusoid. The largest rate of change of $v_o(t)$ is $v_P\omega$.

Solving problems

The design problems associated with slew rate limiting fall usually into two types - both different forms of the same problem.

One is to identify a suitable op-amp for a particular application based on knowledge of the application requirements and published op-amp specifications. Here the objective is to identify the biggest rate of change of voltage in the required output signal and then search for an amplifier that can meet that requirement.

The other is to identify what limitations in terms of frequency and/or amplitude of output signal will be imposed on a design by the use of a particular op-amp. These problems can be expressed in a number of ways but they all involve equating a maximum rate of change of signal voltage at the amplifier output to the slew rate.

Noise

1 Introduction

In general, the term "noise" is used to describe any unwanted signal but sources of noise can be divided into three main categories:

Man - made - This is noise that originates in some form of human activity. Some examples are; unwanted intrusion of radio communication into audio systems, poorly suppressed commutation in brushed ac motors and the reception of terrestrially generated signals in astronomical radio telescopes.

Natural external - This is noise that is caused by natural electromagnetic disturbances in our environment. The lightning associated with thunderstorms and high energy cosmic rays are two examples of the most energetic events.

Natural internal - This is the hiss that you hear if you listen to your stereo with a high volume setting but no programme material. It is caused by the individual behaviour of electrons as they pass through electronic components.

Man - made noise can usually be reduced at source by the application of appropriate suppression or screening strategies. There exists a comprehensive set of legislation which defines how much noise a piece of modern equipment is allowed to emit either as radiation or back into the main power supply; considerations such as these fall under the term "electromagnetic compatability". The effects of natural external noise can be reduced by careful screening of sensitive circuitry and appropriate filtering on all input and output connections to the system. Natural internal noise is generated within the resistors, diodes and transistors that make up a system, so in that sense it is the enemy within. It is natural internal noise which is of interest in what follows. After discussing how a random noise signal is quantified and characterised, the effects of noise in circuits and systems are examined and, where possible, design approaches that minimise the effects of internal noise are mentioned.

2 Quantifying and Characterising Random Noise

(i) Amplitude

If looked at on an oscilloscope, random noise looks like a thick woolly horizontal trace with no detectable coherent shape, as shown in figure 1. The noise voltage waveform, $v_n(t)$, is a completely random variable - in other words, knowledge of its value at one instant of time offers no information about its value at the next instant and the usual concept of amplitude is meaningless. Thus changing the timebase setting of the oscilloscope will leave the trace unchanged. (This is true providing the time-

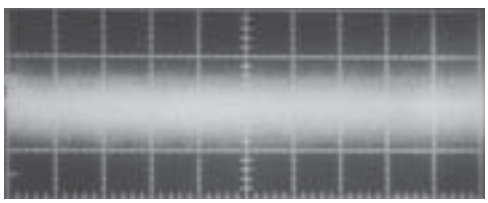


Figure 1

An analogue oscilloscope trace showing the appearance of random noise. The lack of coherence in the noise signal causes succesive traces to follow different paths across the screen. A crude idea of the distribution of noise amplitudes can be inferred from the way trace intensity changes from its centre to its extremes.

base setting is not such that the frequencies being viewed are close to the oscilloscope's bandwidth limit. The finite bandwidth of the oscilloscope gives a visible degree of coherence to the noise waveform in the immediate vicinity of the trigger point at faster timebase settings.) Digital ocilloscopes will display noise in a slightly different way.

The time average value of the sort of random waveform of interest here is zero, ie

$$\frac{1}{t_1}\int_0^{t_1} v_n(t)dt \;\rightarrow\; 0 \text{ as } t_1 \;\rightarrow\; \infty .$$

Although the time average value of $v_n(t)$ is zero, its instantaneous value is non - zero for most of the time and consequently it is capable of dissipating power in a resistor. This power dissipation capability is used to obtain some useful measure of noise amplitude. Power dissipation is proportional to the "mean square" value of a voltage (or current) waveform so the amplitude of $v_n(t)$ is usually expressed as a mean square value, $\overline{v_n^2}$ (with units of V^2) or as a root mean square (rms) value , $\sqrt{\overline{v_n^2}}$ (with units of V). Some writers say that the peak to peak value of random noise is six times its rms value (or peak is three times rms). They mean that from a *statistical* point of view the peak to peak value of the noise is less than six times the rms value for 99.7% of the time, but it should always be remembered that, since the instantaneous behaviour of a noise voltage cannot be predicted, this figure is only an approximation.

(ii) Frequency Distribution

Noise tends to have its most serious effects in circuits dealing with small signals, such as audio amplifier front ends for tape heads or microphone, satellite TV receivers and radar/radio systems. Since all these systems have particular bandwidths, it is useful to know how much noise energy exists within a particular bandwidth.

Being a random function of time, the noise voltage $v_n(t)$ contains energy over a wide range of frequencies. The frequency distribution of the noise is described in terms of mean square voltage per unit bandwidth. Imagine that $v_n(t)$ is put through a tuneable filter with a bandwidth δf centred on f_o, where δf is small enough to be singling out only the f_o frequency component of $v_n(t)$. Imagine also that the filter output is fed to a mean square voltmeter whose output, $\overline{v_n^2}(f_o)$, represents the noise power within the bandwidth δf. Such a hypothetical system is shown in figure 2.

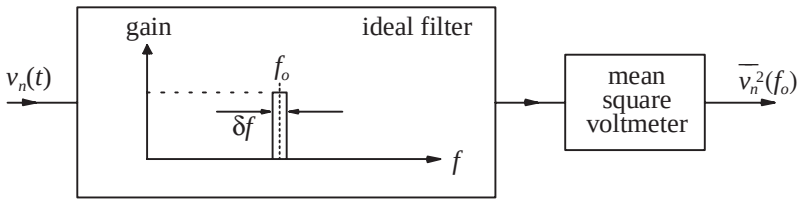


Figure 2

A notional system to measure the power spectrum of a noise signal.

If f_o is tuned over all frequency and $\frac{\overline{v_n^2}(f_o)}{\delta f}$, = $\overline{v_n^2}(f)$, the noise spectral density with units of $V^2\ Hz^{-1}$, is plotted as a function of frequency, the resulting curve, known as the "power spectral density" of the noise, describes how the noise power delivering capability of $v_n(t)$ varies with frequency.

In most cases of interest for natural internal noise, the power spectral density is independent

of frequency. This means that the noise has the same energy for a unit bandwidth placed anywhere on the frequency scale. Such noise is called "white" by analogy with white light. There are some noise sources that have a power spectral density curve that gets smaller as frequency increases; such noise is known as "pink", again by analogy with light. Figure 3 shows the power spectral density curves for white and pink noise.

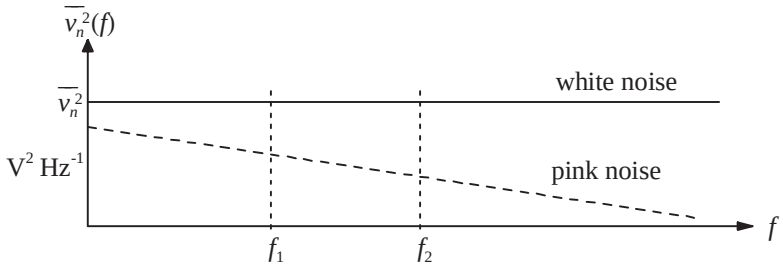


Figure 3
The power spectra of white noise and pink noise.

To find the total mean square noise voltage within a given frequency range, the power spectral density curve must be integrated over the frequency range of interest. This is straightforward for the case of white noise since its power spectral density is constant, so over a bandwidth of $(f_2 - f_1)$, the total mean square voltage is:

$$\overline{v_{nT}^2} = \int_{f_1}^{f_2} \overline{v_n^2}(f)df = \overline{v_n^2}(f_2 - f_1) = \overline{v_n^2} B = \overline{v_n^2} \Delta f \quad V^2$$

where $(f_2 - f_1)$, B and Δf are three commonly used symbols for bandwidth. For pink noise the integral is the same but the result is not as straightforward because $\overline{v_n^2}(f)$ is a function of frequency. It follows that $\overline{v_n^2}(f)$ must be known in order to evaluate the integral.

3 Internal Noise Sources

There are several types of noise source in electronic devices. The two most important are thermal noise and shot noise and these are dealt with below. A third noise source, flicker noise is also mentioned below. There are sources such as partition noise which, although important in multi-electrode vacuum tubes and some solid state devices, will not be considered here.

(i) Thermal or "Johnson" noise - (white)

Thermal noise is caused by the random thermal motion imparted to electrons by collision interactions with the structure of the resistive medium through which the electrons are travelling. It is modelled as a Thevenin equivalent as shown in figure 4.

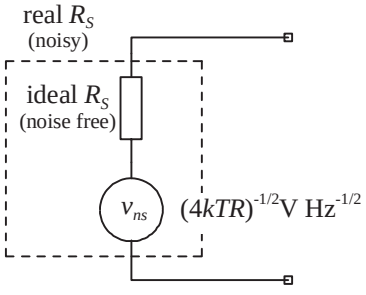


Figure 4
The noise equivalent circuit of a resistor

Thermal noise is given by:

$$\overline{v_n^2} = 4kTR \ V^2\ Hz^{-1}$$
$$= 4kTR\,\Delta f \ V^2$$

where:

k = Boltzmann's constant (1.38×10^{-23} J K^{-1})
T = Absolute temperature
R = Static resistance
Δf = Bandwidth

Note that thermal noise is **not** generated by incremental, slope, dynamic or differential resistances. Only static resistances which obey Ohm's law generate noise.

(ii) Shot noise - (white)

Shot noise is due to the fact that current is not continuous but composed of packets of charge. It is caused by the individual way in which electrons cross potential barriers in devices such as p-n junctions and thermionic diodes. The noise is modelled by a noise current generator in parallel with the noise free diode slope resistance as shown in figure 5.

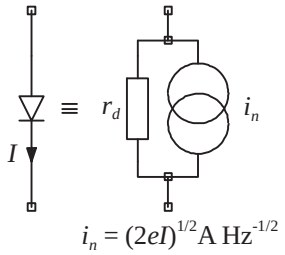


Figure 5

The noise equivalent circuit of a diode. $r_d = kT/eI$ for a p-n junction

Shot noise is given by:

$$\overline{i_n^2} = 2eI \text{ A}^2 \text{ Hz}^{-1}$$
$$= 2eI\Delta f \text{ A}^2$$

where:

e = electronic charge (1.6×10^{-19} C)
I = diode current (A)
Δf = bandwidth of interest

(iii) "1/f" or "flicker" noise - (pink)

There are many other names that have been used to describe this type of noise, partly because its origins are obscure and partly because its behaviour varies widely in different devices. The name "1/*f*" is probably the most useful of the names because it gives an approximate idea of how the noise power spectral density varies with frequency; other names tend to reflect the subjective impressions that this type of noise has created in its observers.

1/*f* noise affects all solid state devices and many other electronic components. It usually takes the form of an excess noise that increases in proportion to the current flowing through the component of interest. Evidence suggests that it is related to technological defects, since its effects have reduced as technology has improved. Manufacturers of devices such as op - amps specify 1/*f* noise by means of a

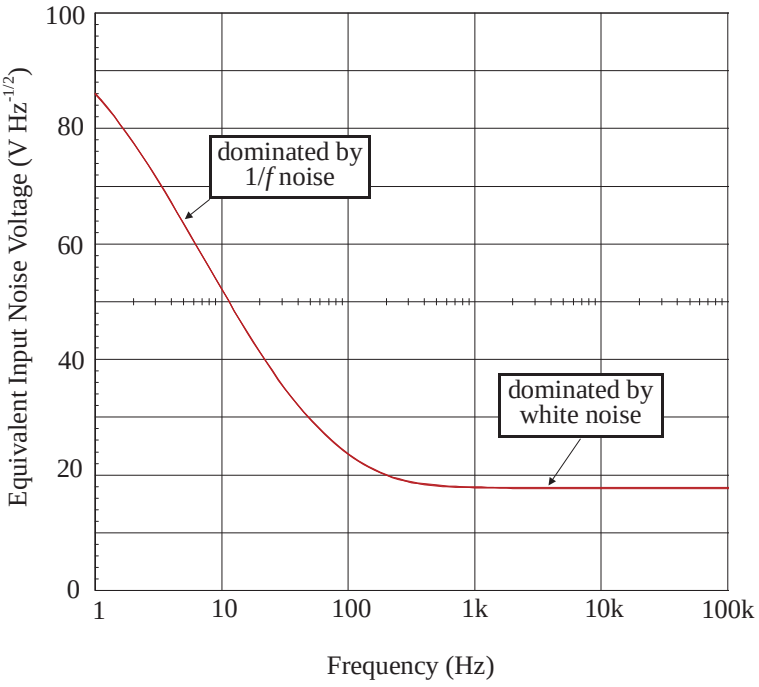


Figure 6

A typical relationship between equivalent input noise voltage and frequency as specified by op-amp manufacturers

graph of equivalent input noise voltage spectral density (V $Hz^{-½}$) against log (frequency) as shown in figure 6. Some manufacturers use a logarithmic vertical scale and others use a linear one. Figure 6 represents the sum of 1/*f* and white noise sources; at low frequencies behaviour is dominated by 1/*f* noise, while at high frequencies white noise dominates. At one particular frequency, 1/*f* and white sources contribute equally (in power terms) to the total noise and this occurs when $\sqrt{\overline{v_n^2}}$ has increased by a factor of 1.4 above its high frequency (white) value. This value of frequency is known as the "1/*f* corner frequency" and, for modern op-amps, it lies typically between 100Hz and 1000Hz.

1/*f* noise is described by the relationship $\overline{v_n^2}(f) = K/f^{\alpha}$ where *K* is a constant and α lies typically between 0.7 and 1.4, although it can occasionally be as high as 2. To work out the total noise over an interval $f_2 - f_1$ it is necessary to integrate $\overline{v_n^2}$ over that interval. Assuming $\alpha = 1$,

$$\overline{v_{nT}^2} = \int_{f_1}^{f_2} \overline{v_n^2}(f)df = \int_{f_1}^{f_2} \frac{K}{f}\,df = K \ln\left(\frac{f_2}{f_1}\right) \text{ V}^2$$

This result means that true 1/*f* noise has constant power per proportional bandwidth (f_2 / f_1), eg, constant power per decade or per octave, rather than the constant power per absolute bandwidth ($f_2 - f_1$) behaviour of white noise.

4 Noise Sources in Circuits

(i) Maximum Available Power

Maximum available power is the maximum noise power that can be transmitted from one resistor to another.

Consider a resistance R_S feeding a resistance *R*, as shown in figure 7. R_S is represented by its noise equivalent circuit consisting of a noise free R_S in series with a noise voltage generator. The questions to be answered are:

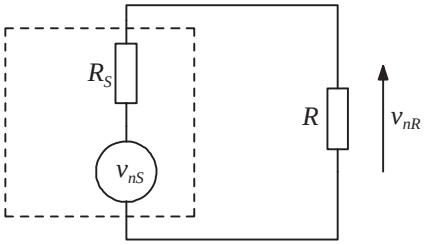


Figure 7

The circuit for the calculation of maximum available power.

a) What value of *R* will maximise the noise power delivered to *R* from R_S?

b) What is the maximum power transferred?

The answer to the first question is when $R = R_S$. The derivation of this standard result is straightforward and can be found in any textbook on circuit theory.

The answer to the second question can be found by evaluating the power delivered to *R* by v_{nS} when $R = R_S$. The voltage across *R* is given by:

$$v_{nR} = v_{nS}\,\frac{R}{R+R_S} = \frac{v_{nS}}{2} \text{ when } R = R_S .$$

The power dissipated in *R* is therefore

$$P_R = \frac{\overline{v_{nS}^2}}{4R_S} = \frac{4kTR_S}{4R_S} = kT \text{ W Hz}^{-1} \text{ or } P_R = kT\Delta f \text{ W}.$$

Note that the maximum available noise power is independent of the value of the source resistance, R_S, even though the noise power generated by R_S is proportional to its value. It is tempting to think that, because energy is being transferred from R_S to R , R will heat up. In fact, when the system is in thermal equilibrium, ie R and R_S at the same temperature as the environment, the same energy will flow from R to R_S as flows from R_S to R and there is no net energy transfer between the resistors. If however R_S was maintained at an elevated temperature with respect to R, there would be a net energy flow from R_S to R which would continue until the two resistors were at the same temperature. Thermal noise can be thought of as a way of moving energy around in order to achieve thermal equilibrium.

(ii) Addition of noise sources

Figure 8 shows two uncorrelated noise voltage sources. The term uncorrelated means that knowledge of the value of one source at an instant in time gives no information about the other source at any instant of time; in other words, the two sources are completely independent of one another.

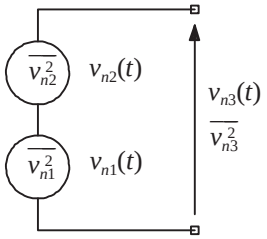


Figure 8

Noise sources in series

At any instant in time, the value of v_{n3} must be the sum of v_{n1} and v_{n2} and since that is true for all instants of time,

$$v_{n3}(t) = v_{n1}(t) + v_{n2}(t)$$

Although true, this relationship is not much help in quantifying the sum for the reasons outlined in section 2 (i). The noise is usefully quantified by its mean squared value so the question of interest is how does $\overline{v_{n3}^2}$ relate to $\overline{v_{n1}^2}$ and $\overline{v_{n2}^2}$? An answer to this question can be found as follows:

$$\overline{v_{n3}^2} = \overline{v_{n3}^2(t)} = \overline{(v_{n1}(t) + v_{n2}(t))^2} = \overline{v_{n1}^2(t)} + \overline{v_{n1}(t)v_{n2}(t)} + \overline{v_{n2}^2(t)}$$

But $\overline{v_{n1}^2(t)} = \overline{v_{n1}^2}$, $\overline{v_{n2}^2(t)} = \overline{v_{n2}^2}$ and, since $v_{n1}(t)$ and $v_{n2}(t)$ are uncorrelated, $\overline{v_{n1}(t)v_{n2}(t)} = \overline{v_{n1}(t)} \,.\, \overline{v_{n2}(t)}$. Both $\overline{v_{n1}(t)}$ and $\overline{v_{n2}(t)}$ are equal to 0, $\overline{v_{n1}(t)v_{n2}(t)} = 0$ and so

$$\overline{v_{n3}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}$$

In other words it is the mean square values of the noise voltage sources which must be added to find the overall noise from a number of sources: noise powers rather than noise voltages add linearly. This is the same as the procedure that must be followed to work out power dissipated by the sum of two sinusoids of different frequency.

(iii) Effects of an *RC* low pass circuit on white noise

Passing white noise through a low pass filter will give the noise a pink hue because the white noise spectral density will be modified by the transmission properties of the low pass filter; high frequency components of noise will suffer some attenuation. The exact nature of the pinkness will depend upon the nature of the low pass filter's power transmission response which is the square of the modulus of the filter's amplitude reponse. The circuit of interest here is a first order *RC* low pass circuit, although the same analytical approach can be used with any frequency dependent circuit. The first order low pass *RC* circuit occurs frequently in reality and the question "What is the total output noise voltage from such a circuit?" leads to an interesting result.

Consider the circuit of figure 9. The voltage v_{onT} is the r.m.s. value of the total output noise

obtained by integrating the spectral density at the output, $\overline{v_o^2}(\omega)$, over all frequency. The spectral density at the output is given by:

$$\overline{v_o^2}(\omega) = \overline{v_n^2}\left|\frac{1}{1+j\omega C R_S}\right|^2 = \frac{\overline{v_n^2}}{1+\omega^2 C^2 R_S^2}$$

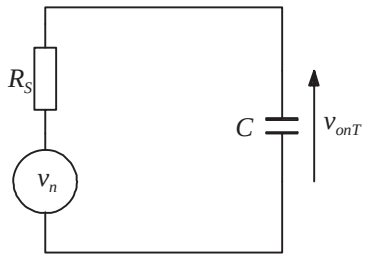


Figure 9

A low pass RC circuit fed by a white noise voltage source. The noise due to R is included in v_n

and thus, $\overline{v_{onT}^2} = \int_0^\infty \overline{v_o^2}(\omega) = \int_0^\infty \frac{\overline{v_n^2}\,df}{1+a^2f^2}$

where $a = 2\pi CR_S$.

This integral is solved by using the substitution $af = \tan x$.

Thus $(1+a^2f^2) \rightarrow (1+\tan^2 x) = \sec^2 x$ and $df \rightarrow \frac{\sec^2 x}{a}\,dx$, so the integral becomes:

$$\overline{v_{onT}^2} = \int_0^\infty \frac{\overline{v_n^2}\,df}{1+a^2f^2} = \int_0^{\frac{\pi}{2}} \frac{\overline{v_n^2}\sec^2 dx}{a\sec^2 x} = \overline{v_n^2}\int_0^{\frac{\pi}{2}} \frac{dx}{a} = \frac{\overline{v_n^2}}{4C R_S}\ \mathrm{V}^2$$ which, if $\overline{v_n^2}$ = the noise $\overline{v_{nS}^2}$ due to the resistor itself, $\overline{v_{onT}^2}$ becomes:

$$\overline{v_{onT}^2} = \frac{\overline{v_{nS}^2}}{4C R_S} = \frac{4kT R_S}{4C R_S} = \frac{kT}{C}\ \mathrm{V}^2$$ where T is the temperature of the resistor.

This result is interesting because it shows that when the noise in the circuit is the thermal noise associated with the resistor, the total noise voltage across the capacitor is independent of the resistor value. All real resistors must have some capacitance associated with them - of the order of 1pF for a typical 0.25W resistor - the total mean square noise voltage across a real resistor is given by kT/C V^2. Furthermore, although in principle noise free, a capacitor on its own could be considered as being in parallel with a resistance of value approaching infinity and one would therefore expect to find a total mean square noise votage of kT/C V^2 across its terminals.

(iv) Noise temperature

If the magnitude of the noise source in figure 9 is not what would be expected from the resistor on the basis of its temperature, ie if v_n consists of the resistor noise and some other noise source, it is possible, providing the source is white, to ascribe to the resistor an effective temperature T_e such that the rms noise voltage generated by the resistor alone at T_e accounts for v_n. The temperature T_e is known as the *noise temperature* of the resistor and is simply the notional temperature to which the resistor must be raised in order to account for all the white noise sources in series with it. Thus for the circuit of figure 9 the noise temperature of R_S is found by equating the total mean square noise voltage in series with R_S, including the noise generated by R_S at its actual temperature, to the mean square noise expected from the same resistance at some elevated temperature, T_e . Remembering that v_n in figure 9 includes all the noise sources in series with R_S , T_e is given by:

$\overline{v_n^2} = 4kT_eR_S$ V^2 or $T_e = \overline{v_n^2}/4kR_S$ K

Thus for a circuit such as that of figure 9, the total mean square noise voltage across C can be found for any magnitude of white noise source v_n by finding the noise temperature, T_e , of R_S and using T_e as the temperature term in kT/C .

Noise temperature is an important concept in communication system analysis and design and its application in that area is dealt with in the next section.

5 Noise in Systems

When dealing with the noise performance of a system, it is often impractical to analyse the system noise behaviour in terms of the individual sources of noise simply because of the number of noise sources involved. The approach usually taken when considering system noise is to represent observed noise behaviour as one or more equivalent noise generators associated with the system. This section describes the parameters used to describe noise effects in systems.

(i) Signal-to-Noise ratio

Consider the amplifier of figure 10. The input signal to noise ratio is defined as:

$$\frac{S_i}{N_i} = \frac{\text{input signal power}}{\text{input noise power}}$$

and the output signal to noise ratio as:

$$\frac{S_o}{N_o} = \frac{\text{output signal power}}{\text{output noise power}}$$

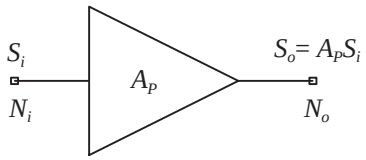


Figure 10

A signal amplifier with a power gain A_P

Signal-to-noise ratio is usually expressed in dB and since it is a power ratio, dB are found by taking 10log(S/N). It can be measured at any point in a system and is essentially a measure of signal quality at that point in the system.

Although the signal to noise ratio will vary throughout a real system, of itself it gives no information about the noise performance of the system. Indeed it gives no information about the magnitude of the noise unless the signal level at which it was measured is specified. To identify the noise performance of a system, the signal to noise ratio at input and output must be compared.

(ii) Noise factor

For a system such as that of figure 10, the noise factor, F, is defined as:

$$F = \frac{\text{signal to noise ratio at the input}}{\text{signal to noise ratio at the output}} = \frac{S_i/N_i}{S_o/N_o} \qquad \textbf{(5.1)}$$

If the power gain of the system is A_P, as in figure 10, this relationship can be written:

$$F = \frac{N_o}{A_PN_i} = \frac{\text{noise power at the output of the real amplifier}}{\text{noise power that would appear at the amplifier output if it were perfect}} \qquad \textbf{(5.2)}$$

This expression for noise factor is very useful for working out the noise factor of systems and

will be used later to investigate the noise behaviour of multistage impedance matched amplifiers such as those that might be found in satellite or radar receivers. The noise power at the output of an impedance matched system is simply the available noise power at the input multiplied by the power gain.

For low frequency unmatched circuits, such as transistor and operational amplifier based amplification circuits, the concept of power gain is often not very useful. It is, however, possible to work in terms of mean-square voltages rather than powers because at a single system node the ratio of mean square voltages is the same as the ratio of powers. When working with mean square voltage quantities the system gain must be expressed in terms of the square of its voltage gain and the input noise is the mean square noise voltage appearing at the input because of the source circuit. The significance of noise factor in low frequency unmatched systems depends on the nature of the system; minimising noise factor in audio amplifiers, for example, does not necessarily lead to an amplifier with the most desirable noise properties.

The output noise, N_o, can be written as the sum of two components; the amplified input noise and the noise added by the amplifier. Thus $N_o = A_P N_i + N_A$, where N_A is called the "added noise" contributed by the amplifier. The expression describing F can thus be developed to:

$$F = \frac{N_o}{A_P N_i} = \frac{A_P N_i + N_A}{A_P N_i} = 1 + \frac{N_A}{A_P N_i} \qquad \textbf{(5.3)}$$

If $N_A = 0$ the amplifier is ideal and $F = 1$. For an impedance matched system, N_i is the available input noise power and F can be written as:

$$F = 1 + \frac{N_A}{A_P N_i} = 1 + \frac{N_A}{A_P kT\Delta f} \qquad \textbf{(5.4)}$$

(iii) Noise figure

The noise figure of a system component is simply the noise factor expressed in terms of dB, thus:

$$\text{Noise Figure, } NF = 10\log F \text{ dB} \qquad \textbf{(5.5)}$$

It is usually the noise figure of impedance matched components, such as RF amplifier blocks, that is specified by manufacturers. In order to perform calculations using this information it is usually necessary to convert the noise figure specification into a noise factor.

(iv) Noise factor of a two stage impedance matched system.

Many analogue systems consist of a cascade of units such as a series of RF amplifier modules in a radar receiver system or a number of sequential amplification stages in a typical audio system. From a design point of view, it is important to know how each part of a system contributes to the overall system noise performance. The analysis that follows considers a combination of two amplifiers in series in an impedance matched system and works out the noise factor of the combination in terms of the noise factor of each element in the cascade. The results developed do not translate directly to the unmatched systems typically found at low frequency because in unmatched systems the input noise is not the available noise power, but the general principals revealed are true for all cascades.

Figure 11 shows two amplifiers in cascade with power gains of A_{P1} and A_{P2} respectively. The noise factors, F_1 and F_2, of the amplifiers, and the available input noise, N_I, are given by:

$$N_I = kT\Delta f$$

$$F_1 = 1 + \frac{N_{A1}}{A_{P1} kT\Delta f} \qquad \textbf{(5.6)}$$

$$F_2 = 1 + \frac{N_{A2}}{A_{P2} kT\Delta f} \qquad \textbf{(5.7)}$$

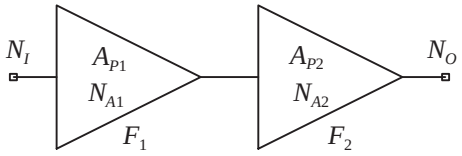


Figure 11
Two impedance matched amplifiers in cascade

To work out the noise factor of the system it is necessary to work out the noise power at the output of the real (noisy) system and divide it by the noise power that would appear at the output of an ideal system. The output noise from the real system has three components; that due to the available input noise which is amplified by both amplifiers, that due to the noise added by amplifier 1 which is amplified by amplifier 2 only and that due to the noise added by amplifier 2. The added noise powers associated with the two amplifiers can be found in terms of noise factor by rearranging equations (5.6) and (5.7). The three contributions are:

(i) output noise component due to the available input noise, N_I,

$$N_O\,(i) = A_{P1}\,A_{P2}\,N_I = A_{P1}\,A_{P2}\,kT\Delta f$$

(ii) output noise component due to the noise added by amplifier 1, N_{A1},

$$N_O(ii) = A_{P2}\,N_{A1} = A_{P2}\,(F_1 - 1)\,A_{P1}\,kT\Delta f$$

(iii) output noise component due to the noise added by amplifier 2, N_{A2},

$$N_O(iii) = N_{A2} = (F_2 - 1)\,A_{P2}\,kT\Delta f$$

The total output noise from the real amplifier is thus,

$$N_O\,(i) + N_O\,(ii) + N_O\,(iii) = A_{P1}\,A_{P2}\,kT\Delta f + A_{P1}\,A_{P2}\,(F_1 - 1)\,kT\Delta f + (F_2 - 1)\,A_{P2}\,kT\Delta f$$

$$= A_{P1}\,A_{P2}\,kT\Delta f\left(F_1 + \frac{(F_2 - 1)}{A_{P1}}\right)$$

The noise output from the ideal amplifier is simply $N_O(i)$ since in this case N_I exists but N_{A1} and N_{A2} are zero. The system noise factor is thus:

$$F = \frac{A_{P1}\,A_{P2}\,kT\Delta f\left(F_1 + \dfrac{(F_2 - 1)}{A_{P1}}\right)}{A_{P1}\,A_{P2}\,kT\Delta f} = F_1 + \frac{(F_2 - 1)}{A_{P1}} \qquad \textbf{(5.8)}$$

This result is extremely important for system designers wishing to minimise the effects of noise in a system. There are two major conclusions to be drawn from it:-

- The system noise factor is at least equal to the noise factor of the first stage so first stage noise performance is critical.
- The noise factor of the second stage is reduced by a factor equal to the first stage power gain before it adds to the noise figure of the first stage.

This means that the first stage dominates the noise performance of the system and should have low added noise and high power gain. A large fraction of the total design effort in noise critical systems goes into the first stage design. For systems with more than two stages a very similar analytical procedure can be followed to yield similar results. For a three stage system a similar process to that resulting in equ. (5.8) gives a system noise factor of

$F = F_1 + \dfrac{(F_2 - 1)}{A_{P1}} + \dfrac{(F_3 - 1)}{A_{P1}\,A_{P2}}$. Again, the first stage dominates and if the first stage has high gain the contributions of subsequent stages to noise factor are small for the second stage and usually negligible for the third.

In unmatched systems such as audio amplifiers the same principles apply. The first stage needs low noise because its noise performance dominates that of the whole system and it needs a high gain to ensure that the noise contributions from subsequent stages are insignificant. In all forms of electronic system dealing with very small signals the term "low noise front end" crops up and this simply reflects the importance of first stage noise. In some systems noise performance is so critical that first stages are cooled to reduce the added noise contribution of the first stage and hence improve the noise performance of the whole system.

(v) Noise temperature of a system element

Communications engineers often use the concept of noise temperature to describe the noise performance of impedance matched elements in a communication system. Figure 12a shows a real (noisy) amplifier with an added noise N_A. In figure 12b, the added noise has been taken out of the amplifier and is instead represented by an equivalent input noise source.

The input noise, N_I, is given by the available noise at the ambient temperature, T_A, because the Thevenin equivalent source resistance is equal to the input resistance of the amplifier by virtue of the system being impedance matched. Thus $N_I = kT_A\,\Delta f$. The equivalent input noise

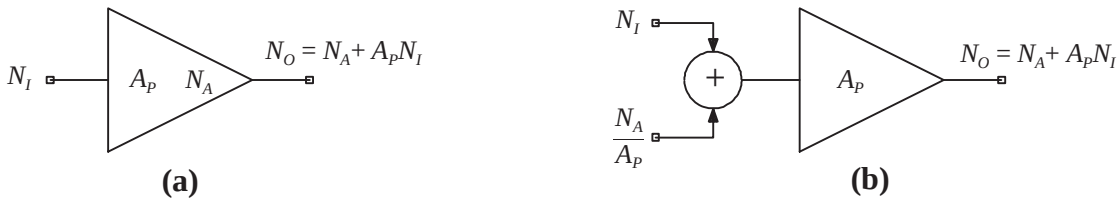


Figure 12

(a) *A noisy amplifier.* **(b)** *A noise equivalent circuit of (a) where the noise is represnted by an equivalent input generator.*

source, N_A/A_P, is also assumed to emanate from a matched resistance but its magnitude is not generally equal to the available noise at the ambient temperature. Thus an effective temperature, T_E, the amplifier noise temperature, must be ascribed to the matched resistance generating the equivalent input noise such that $\dfrac{N_A}{A_P} = kT_E\,\Delta f$. If the amplifier is perfect from a noise point of view $T_E = 0$K but if N_A is finite, $T_E > 0$. When the amplifier added noise is expressed in terms of an equivalent temperature in this way, the noise factor of the amplifier can also be expressed in terms of temperatures:

$$F = \frac{N_O\,(\text{real})}{N_O\,(\text{ideal})} = \frac{N_A + A_P\,N_I}{A_P\,N_I} = \frac{A_P\,kT_E\Delta f + A_P\,kT_A\Delta f}{A_P\,kT_A\Delta f} = 1 + \frac{T_E}{T_A} \qquad \textbf{(5.9)}$$

The noise temperature gives a direct idea of the magnitude of noise power cotributed by the system element compared to the available noise power. For example, an element with a noise temperature of 300K would contribute an added noise at the output equal to that due to the input noise. Some typical noise temperatures of elements in satellite television receivers are:

Low noise r.f. amplifier 150K

Mixer	850K
IF amplifier	400K

6 Equivalent Input Noise Generators

Representing the noise behaviour of a system by modelling the system added noise as some form of source at the input is an attractive approach for a number of reasons.

- It offers a simple representation of the noise performance of an otherwise complex systems.
- It offers a standard approach to the representation of noise sources which is convenient for comparison of noise specifications.
- It enables a standard analytical approach to system noise assessment.
- The equivalent input parameters are relatively easy to measure.

(i) The equivalent circuit

The strategy of representing system added noise by introducing at the system input an impedance matched resistive noise source at an appropriate temperature is not suitable for unmatched systems. For unmatched systems the added noise is instead represented by two generators, a series voltage generator and a shunt current generator. Two generators are necessary in order to achieve a model of system noise that is independent of the value of source impedance. In principle each system input should have equivalent generators associated with it. In systems such as operational amplifiers, the magnitude of the equivalent input generators is substantially independent of local circuit conditions but for simpler systems such as BJTs or FETs the equivalent input generator magnitudes are dependent on bias conditions.

Figure 13 shows an amplifier with a voltage gain G and added noise represented by the equivalent input noise generators, v_n and i_n. The input resistance, r_i (which can be regarded as noise free since any noise it generates is included in v_n and i_n) can usually be neglected if its value is large compared with R_S.

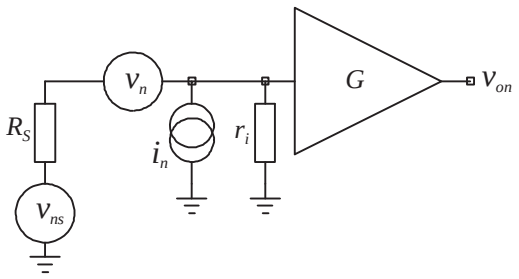


Figure 13

The equivalent input noise generators, v_n and i_n, account for all the noise added by the amplifier to any passing signal.

(ii) Quantifying the equivalent input noise generators

The equivalent input generators can be quantified by measuring the output noise voltage for different values of R_S. The measurement should be done using a true rms voltmeter with a known noise bandwidth, Δf.

If R_S is 0Ω, the voltmeter reading will be $v_{on} = \left(G^2 \overline{v_n^2} \Delta f\right)^{1/2}$, ie the equivalent input current generator will have no effect and v_n is easily determined. A second measurement with a suitable finite R_S enables the equivalent input current generator to be quantified. With finite R_S,

$$\overline{v_{on}^2} = G^2\left[\overline{v_n^2}\left(\frac{r_i}{R_S+r_i}\right)^2 + \overline{v_{ns}^2}\left(\frac{r_i}{R_S+r_i}\right)^2 + \overline{i_n^2}\left(\frac{r_i R_S}{R_S+r_i}\right)^2\right]\Delta f$$
$$= G^2\left(\frac{r_i}{R_S+r_i}\right)^2\left[\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_n^2}R_S^2\right]\Delta f \qquad \textbf{(6.1)}$$

The only unknown in equation (6.1) is i_n. If r_i is very large and ill defined, as it might be in the case of a FET input op-amp, a finite R_S is necessary in order to create a well defined input voltage due to i_n. If r_i is well defined in value, R_S can be omitted and equation (6.1) simplifies to $v_{on} = \left(G^2\,\overline{i_n^2}r_i^2\,\Delta f\right)^{1/2}$.

(iii) Optimum source resistance

Consider the amplifier of figure 13, with a voltage gain G, a noise free input resistance r_i, equivalent input noise voltage and current generators v_n and i_n and a noisy source resistance R_S. The noise factor of the system can be worked out using the relationship of equation (5.2),

$$F = \frac{N_o}{A_P N_i} = \frac{N_{o\,real}}{N_{o\,ideal}}$$

The output noise from the real amplifier is given by equation (6.1):

$$N_{o\,real} = \overline{v_{onr}^2} = G^2\left[\overline{v_n^2}\left(\frac{r_i}{R_S+r_i}\right)^2 + \overline{v_{ns}^2}\left(\frac{r_i}{R_S+r_i}\right)^2 + \overline{i_n^2}\left(\frac{r_i R_S}{R_S+r_i}\right)^2\right]$$
$$= G^2\left(\frac{r_i}{R_S+r_i}\right)^2\left[\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_n^2}R_S^2\right]$$

and since v_n and $i_n = 0$ for an ideal amplifier, that from its ideal equivalent is:

$$N_{o\,ideal} = \overline{v_{oni}^2} = G^2\,\overline{v_{ns}^2}\left(\frac{r_i}{R_S+r_i}\right)^2$$

The system noise factor is therefore:

$$F = \frac{\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_n^2}R_S^2}{\overline{v_{ns}^2}} = \frac{\overline{v_n^2} + 4kT\,R_S + \overline{i_n^2}R_S^2}{4kT\,R_S} = 1 + \frac{\overline{v_n^2}}{4kT\,R_S} + \frac{\overline{i_n^2}R_S}{4kT} \qquad \textbf{(6.2)}$$

Equation (6.2) has one term directly proportional to R_S and one inversely proportional to R_S so F will become very large for the extremes of R_S very large or R_S very small and there will be a minimum value of F for some intermediate value of R_S. To find the value of R_S that minimises F, it is necessary to differentiate equation (6.2) and equate the result to zero. F is minimised, therefore, when

$$\frac{dF}{dR_S} = -\frac{\overline{v_n^2}}{4kT\,R_S^2} + \frac{\overline{i_n^2}}{4kT} = 0 \text{ or when } R_S = \frac{v_n}{i_n}. \qquad \textbf{(6.3)}$$

It is important to realise that it is noise factor that has been minimised here, not the output noise voltage. In some applications it may not be desirable to minimise F in this way. Minimising F minimises the degradation in signal to noise ratio caused by the passage of the signal through the amplifier.

The source resistance is usually not adjustable so other steps have to be taken to achieve the

minimum F condition. One method is to connect several amplifiers in parallel and another is to use impedance matching transformers.

(iv) Parallel amplifiers

Figure 14 shows N amplifiers in parallel fed by a single source with a Thevenin equivalent resistance R_S. The circuit is simplified in that r_i is assumed infinite in each amplifier; the inclusion of an r_i would lead to more terms in the intermediate parts of the analysis but the conclusions would be the same as those that follow here. Each amplifier output is potentially divided between its own R_O and the N-1 other R_Os in parallel, that is by a factor of N, before contributing to the overall output, v_{onT}. Noise at the amplifier outputs arising from a single input source adds linearly whereas noise from independent sources must add as mean squared quantities.

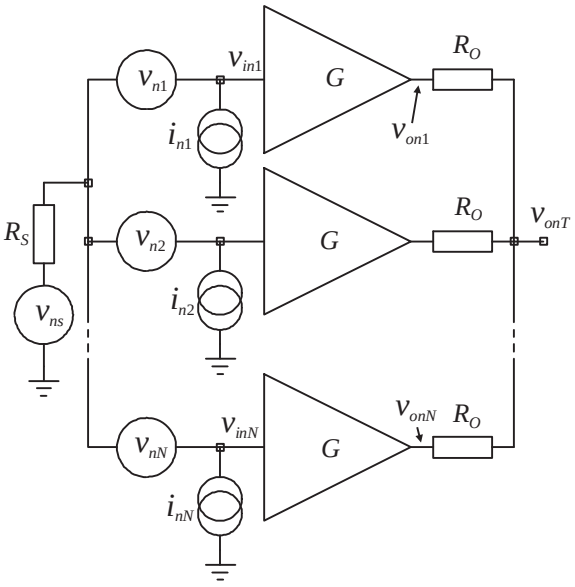


Figure 14
Identical amplifiers connected in parallel to achieve optimum source impedance matching.

The component of the output at any amplifier due to v_{ns}, the thermal noise of the source resistance, is $v_{on} = v_{ns}G$. Since vns appears at each amplifier input, these output contributions add linearly and the component of v_{onT} due to vns is $v_{onT} = Nv_{ns}G/N = v_{ns}G$.

Each of the equivalent input voltage sources affects only its own amplifier so the output at any amplifier due to its v_n is $v_{on} = v_nG$ and the component of the overall output due to each vn is $v_{onT} = v_n\,G/N$. Since each v_n is independent, their contributions must add as mean squared quantities so the v_{onT} due to all v_n is given by $\overline{v_{onT}^2} = \dfrac{\overline{v_n^2}\,G^2}{N^2}N = \dfrac{\overline{v_n^2}\,G^2}{N}$.

Each equivalent input current source affects each amplifier equally; the voltages appearing at each output due to any one current source must be combined linearly while the contributions from the different sources must be combined as mean squared additions. The overall output due to a single current source is $v_{onT} = i_n\,R_S\,G$ since i_n flowing through R_S creates a voltage which behaves in the same way as v_{ns}. The contributions from the N current sources must be added as mean squared contributions to give a total v_{onT} due to current sources of $\overline{v_{onT}^2} = N\ \overline{i_n^2}R_S^2\,G^2$.

The overall output noise voltage, including all contributions, is given by,

$$\overline{v_{onT}^2} = \overline{v_{ns}^2}\,G^2 + \frac{\overline{v_n^2}\,G^2}{N} + N\ \overline{i_n^2}R_S^2\,G^2. \qquad \textbf{(6.4)}$$

Using the same process as that which led to equations (6.2) and (6.3) above the noise factor of the parallel system can be shown to be:

$$F = 1 + \frac{\overline{v_n^2}}{4kT\,R_S\,N} + \frac{\overline{i_n^2}R_S\,N}{4kT}, \text{ and this is minimum when } R_S = \frac{v_n}{N\ i_n} \qquad \textbf{(6.5)}$$

Note that v_{ns} is in the same position in the circuit as a signal generator would be so equation (6.4) indicates that the signal gain of the parallel arrangement of figure 14 is the same as a single

amplifier. Note also that equation (6.5) indicates that the parallel amplifier approach is only useful for cases where the source resistance is smaller than the optimum value required for a single amplifier. The parallel approach tends to be used with transistor amplifiers rather than operational amplifiers. The output node in the case of transistors consists of *N* Norton equivalent circuits connected in parallel, but Norton to Thevenin transformations on the transistor output circuits would yeild a similar circuit to figure 14, and give very similar results.

(v) Transformer matching

The second technique used for presenting an amplifier with the source resistance that will minimise its noise factor involves the use of a transformer as an impedance changer. Figure 15 shows a transformer coupled amplifier together with its equivalent circuit. The transformer has a turns ratio of 1:*n* with the *n* being on the amplifier side. The circuit of figure 15(b) is the same

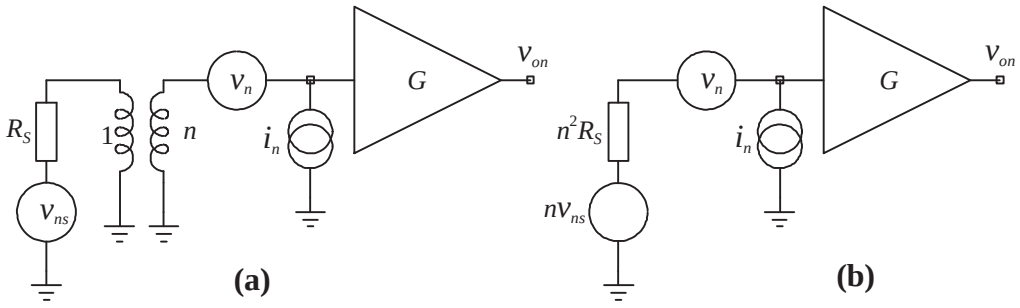


Figure 15

(a) *A transformer coupled input stage and* **(b)** *its equivalent circuit*

as figure 13 with the exception that r_i does not exist so the analysis of section 6(iii), with appropriate modification to symbols, can be used here. Thus, R_S becomes n^2R_S and v_{ns} becomes nv_{ns} to give:

$$F = \frac{\overline{v_n^2} + n^2\,\overline{v_{ns}^2} + \overline{i_n^2}n^4R_S^2}{n^2\,\overline{v_{ns}^2}} = \frac{\overline{v_n^2} + 4kT\,n^2R_S + \overline{i_n^2}n^4R_S^2}{4kT\,n^2R_S} = 1 + \frac{\overline{v_n^2}}{4kT\,n^2R_S} + \frac{\overline{i_n^2}n^2R_S}{4kT} \qquad \textbf{(6.6)}$$

In this case R_S is fixed but since *n*, the turns ratio, can be controlled by design, equation (6.6) must be differentiated with respect to *n* to find the value of *n* that minimises *F*. What is actually happening is that as n changes, the source resistance presented to the amplifier changes. The appropriate value of *n* could equally well be found by evaluating the optimum source resistance for the amplifier of interest and then working out the turns ratio needed to transform the actual source resistance into the optimum value. By either method, *F* is minimised when:

$$n = \left(\frac{v_n}{i_n R_S}\right)^{1/2}$$

This approach to optimising noise performance is commonly used in audio systems to match low impedance microphones to low noise amplifiers.

7 Noise in Operational Amplifiers

Operational amplifier ICs, op-amps, are relatively sophisticated analogue subsystems and it would be impractical to evaluate their noise performance by examining each separate noise source within the IC. Instead it is the macroscopic noise performance of the whole amplifier that is modelled by abstracting all internal noise sources and representing them as equivalent input noise generators. Much the same approach is taken to the modelling of dc offset effects.

(i) Op-amp noise equivalent circuits.

Op-amps are usually used in impedance unmatched systems so equivalent input noise generators are used to model the op-amp noise behaviour. Three equivalent circuits are commonly used and these are shown in figure 16. Figure 16(a) is the most detailed of the three circuits, using two noise generators at each input. This model must be used in situations where the op-amp input current is too high to be ignored - in other words when the input resistance is low. Providing the input resistance of the op-amp is very high - so high that currents flowing into the inputs are negligible in comparison to other currents in the circuit - only one equivalent input voltage source placed in series with either the inverting or non-inverting input of a standard op-amp is necessary and the model of figure 16(b) results. Since the assumption of very high input resistance is valid for most modern op-amps, the single voltage source model is the one which will be followed here. A third model, shown in figure 16(c), has a single current source connected between the inputs. Connecting the current noise generator between the inputs models the current noise in the two inputs as correlated and thus, at any instant, the noise current in one input is minus that in the other. Note that in the models of figures 16(b) and 16(c) the equivalent input voltage generator can be put in series with either input without affecting the model behaviour.

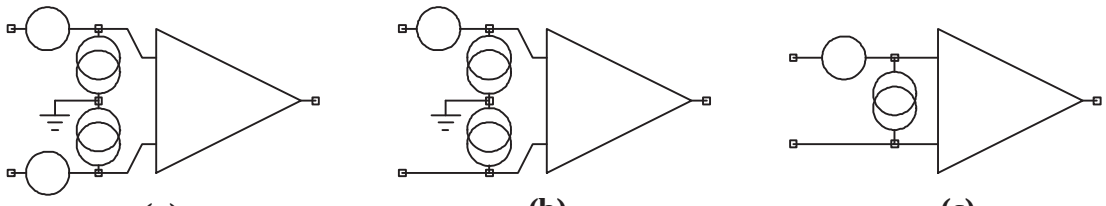


Figure 16

Three noise models for op-amps. The + and - inputs have not been marked because it makes no difference from a noise point of view which is which. **(a)** *The most accurate of the three but more accurate than necessary in most cases.* **(b)** *Suitable for amplifiers with very high input resistance - ie, most op-amps.* **(c)** *Sometimes used for op-amps but makes the two equivalent input noise currents coherent.*

(ii) Noise analysis of op-amp circuits

Figure 17a shows the op-amp noise equivalent circuit and figure 17b shows an op-amp circuit with only noise sources included - if a noise analysis is being performed, signal sources should be replaced by their Thevenin equivalent impedances. For an inverting amplifier the signal source would be inserted in series with R_1 and for a non-inverting amplifier the signal source would be connected in series with R_3; the noise equivalent circuit is the same for both cases. Since the objective here is a noise analysis all other aspects of amplifier performance are assumed to be ideal. Analysis of figure 17b gives:-

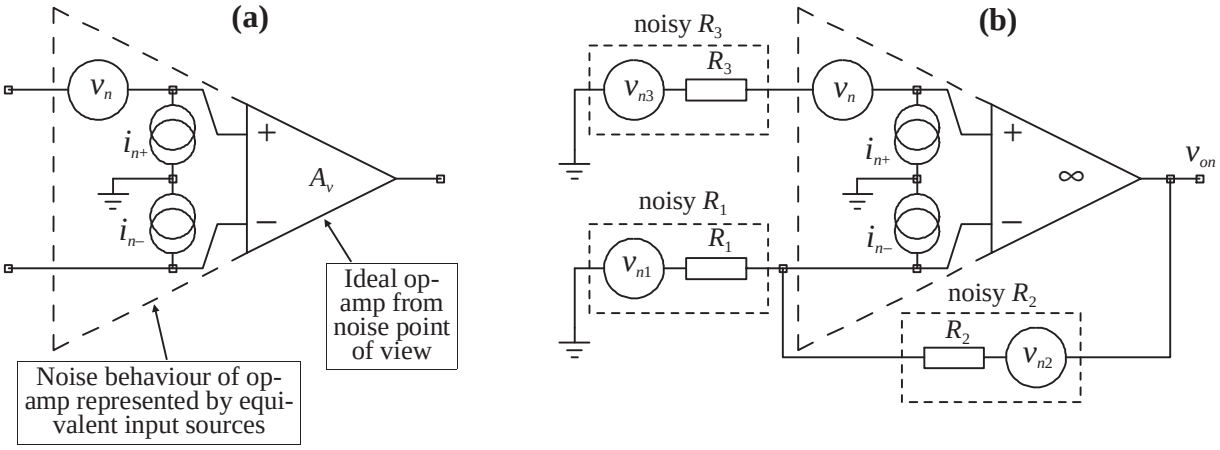


Figure 17

(a) *The noise equivalent circuit of an op-amp.* **(b)** *The noise equivalent circuit appropriate for inverting and non-inverting amplifier circuit connections.*

$$\overline{v_{on}^2} = G^2\left[\overline{i_{n+}^2}R_3^2 + \overline{i_{n-}^2}\left(\frac{R_1R_2}{R_1+R_2}\right)^2 + \overline{v_n^2} + \overline{v_{nf}^2} + \overline{v_{n3}^2}\right] \qquad \textbf{(7.1)}$$

where

G = closed loop gain, $(R_1+R_2)/R_1$
$\overline{v_{n3}^2}$ = noise due to R_3, $4kTR_3$ V^2 Hz^{-1}
$\overline{v_{nf}^2}$ = noise due to the feedback resistors R_1 and R_2, $4kTR_1R_2/(R_1+R_2)$ V^2 Hz^{-1}
$\overline{v_n^2}$ = op-amp's equivalent input noise voltage generator
$\overline{i_{n+}^2}$ = op-amp's equivalent input noise current generator at the non-inverting input
$\overline{i_{n-}^2}$ = op-amp's equivalent input noise current generator at the inverting input

The derivation of equation (7.1) provides an excellent exercise in the analysis of circuits with multiple uncorrelated noise sources. The easiest way of arriving at the solution is probably to use the superposition principle to consider the output voltage due to each individual source in turn and then sum the squares of each output component in order to arrive at the total output voltage. This approach also has the advantage that it is easy to compare the relative magnitudes of contributions from various parts of the circuit and hence identify any problem areas. Note that the non-inverting closed loop gain has been taken as a factor from each term in equation (7.1). Since it is the non-inverting closed loop gain that operates on noise sources at the input, irrespective of the type of circuit connection (ie, inverting or non-inverting), the non-inverting gain is often called the "noise gain".

Inspection of equation (7.1) will tell the op-amp circuit designer whether it is possible to affect the noise performance of the circuit by careful design. Consider the terms as they appear in equation (7.1):

(i) The first term is due to the voltage developed across R_3 by i_{n+}. If R_3 is made equal to zero, the noise contribution due to i_{n+} disappears. Remember, though, that R_3 may be there to minimise offset effects or alternatively it may be a Thevenin equivalent source resistance, so it may not be sensible or possible to change its value. Under such circumstances the magnitude of the first term can only be reduced by choosing an op-amp with a very low i_{n+}.

(ii) The second term is due to the voltage developed across the parallel combination of

R_1 and R_2 by i_{n-}. Choice of an op-amp with a low i_{n-} will reduce this term, as will a reduction in the value of the parallel combination of R_1 and R_2. R_1 and R_2 determine the circuit gain so the ratio of their values is defined by the gain requirement. A high value of gain means $R_2 \gg R_1$ and then the parallel combination approximates to R_1. The lowest values that can be used may be limited by offset considerations or by the acceptable magnitude of signal current drawn through R_1 and R_2; the output current capability of an op-amp is limited and signal current wasted down the feedback path is not available for driving a load.

(iii) The third term is due to the op-amp's equivalent input noise voltage generator. There is nothing that can be done to reduce this component except choosing an op-amp with a low value of v_n.

(iv) The fourth term is caused by the thermal noise generated in the feedback resistors, R_1 and R_2. As for term (ii), R_1 and R_2 are effectively in parallel and their combined value approximates to R_1 if the circuit gain is high. Making the parallel combination as small as possible will minimise the noise contributed by the feedback resistors but the constraints are the same as for term (ii).

(v) The fifth term is due to the thermal noise generated in R_3. It can be reduced by reducing R_3. Considerations limiting the smallness of R_3 are discussed in term (i)

A general purpose op-amp will have an equivalent input noise voltage generator of around 20nV $Hz^{-1/2}$ and at room temperature the resistance that will generate a thermal noise of the same value is around 24kΩ. In many cases it is possible to reduce R_3 and the parallel combination of R_1 and R_2 to values well below 24kΩ and thus ensure that terms (iv) and (v) make a small contribution to total noise. Op-amps with FET input devices have equivalent input current noise generators of the order of 0.01pA $Hz^{-1/2}$, as opposed to the significantly larger 0.4 pA $Hz^{-1/2}$ typical of their BJT input counterparts, and hence represent a good choice for reducing terms (i) and (ii).

Wide bandwidth op-amps tend to have lower equivalent input noise voltage generators and higher equivalent input noise current generators than general purpose op-amps and there are other devices specially designed to minimise noise. Remember though that a device designed to minimise one undesirable effect may well be worse than average in some other respects.

(iii) A simplified op-amp noise model

If a circuit such as figure 17b has been designed such that the noise associated with the feedback resistors has been made negligible, that is terms (ii) and (iv) in equation (7.1) have been made small compared to the other noise sources in the circuit, and the circuit connection is non-inverting, the simplified equivalent circuit of figure 18 can be used. The circuit of figure 18 is also appropriate for the small number of special amplifiers that have built in dc bias on the non-inverting input and built in feedback components. Such special amplifiers are often optimised for low noise performance and are typically intended for amplification in ac coupled environments such as audio systems, where designer access

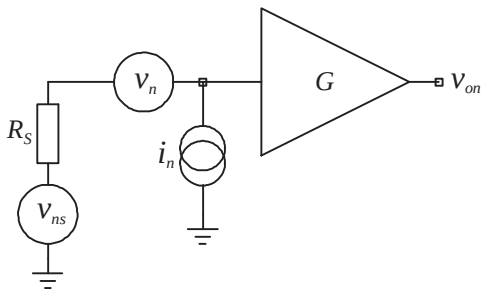


Figure 18
A simplified amplifier noise model

to differential inputs is not usually essential.

The gain of the amplifier is now that defined by the manufacturers or by the feedback. Any noise introduced by the feedback components is either negligible by design or included in the equivalent input generators, v_n and i_n. If the amplifier has an input resistance, which may or may not be the case, its effect is to potentially divide the voltage sources and provide a parallel path for current sources and these effects must be taken into account when calculating output noise. The input resistance, if it exists, will be noise free since its noise contribution will be accounted for by the equivalent input generators.

8 Concluding Comments

This handout was intended to provide you with an introductory working knowledge of noise and how to handle it. The physical processes that give rise to the noise and the derivations of the expressions describing the magnitudes of thermal noise and shot noise have not been mentioned. The sources considered have all been independent and hence uncorrelated although many situations exist where the sources are partially correlated. BJTs and FETs have been mentioned in passing but the details of their noise behaviour have not been discussed. The list below provides some sources of further information on noise:

W.M. Leach: "Fundamentals of Low-Noise Analog Circuit Design", IEEE Proc. **82**, pp 1515 - 1538, Oct 1994. (*This is a tutorial paper concentrating on device modelling and circuit design techniques for low noise*.)

C.D. Motchenbacher and J.A. Connelly: "Low noise Electronic System Design", Wiley, 1993, ISBN 0-471-57742-1. (*A general book about noise in circuits and systems.)*

A. Van Der Ziel: "Noise in Solid State Devices and Circuits", Wiley, 1986. (*Van Der Ziel has written many titles on noise; this is one of the more recent ones. The books tend to be written from a solid state rather than a system viewpoint.*)

D.A. Bell: "Electrical Noise", Van Nostrand, 1960. (*Concentrates on physical mechanisms.*)

Handouts

(The Lecture Slides)



EEE225: Analogue and Digital Electronics

Lecture I

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This Lecture

1. Introduction
   - Aims & Objectives
2. Books
3. Review of Transistor Operation
   - Output Characteristics
   - Transfer, Mutual or Transconductance (g_m) Characteristics
   - Small Signal Model
4. One Transistor Circuits
   - Common Emitter Amplifier without Degeneration
   - Common Emitter Amplifier with Degeneration
5. Review
6. Bear

Aims & Objectives

To continue our description of the operation of analogue circuits.

These lectures cover three topics,

1. Introduction to some common analogue building blocks
2. Frequency dependence in operational amplifier circuits
3. Introduction to electronic noise in circuits

Approximately 4-5 lectures on each topic.

Many things not included: (C)MOS, second & higher order circuits, translinear circuits, oscillators, full discussion of feedback, SFDs, current mode circuits, practical considerations (board or IC layout) etc. etc.

How is this different from the other parts of EEE225?

Neil Powell's part of the course develops a description of digital building blocks and design techniques.

John David's part of the course continues the description of semiconductor devices.

In this part of the course the objective is

to broaden our understanding of how to make electronic devices work in circuits especially in integrated circuits.

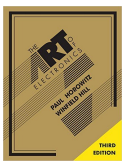
Can I use what I know about electron device operation and circuit design to analyze and design ICs and discrete circuits.

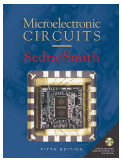
What to expect...

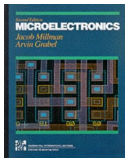
- Slides
- Handouts in lectures
- Handouts available on-line
- Videos of the lectures available on-line
- Biscuits (sometimes)
- Problem sheets & classes, Wednesday 1200 – 1300
- Going to the Library...
- Still need Help? Email Me.

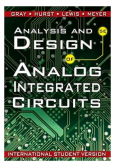
I'm assuming familiarity with the content of EEE117 and EEE118 and mathmatics modules. If you've not seen EEE118 or need a refresher look for the videos on YouTube `https://goo.gl/FK5Ded`.

Books





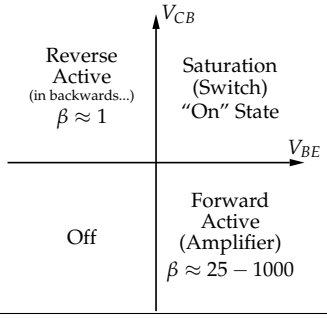




- Horowitz, P. and Hill, W., "The Art of Electronics", Cambridge University Press, 3rd ed., 2015.
- Sedra, A. S., and Smith, K. C., "Microelectronics", Oxford University Press, 5th ed., 2006.
- Millman, J., and Grabel, A., "Microelectronics", McGraw-Hill Higher Education, 2nd ed. 1988.
- Grey, P. *et al.*, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 5th ed. 2009.

BJT Modes of Operation

There are four possible modes of operation where each of the two junctions is either forward or reverse biased.



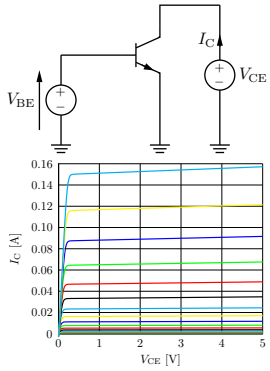
- Forward active is used for amplification B-E forward biased, C-B reverse biased.
- Saturation is a "switch" in the on state B-E and C-B forward biased.
- Off ... All reverse biased
- Reverse active is not used but could make a poor amplifier C-B and B-E junctions exchanged.

BJT Modes of Operation II

- The forward active region provides amplification of voltage and/or current (both means power amplification ($P = IV$)).
- In the saturation region the transistor appears like a switch which is turned on.
- In the 'off' region the transistor appears like a switch which is turned off.
- The reverse active region is used when the BE and CB junctions are accidentally exchanged (transistor in the circuit backwards). Performance is poor c.f forward active region as transistor designers adjust doping densities and region widths to optimise performance in other regions.

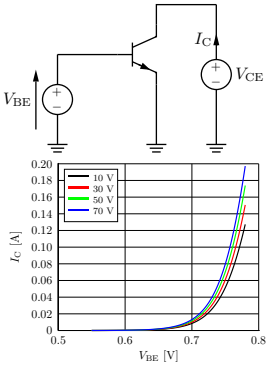
Note: some transistors are designed for amplification (linear) use others are designed for switching use. All transistors can perform both functions but the design of "switching" transistors is optimised for switching applications. Likewise for "amplifier transistors".

Output Characteristics



A family of curves showing effect on the output V_{CE} and I_C as a function of the input V_{BE} (or I_B). When V_{CE} is small the transistor is in saturation both BE and CB junctions forward biased (transistor switched "on") (left of graph). When V_{BE} is too small to cause I_C to rise above the leakage current level, the transistor is off ($y \approx 0$ on the graph). Forward active region is indicated by nearly parallel characteristics.

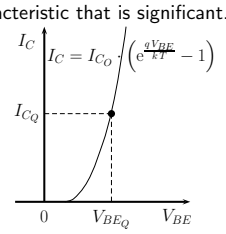
Transfer Characteristics



The transfer characteristic relates the controlling voltage (V_{BE}) to the controlled parameter I_C. V_{BE} is related to I_C for a BJT by $I_C = I_S \left(exp \left(\frac{q V_{BE}}{k T} \right) - 1 \right)$ and by square law expressions for FETs (see EEE118). This expression holds over many orders of magnitude while the relationship between base current and collector current changes considerably (h_{FE} not constant). See Horowitz and Hill, second Ed. pp 79 - 81 section 2.10 for full details.

Small Signal Model

In EEE118 small signal models were developed for a diode and for a transistor acting as an amplifier. The fundamental mechanism underpinning "transistor action" is the transconductance - a small change in input voltage elicits a larger change in output current. For small signals it is the slope of the transconductance characteristic that is significant.



$$I_C = I_{C_O} \left(\exp^{\left(\frac{q V_{BE}}{k T} \right)} - 1 \right) \quad (1)$$

the slope is,

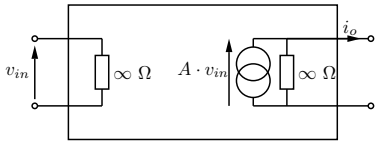
$$\frac{d I_C}{d V_{BE}} = I_{C_O} \frac{q}{k T} \exp^{\left(\frac{q V_{BE}}{k T} \right)} \quad (2)$$

For a conducting diode, $\exp^{\left(\frac{q V_{BE}}{k T} \right)} >> 1$ so,

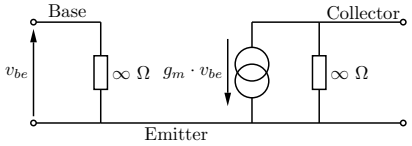
$$I_C = I_{C_O} \left(\exp^{\left(\frac{q V_{BE}}{k T} \right)} - 1 \right) \approx I_C = \left[I_{C_O} \exp^{\left(\frac{q V_{BE}}{k T} \right)} \right] \quad (3)$$

$$\therefore \frac{d I_C}{d V_{BE}} = \frac{q}{k T} \cdot \left[I_{C_O} \exp^{\left(\frac{q V_{BE}}{k T} \right)} \right] = \frac{q I_C}{k T} \quad (4)$$

$g_m = \frac{q I_C}{k T}$ is a fundamental relationship which holds over more than nine orders of magnitude of I_C. Remember it! Looking back at EEE118 lecture 13, the generalised transconductance amplifier is,



But, the transistor only has three terminals. For the circuits in this course the emitter terminal is common to both the input and output networks. The small signal model of a transistor reduces to,



this is a good low frequency model for JFETs, MOSFETs and Valves. The BJT is special however because there is recombination of carriers in the base region, a base current flows. As a result the resistance looking into the base towards the emitter must be finite (by Ohm's law). The characteristics can be used indirectly to yield the small signal base emitter resistance, r_{be}.

$$r_{be} = \frac{d\,V_{BE}}{d\,I_B} = \frac{d\,I_C}{d\,I_B} \cdot \frac{d\,V_{BE}}{d\,I_C} \tag{5}$$

$$\frac{d\,I_C}{d\,I_B} = \beta = \text{ small signal current gain (see datasheet)} \tag{6}$$

$$\frac{d\,V_{BE}}{d\,I_C} = \frac{1}{g_m} \tag{7}$$

$$\therefore r_{be} = \frac{\beta}{g_m} \tag{8}$$

This is another vital BJT relationship. $d\,V_{BE}$, $d\,I_C$ and $d\,IB$ are the small changes in the bias conditions and may be represented as small signal quantities, v_{be}, i_b and i_c.

$$r_{be} = \frac{\beta}{g_m} = \frac{d\,V_{BE}}{d\,I_B} = \frac{v_{be}}{i_b} \tag{9}$$

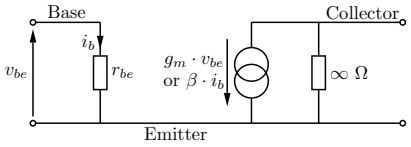
$$r_{be} = \frac{\beta}{g_m} = \frac{v_{be}}{i_b} \tag{10}$$

multiplying through yields,

$$g_m\, v_{be} = \beta\, i_b \tag{11}$$

This means that the BJT can be thought of as a device which accepts an input voltage and outputs a current (transconductance amplifier) or a device that accepts an input current and outputs a current (current amplifier). The choice of how one should think about it depends on the situation. Some circuits are easier to solve if the transistor is thought about in terms of a current amplifier and other circuits are solved more simply by considering the transistor a transconductance device. Only BJTs have the option of two avenues of thought. MOSFETs, JFETS and Valves can only be thought about in terms of transconductance.

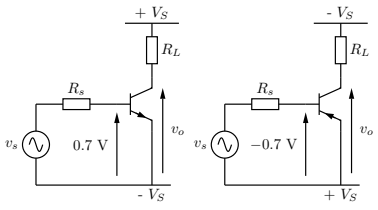
Including the effect of a finite r_{be} in the small signal model yields,



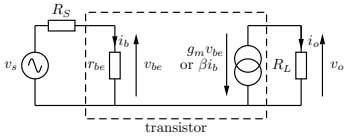
- Usually $\beta \neq h_{FE}$. β is a small signal parameter and h_{FE} is a large signal parameter.
- β is sometimes called h_{fe} (notice the lower case subscripts). h_{FE} and β can be assumed equal at low frequencies
- Other circuit elements can be added to more accurately reflect real device performance e.g. the infinite reistance in parallel with the $g_m \cdot v_{be}$ generator is finite and is responsible for the gentle slope of the output characteristics in the forward active region.

Common Emitter Amplifier

- Large voltage gain.
- Either npn or pnp transistors.
- Both the npn and pnp versions have the same small signal equivalent circuit – next slide.
- The resistors R_S are the Thévenin resistance feeding the base, assume that effects of the biasing circuit are included within R_S.



- R_L represents the total resistance looking from the collector to ground – it is composed of the transistor load resistor, the input resistance of the *next* circuit and the transistor's r_{ce}.



Sum currents at the output,

$$v_o = i_o\, R_L \tag{12}$$

$$= -g_m\, v_{be}\, R_L \tag{13}$$

At the input,

$$v_{be} = v_s \frac{r_{be}}{R_S + r_{be}} \tag{14}$$

Substituting yields,

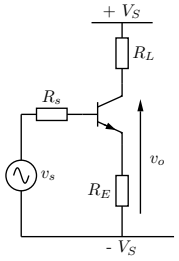
$$\frac{v_o}{v_s} = -g_m\, R_L\, \frac{r_{be}}{R_S + r_{be}} \tag{15}$$

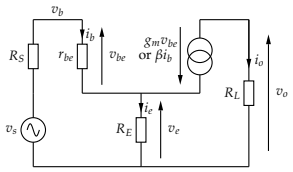
Note:

- The gain is inverting; "–" sign.
- Gain $\propto g_m$ (so large g_ms are attractive).
- Gain $\propto R_L$ (so large R_Ls are attractive).
- Ideally $r_{be} >> R_S$, to avoid attenuation of input.
- resistance looking into input $r_i = r_{be}$.

Common Emitter with Degeneration

- Sometimes CE circuits have a small value of resistance 10s of Ω to low kΩ between the emitter terminal and ground.
- This resistance is called an "emitter degeneration" resistance.
- The small signal equivalent circuit adjusted to add a resistor R_E between the emitter node and ground.
- This complicates the small signal analysis, especially if r_{ce} is included in the analysis, because R_E couples the output circuit to the input circuit.
- We will assume that r_{ce} has a negligible effect.





Summing currents at the emitter,

$$i_e = i_b + g_m\, v_{be} \qquad (16)$$

$$\text{or } \frac{v_e}{R_E} = \frac{v_{be}}{r_{be}} + g_m\, v_{be} \qquad (17)$$

$$v_e = v_{be}\, R_E \left(\frac{1}{r_{be}} + g_m\right) \approx v_{be}\, R_E\, g_m \qquad (18)$$

because $1/r_{be} = g_m/\beta$ and $\beta >> 1$.

For the input loop,

$$v_s = i_b\, R_s + v_{be} + v_e \qquad (19)$$

$i_b = v_{be}/r_{be}$ and using (18),

$$v_s = v_{be}\left(1 + \frac{R_S}{r_{be}} + g_m\, R_E\right) \qquad (20)$$

Looking at the collector circuit, $v_o = i_o\, R_L$ and $i_o = -g_m\, v_{be}$ and using (20),

$$v_o = -g_m\, R_L\, v_{be} = -\frac{g_m\, R_L\, v_s}{\left(1 + \frac{R_S}{r_{be}} + g_m\, R_E\right)} \qquad (21)$$

isolating for v_o/v_s,

$$\frac{v_o}{v_s} = \frac{-g_m\, R_L}{\left(1 + \frac{R_S}{r_{be}} + g_m\, R_E\right)} \qquad (22)$$

$$= -\frac{R_L}{r_e + \frac{R_S}{\beta} + R_E} \qquad (23)$$

where $r_e = 1/g_m$

The important conclusions are:

1. The gain is inverting.
2. The gain is proportional to R_L.
3. R_E reduces the gain.
4. If $R_E >> \frac{1}{g_m}$ and $R_E >> \frac{R_S}{\beta}$ then gain $-\frac{R_L}{R_E}$

The addition of R_E also affects the input resistance of the amplifier. Use node or loop analysis to find v_b/i_b... see handout page 4.

Review

- Stated the Aims and Objectives of the course
  Continue discussion of electronic devices (diodes, transistors *et al.* in circuits)
- Reviewed operating region of transistors. Forward active, saturation, reverse active and off.
- Reviewed output and transfer characteristics as an explanation of transistor operation. Relationship between V_{CE}, I_C and V_{BE}, which describes transistor opperation.
- Re-familliarised ourselves with the idea of small signal models especially in relation to a BJT.
- Reviewed and expanded description of the one transistor common emitter amplifier from EEE118. With and without "degeneration" (negative feedback).



EEE225: Analogue and Digital Electronics

Lecture II

James E. Green

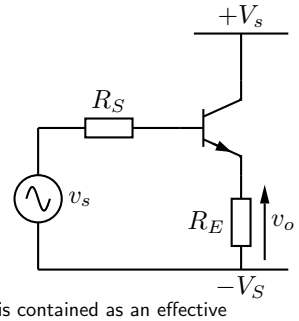
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This Lecture

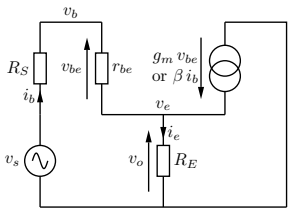
1. One Transistor Circuits Continued...
   - Emitter Follower or Common Collector
   - Emitter Follower Voltage Gain
   - Emitter Follower Input Resistance
   - Emitter Follower Output Resistance
   - Common Base
   - Common Base Voltage Gain
   - Common Base Input Resistance
2. Inside the Opamp
   - Feedback System
   - Simplified Schematic of an Opamp
   - Opamp Circuit DC Conditions
   - Differential Amplifier
3. Review
4. Bear

Emitter Follower / Common Collector

- A kind of "voltage follower" or "buffer"
- Approximately unity voltage gain
- pnp or npn versions possible
- High current gain
- May be thought of as impedance transformer (so can all transistor circuits...)



In this figure the biasing circuitry is contained as an effective resistance within R_S



$$v_o = v_{be}\, R_E \left(\frac{1}{r_{be}} + g_m\right) \quad (1)$$

$$\approx v_{be}\, R_E\, g_m \quad (2)$$

and a relation between v_{be}, v_s and v_o is given by summing voltages around the input loop.

$$v_s = i_b R_S + v_{be} + v_o \quad (3)$$

$$= v_{be}\left(1 + \frac{R_S}{r_b e}\right) + v_o \quad (4)$$

using the result in (2) to eliminate v_{be},

$$\frac{v_o}{v_s} = \frac{r_{be}\, g_m\, R_E}{r_{be}\, g_m\, R_E + R_S + r_{be}} \quad (5)$$

$$= \frac{R_E}{\frac{1}{g_m} + \frac{R_S}{\beta} + R_E} \quad (6)$$

1. The gain is non-inverting
2. Gain ≈ 1 if $R_E >> R_S/\beta$ and $R_E >> 1/g_m$

The input resistance is given by considering v_b/i_b, recall (1)

$$v_e = v_{be}\, R_E \left(\frac{1}{r_{be}} + g_m\right) \quad (7)$$

and summing up the voltages...

$$v_b = v_{be} + v_e \quad (8)$$

$$= v_{be} + v_{be}\, R_E \left(\frac{1}{r_{be}} + g_m\right) \quad (9)$$

$$= v_{be}\left(1 + R_E\left(\frac{1}{r_{be}} + g_m\right)\right) \quad (10)$$

since $v_{be} = i_b\, r_{be}$ and $g_m\, r_{be} = \beta$ we can write,

$$r_i = \frac{v_b}{i_b} = r_{be} + (\beta + 1)\, R_E \quad (11)$$

Generally $(\beta + 1)\, R_E >> r_{be}$ so the input resistance is dominated by the $(\beta + 1)\, R_E$ term. By comparing this result with the input resistance of the non-degenerated common emitter amplifier we could show negative feedback can be used to increase the input resistance of a transistor stage.

To obtain the output resistance inject a test current i_t with the input grounded and find v_o/i_t. Summing currents at v_e

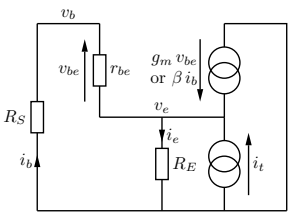
$$(1 + \beta)\, i_b + i_t = \frac{v_e}{R_E} \quad (12)$$

and summing up the voltages in the base loop

$$v_e = -i_b\,(R_S + r_{be}) \quad (13)$$

substituting (13) into (12) and solving for v_e/i_t,

$$r_o = \frac{1}{\frac{1+\beta}{R_S + r_{be}}} + \frac{1}{R_E} \quad (14)$$

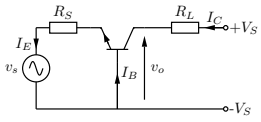


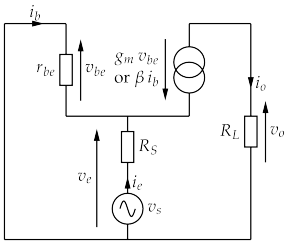
$$r_o \approx \frac{1}{g_m} + \frac{R_S}{\beta} \quad (15)$$

If $\beta >> 1$, the first term becomes $\frac{R_S + r_{be}}{\beta}$ and if R_E is large, we can ignore the $\frac{1}{R_E}$ term.

Common Base Connection

Generally used in conjunction with other transistors in "circuit blocks", but sometimes alone[1]. i_e is the input current (flowing from v_s), since $i_e = i_o + i_b$ the current gain (i_o/i_e) is slightly less than 1 (actually it's $= \alpha$).





summing currents,

$$i_e + i_b + g_m v_{be} = 0 \qquad (16)$$

[1] http://dx.doi.org/10.1088/0957-0233/23/12/125901

$$\frac{v_s - v_e}{R_S} + \frac{v_{be}}{rbe} + g_m v_{be} = 0 \quad (17)$$

$v_e + v_{be} = 0$ so $v_e = -v_{be}$ therefore (17) can be solved for v_{be}

$$v_{be} = -\frac{v_s}{R_S\left(\frac{1}{R_S} + \frac{1}{r_{be}} + g_m\right)} \qquad (18)$$

$$\approx -\frac{v_s}{1 + g_m R_S} \qquad (19)$$

approximation is because $1/r_{be} = g_m/\beta$ and $\beta >> 1$

At the output,

$$v_o = i_o R_L = -g_m v_{be} R_L \qquad (20)$$

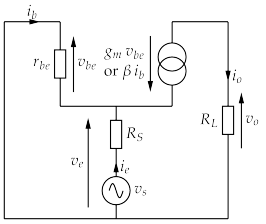
combining this with (19) to eliminate v_{be}

$$\frac{v_o}{v_s} = \frac{g_m R_L}{1 + g_m R_S} = \frac{R_L}{r_e + R_S} \qquad (21)$$

where $r_e = 1/g_m$.

- The gain is non-inverting
- Gain $\propto R_L$
- If $R_S >> r_e$ gain controlled by ratio R_L/R_S

Common Base Input Resistance



The resistance looking into the emitter,

$$r_i = \frac{v_e}{i_e} = \frac{v_e}{\frac{-v_{be}}{r_{be}} - g_m v_{be}} \qquad (22)$$

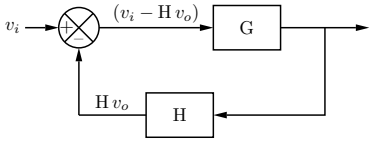
Since $v_e = -v_{be}$ and $g_m >> 1/r_{be}$ this reduces to $r_i \approx \frac{1}{g_m} = r_e$ The value is small 10s - 100s Ω

There is another model of the transistor called "T Model" in which r_e plays a much bigger role. However hybid-π is the only model we will use. The original π paper is by Giacolletto[2].

[2] http://dx.doi.org/10.1109/JSSC.1969.1049963

Feedback Systems (Quick reminder)

In EEE118 we discussed the opamp in terms of a general feedback system.



So $v_o = G(v_i - H v_o)$ (23)

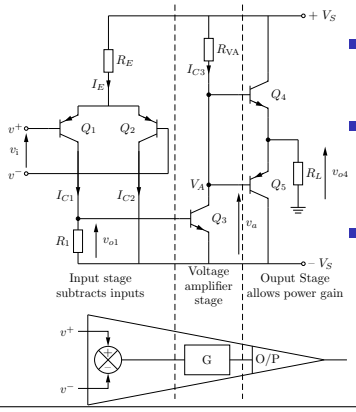
or $v_o(1 + G H) = G v_i$ (24)

$$\frac{v_o}{v_i} = \frac{G}{1 + G H} \qquad (25)$$

If $|G H| >> 1$,

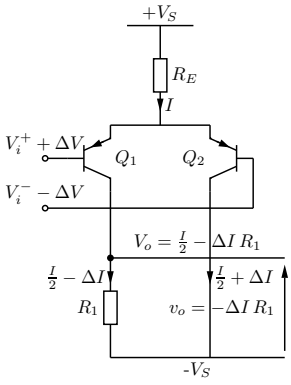
$$\frac{v_o}{v_i} = \frac{G}{G H} = \frac{1}{H} \qquad (26)$$

System dependent on H, designer controls H with ratio of resistors.

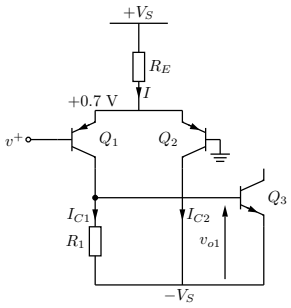


- Input stage: differential amplifier or "long tailed pair". Subtracts the inputs.
- Voltage amplifier stage (VAS): common emitter amplifier. Provides majority of voltage gain.
- Output stage: emitter follower. Increases current capability of VAS (voltage × current = power... hence "power gain".

- Opamp will not work properly without feedback. Feedback controls the gain of the circuit but also helps define the DC conditions. Feedback adjusts v_i in order to achieve the internal voltage drops required for proper operation. If $v_o = 0$, v_i will be at the value it needs to be in order to make $v_o = 0$. Feedback is *not* shown on prior slide.
- If $v^+ \approx v^- \approx 0$, V_{E1} and $V_{E2} \approx 0.7$ so $I_E \approx (+V_S - 0.7)/R_E$.
- I_E splits between Q_1 and Q_2 to form I_{C1} and I_{C2}.
- I_{C1} has two functions 1) create a voltage drop of 0.7 V across R_1 in order to bias Q_3 into conduction. 2) Provide the base current for Q_3. I_{C1} will be $0.7/R_1 + I_{C3}/h_{FE3}$.
- The value of I_{C3} varies with V_A and hence with V_{o4} but assuming $V_A = 0$, $I_{C3} = +V_S/R_{VA}$.
- I_{C2} is returned directly to the negative supply.
- In the case where $v^+ \approx v^- \neq 0$, there is a common mode input voltage, v_{cm}, and $I_E \approx (+V_S - v_{cm})/R_E$.

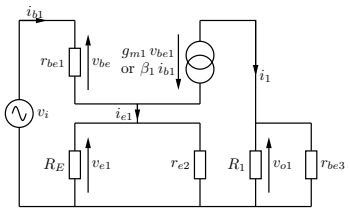


- If v^+ increases by Δv_i and v^- decreases by Δv_i, the average of v^+ and v^- is unchanged so I_E is unchanged because V_{be} is unchanged.
- If v^+ and v^- increase or decrease by Δv_i, v_i is called a "common mode signal" ideally the differential amplifier will not amplify any common mode component of the input.



We must consider the effects of three transistors. Q_1 and Q_2 are the input differential pair.

Q_3 must also be considered now because its input resistance forms part of Q_1's collector load resistance. If the input signal is regarded as v^+ with respect to ground, Q_2 looks like a common base connection and can be represented by its common base input resistance $1/g_{m2}$. The collector current of Q_1 sees two resistors in parallel, R_1 and the input resistance of Q_3. Q_3 is a common emitter amplifier *without* degeneration. Its input resistance is r_{be3}.



A small signal equivalent circuit describes the three transistor circuit block according to our simplifications.

This small signal model is very similar to the common emitter *with* degeneration from Lecture 1. In this case $R_S = 0$ and R_E and R_L are parallel combinations $R_E//r_{e2}$ and $R_1//r_{be3}$. Since $R_E >> r_{e2}$, r_{e2} dominates. The gain expression for the circuit is (based on the degenerated CE analysis)

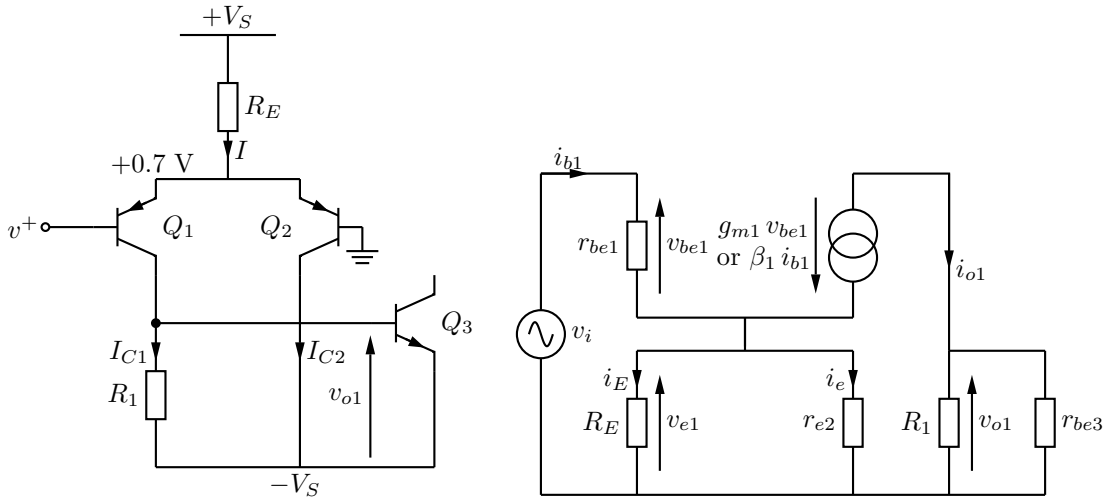
$$\frac{v_{o1}}{v_i} = -\frac{R_1//r_{be3}}{r_{e1} + r_{e2}} \quad (27)$$

Review

- Considered the emitter follower circuit (voltage gain, current gain, input and output resistances).
- Considered the common base circuit (voltage gain, current gain, input resistance).
- Recapped the idea of the opamp as a feedback system.
- Introduced a simplified schematic of an opamp.
- Developed some ideas around the DC conditions of the simplified opamp
- Looked at the combination of three transistors into a differential amplifier + common emitter stage and considered their combined effect.



A Small Signal Analysis of the Differential Amplifier in an Opamp



(a) Circuit 1 (b) Circuit 2

Figure 1: Differential Amplifier Circuit used in the input stage of a simple operational amplifier.

Starting at the output

$$v_{o1} = i_{o1} \cdot R_1 // r_{be3} \tag{1}$$

$$i_{o1} = -g_{m1}\, v_{be1} \tag{2}$$

$$\therefore v_{o1} = -g_{m1}\, v_{be1} \cdot R_1 // r_{be3} \tag{3}$$

$$\text{or } \frac{v_{o1}}{v_{be1}} = -g_{m1}\, R_1 // r_{be3} \tag{4}$$

We now need a relationship between v_{be1} and v_i.

Sum the currents at the emitter node

$$\frac{v_{be1}}{r_{be1}} + g_{m1}\, v_{be1} = i_E + i_e \tag{5}$$

$$\frac{v_i - v_{e1}}{r_{be1}} + g_{m1}\, v_{be1} = v_{e1}\left[\frac{1}{R_E} + \frac{1}{r_{e2}}\right] \tag{6}$$

$$\tag{7}$$

remember that

$$v_{e1} = v_i - v_{be1} \tag{8}$$

$$\frac{v_i - (v_i - v_{be1})}{r_{be}} + g_{m1}\, v_{be1} = (v_i - v_{be1}) \left[\frac{1}{R_E} + \frac{1}{r_{e2}}\right] \tag{9}$$

$$\frac{v_{be1}}{r_{be1}} + g_{m1}\, v_{be1} + v_{be1} \left[\frac{1}{R_E} + \frac{1}{r_{e2}}\right] = v_i \left[\frac{1}{R_E} + \frac{1}{r_{e2}}\right] \tag{10}$$

$$v_{be1} \left[\frac{1}{r_{be1}} + g_{m1} + \frac{1}{R_E} + \frac{1}{r_{e2}}\right] = v_i \left[\frac{1}{R_E} + \frac{1}{r_{e2}}\right] \tag{11}$$

r_{be1} and R_E are $>>$ $\dfrac{1}{g_{m1}}$ and r_{e2}

$$v_{be1} \left[g_{m1} + \frac{1}{r_{e2}}\right] \approx v_i \left[\frac{1}{r_{e2}}\right] \tag{12}$$

If Q_1 and Q_2 have the same collector current then $g_{m1} = g_{m2} = \dfrac{1}{r_{e2}}$

$$v_{be1} \left[2\, g_{m1}\right] = v_i \left[g_{m1}\right] \tag{13}$$

$$\frac{v_{be}}{v_i} \approx \frac{1}{2} \tag{14}$$

The overall gain is given by

$$\frac{v_{o1}}{v_i} = \frac{v_{o1}}{v_{be1}} \cdot \frac{v_{be1}}{v_i} \tag{15}$$

$$= -g_{m1} \cdot R_1 // r_{be3} \cdot \frac{1}{2} \tag{16}$$

The final form depends on the assumptions made and the particulars of the circuit. It is *pointless* to memorise this analysis - it's just an example... the methods used are the important tools, these should be practised.

EEE225: Analogue and Digital Electronics

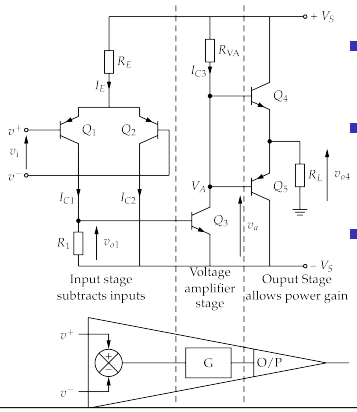
Lecture III

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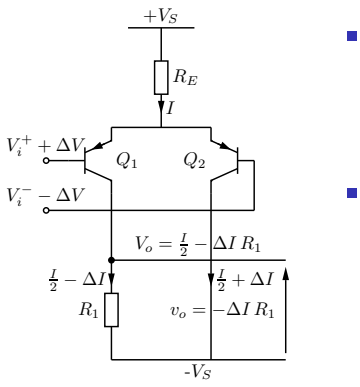
This Lecture

1. Into The Opamp
   - Simplified Schematic of an Opamp
   - Opamp Circuit DC Conditions
   - Differential Amplifier
2. The "Voltage Amplifier" stage
   - Voltage Amplifier Stage Gain
3. The Output Stage
4. Class A and B Push Pull Amplifiers - Angle of Conduction
5. Review
6. Bear

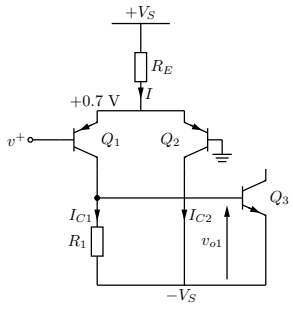


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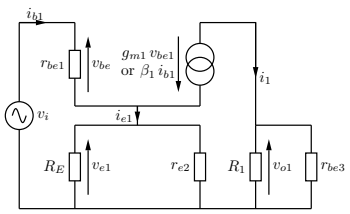


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We must consider the effects of three transistors. Q_1 and Q_2 are the input differential pair.

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This small signal model is very similar to the common emitter *with* degeneration from Lecture 1. In this case $R_S = 0$ and R_E and R_L are parallel combinations $R_E//r_{e2}$ and $R_1//r_{be3}$. Since $R_E >> r_{e2}$, r_{e2} dominates. The gain expression for the circuit is (based on the degenerated CE analysis)

$$\frac{v_{o1}}{v_i} \approx -\frac{g_{m1} \cdot R_1//r_{be3}}{2} \tag{1}$$

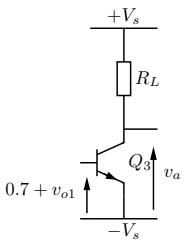
- To maximise gain make both R_1 and r_{be3} as big as possible.
- Could try to increase g_{m1} however, since $g_{m1} = \frac{e\,I_{C1}}{k\,T}$ increasing g_{m1} would require an increase of I_{C1}. I_{C1} can't change without decreasing R_1 in order to maintain the DC conditions of $I_{C1}\,R_1 = 0.7\ V$. There is no advantage in trying to increase g_{m1} to yield a larger gain. Other factors such as base currents and frequency dependent behaviour would also be affected.

The input resistance of the circuit is given by

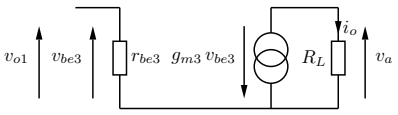
$$r_i = r_{be1} + (\beta_1 + 1)\ r_{e2} \tag{2}$$

which is similar to the common emitter amplifier *with* degeneration. If $I_{C1} \approx I_{C2}$ and $\beta_1 \approx \beta_2$ i.e. Q_1 and Q_2 are balanced and identical, $r_i = 2\,r_{be1}$.

Voltage Amplifier Stage



The VAS is a non-degenerated common emitter circuit.



1. A small signal equivalent circuit describes the voltage amplification stage.
2. We can neglect any R_S because the effects of the finite output resistance of the differential stage have already been taken into account - we included r_{be3} in our earlier calculations.
3. v_{o1} and v_{be3} are equal.

Voltage Amplifier Stage Gain

The resistance a small signal sees looking out from Q_3's collector is the parallel combination of:

1. The input resistance of Q_4, r_{i4}.
2. The input resistance of Q_5, r_{i5}.
3. The Early resistance of Q_3, r_{ce3}.
4. The resistor R_{VA}.

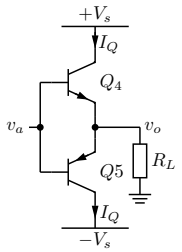
R_{VA} is much smaller than any of the others and so dominates the value of R_L. $R_L \approx R_{VA}$.

Some standard analysis...

$$v_a = i_o\,R_L \tag{3}$$
$$i_o = -g_{m3}\,v_{be3} \tag{4}$$
$$\text{so } v_a = -g_{m3}\,v_{be3}\,R_L \tag{5}$$
$$\text{but } v_{be3} = v_{o1} \tag{6}$$
$$\text{so } v_a = -g_{m3}\,v_{o1}\,R_L \tag{7}$$
$$\frac{v_a}{v_{o1}} = -g_{m3}\,R_L \tag{8}$$

For typical values the gain of the voltage amplifier stage when R_{VA} is a resistor is a few hundred.

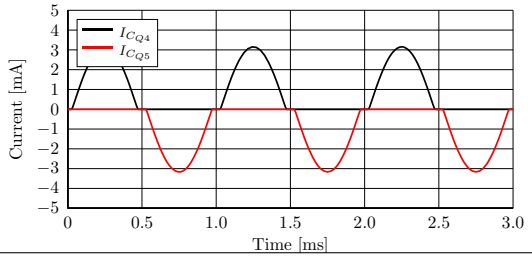
The Output Stage



An NPN and PNP emitter follower.

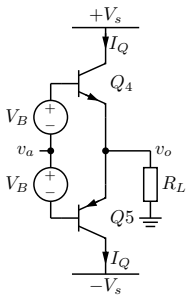
- The output stage operates on "large" signals.
- Q_4 deals with positive currents - from $+V_s$ into the ground via R_L
- Q_5 deals with negative currents - from the ground via R_L into $-V_s$
- The signals are "large" because the quiescent current I_Q is *not* many times bigger than the signal currents.
- The signal currents upset the quiescent conditions. It is not fruitful to draw a small signal diagram.

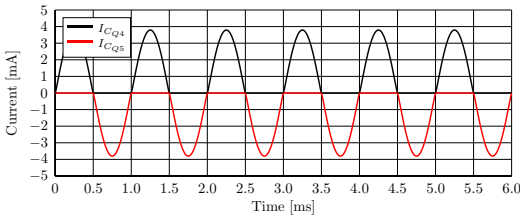
- The voltage gain of the output stage is approximately unity.
- The objective of the output stage is to increase the VAS's ability to drive current into the load resistance.
- The combination of the VAS and OPS provide power gain.
- The transistors must be turned on by the signal, consequently a kind of distortion - "Crossover Distortion" exists around the transistion between Q_4 conduction and Q_5 conduction.

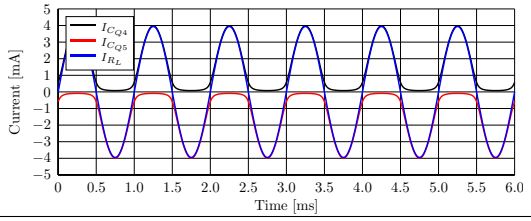


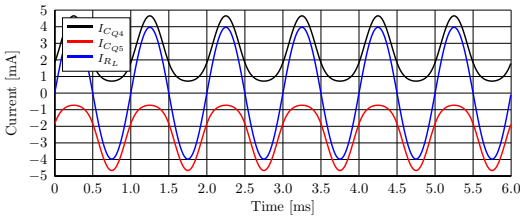
Biasing the Output Stage

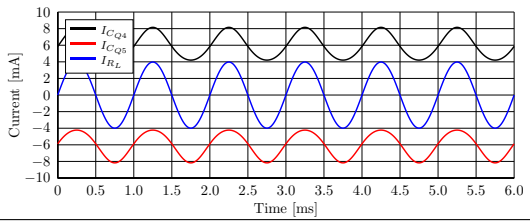
- Biasing the transistors into conduction can lessen the effect of crossover distortion a great deal.
- It also allows us to think about the relationship between the quiescent current and the signal current in the push pull stage.
- These thoughts can be widely generalised.
- Consider five sets of V_B which yield differing "angles of conduction".
- Without any bias each transistor conducts for slightly less than 1/2 a cycle $< 180^\circ$









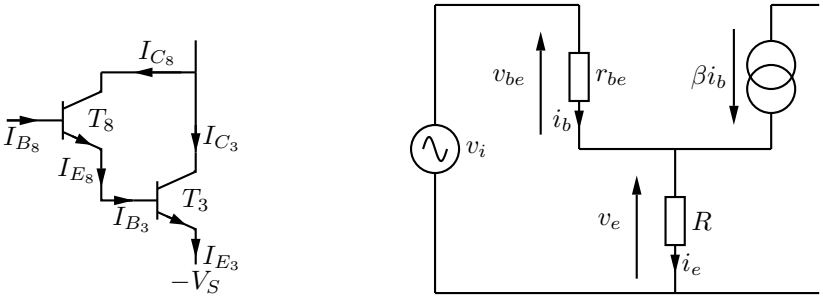


Review

- Reviewed structure of the Opamp.
- Considered DC conditions of the input and voltage amplifier stages.
- Described the gain and input resistance of the input stage to a differential signal.
- Analysed the voltage amplification stage from a small signal perspective.
- Qualitatively described the push-pull emitter follower output stage.
- Introduced the idea of "classes" of amplifier and "conduction angle".
- Noted that the relative size of the quiescent current and the signal current will determine the conduction angle and so the class of amplifier.



Small Signal Input Resistance of a Darlington Pair



(a) Darlington Pair circuit connection(b) Darlington pair small signal model showing the DC or quiescent currents. where the input resistance of the lower transistor is "R".

Summing currents at the Emitter

$$i_e = i_b + \beta i_b \tag{1}$$

$$\frac{v_e}{R} = \frac{v_{be}}{r_{be}} + g_m\, v_{be} \tag{2}$$

Summing voltages around the input loop

$$v_b = v_{be} + v_e \tag{3}$$

$$\frac{v_{be}}{r_{be}} + g_m\, v_{be} = \frac{v_b - v_{be}}{R} \tag{4}$$

$$v_{be} + \left(\frac{1}{r_{be}} + g_m + \frac{1}{R}\right) = \frac{v_b}{R} \tag{5}$$

$$i_b\, r_{be} \left(\frac{1}{r_{be}} + g_m + \frac{1}{R}\right) = \frac{v_b}{R} \tag{6}$$

$$r_i = \frac{v_b}{i_b} = \left(1 + g_m\, r_{be} + \frac{r_{be}}{R}\right)\, R \tag{7}$$

$$= (R + g_m\, r_{be}\, R + r_{be}) \tag{8}$$

$$\tag{9}$$

A standard expression for g_m,

$$g_m = \frac{\beta}{r_{be}} \tag{10}$$

so

$$r_i = (R + \beta\, R + r_{be}) \tag{11}$$

if

$$\beta >> 1 \tag{12}$$

then

$$r_i = r_{be} + \beta R \tag{13}$$

For a Darlington connection $R = r_{be_3}$, the input resistance of T_3. So we have,

$$r_i = r_{be_8} + \beta_8 r_{be_3} \tag{14}$$

EEE225: Analogue and Digital Electronics

Lecture IIII

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This Lecture

1. Problems with the Basic Opamp
   - Differential Stage
   - VAS and OPS
   - Problems with the Output Stage
2. Solutions...
   - Input Stage Balance and Gain
   - Voltage amplification stage biasing current and input resistance
   - Voltage amplification stage load resistance
3. Review
4. Bear

Differential Stage Problems

Problems with the input (differential) stage

1. Half of the differential signal is wasted. The collector of T_2 is connected to the negative supply. The output from the differential stage is ΔI for a given ΔV input (see lecture 3 slide 5) but we can do better...
2. The balance of collector current in T_1 and T_2 is difficult to maintain due to loading effect of T_3 - this leads to DC offset at the output.
3. The current flowing into the base of T_1 and T_2 is quite high. This input current has to be supplied by the signal source. The basic opamp has a low input resistance compared to a commercial opamp.
4. The effective load resistance of the differential stage (approximately // combination of R_1 and r_{be3}) is very low so the differential stage has low gain.

VAS and OPS Problems

Problems with the voltage amplification stage

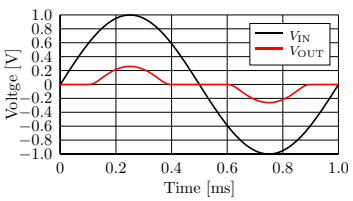
1. R_{VA} needs to be quite small to maintain correct DC (quiescent) conditions – the quiescent current of T_3 flows through R_{VA} – but the gain of the VAS is proportional to R_{VA} so a very large value is desirable which the DC current does not permit.

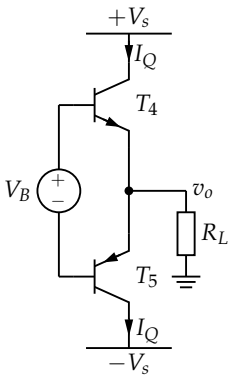
Problems with the output stage

1. The input resistance of T_4 and T_5 depends on the external opamp load resistance, this affects the effective load resistance of the VAS altering its gain.
2. The output resistance of the emitter follower is dependent on the source resistance driving it.
3. Without OPS biasing T_4 and T_5 will give rise to severe crossover distortion (as per Amplifier Lab).

Briefly discussed in Lecture 3, where OPS biasing was considered,

1. In terms of the magnitude of the signal current compared to the quiescent current.
2. In terms of the angle of conduction of T_4 and T_5 as a fraction of one cycle (360°)





$V_B = 0$

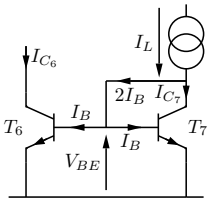
Input Stage Balance and Gain - Current Mirrors

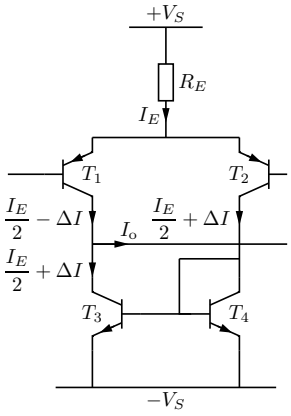
- Assume T_6 and T_7 are identical
- Circuit tries to make $I_{C_6} = I_L$
- Collector and base of T_7 connected together
- Base of T_6 and T_7 connected together
- Emitters of T_6 and T_7 connected together
- V_{BE} identical for both transistors

I_L develops a V_{BE} sufficient to make T_7 conduct a current $I_{C_7} = I_L - 2I_B$

$$I_L = I_{C_7}\left(1 + \frac{2}{h_{FE}}\right) \quad (1)$$

$$I_{C_7} = I_L \frac{h_{FE}}{2 + h_{FE}} \quad (2)$$





Suppose T_1's base is slightly positive with respect to T_2's. Considering the action of the current mirror we can sum currents at the collector of T_3.

$$I_o = \frac{I_E}{2} - \Delta I - \left(\frac{I_E}{2} + \Delta I\right) \quad (3)$$

$$I_o = -2\Delta I \quad (4)$$

The output signal current from the differential stage has been doubled. And the quiescent currents in T_1 and T_2 are now nearly identical.

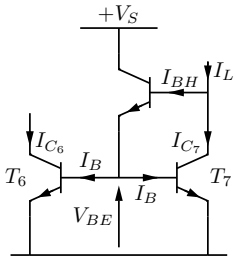
- The mirror is not perfect however as the mirroring depends on h_{FE}.
- In reality the transistors will not be identical.
- The error due to finite h_{FE} can be reduced by using a "β helper" transistor.

Assuming all transistors have the same h_{FE}

$$I_{BH} = \frac{2\,I_B}{h_{FE}} \quad (5)$$

$$I_L = I_{C_7} + I_{BH} \quad (6)$$

$$= I_{C_7}\left(\frac{h_{FE}^2 + 2}{h_{FE}^2}\right) \quad (7)$$



For small signals, h_{FE} becomes β and the small signal Early resistance of T_7, r_{ce} conducts a small part of i_L into the negative rail.

The main cause of imbalance of current in the differential pair collectors is the base current flowing into the VAS. A second transistor can be added to the VAS to form a Darlington pair.

$$I_{E_3} = I_{C_3} + I_{B_3} \quad (8)$$

$$I_{E_3} = h_{FE_3}\, I_{B_3} + I_{B_3} \quad (9)$$

$$I_{E_3} = I_{E8}\,(h_{FE_3} + 1) \quad (10)$$

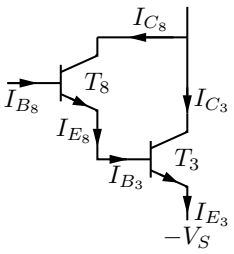
similarly

$$I_{E_8} = I_{B_8}\,(h_{FE_8} + 1) \quad (11)$$

Eliminating I_{E_8}...

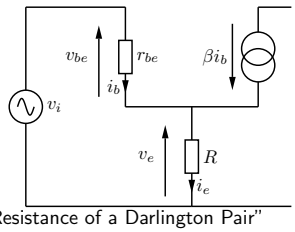
$$I_{E_3} = I_{B_8}\,(h_{FE_8} + 1)\,(h_{FE_3} + 1) \quad (12)$$

If h_{FE_3} & $h_{FE_8} >> 1$, $I_{E_3} = I_{C_3}$ and $\frac{I_{C_3}}{I_{B_8}}$ is very large.



For small signals,

- Assume that the input resistance of T_3 is "R".
- Draw a small signal diagram.
- Sum currents at the emitter.
- Sum voltages round the input loop.

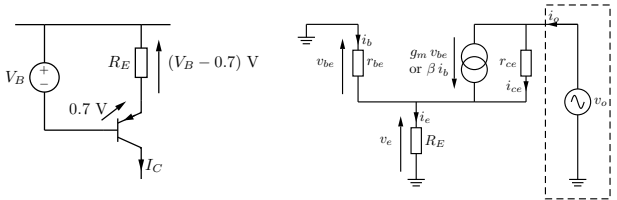


See handout "Small Signal Input Resistance of a Darlington Pair" for a possible solution. But in brief,

$$r_i = r_{be_8} + \beta_8\, r_{be_3} \quad (13)$$

r_i is increased by the β of the (new) upper transistor multiplied by the input resistance of the lower transistor. Remember quiescent currents in T_3 and T_8 will be different and so their g_m's will be different as a consequence $r_{be_8} \neq r_{be_3}$. more precisely $r_{be_8} >> r_{be_3}$.

From lecture 3, the resistance looking out of T_3's collector is $\approx R_{VA}$. Increasing the value of R_{VA} is desirable as it increases gain. However T_3's quiescent collector current has to flow through R_{VA} limiting its value. R_{VA} can be replaced by a current source (left) and its small signal model (right).



The effective resistance looking into the current source output – it's output resistance – will become the new R_{VA}. For analysis see handout "Small Signal Output Resistance of a Simple Current Source". In brief $r_o \approx r_{ce}\,(1 + \beta)$.

Review

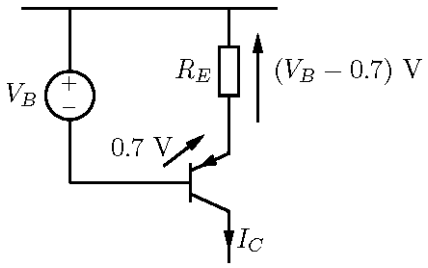
- Considered problems related to input stage, voltage amplification stage and output stage of the simple opamp.
- Introduced current mirrors (two kinds)
- Introduced the Darlington pair
- Introduced a one transistor current source

The key points about these integrated circuit building blocks are,

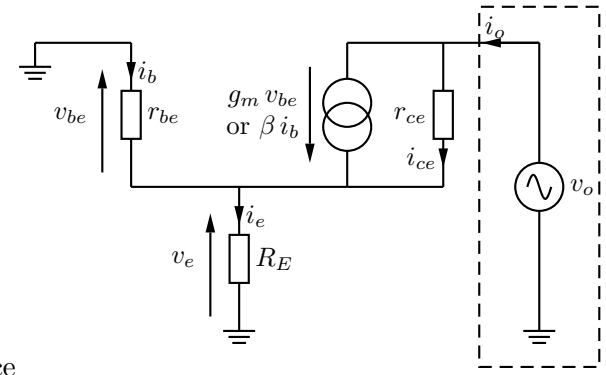
1. To understand the bigger circuits one must first be confident with all their various circuit blocks.
2. To put the circuit blocks together one must appreciate how they are likely to interact.
3. Reducing the problem to the components which are dominant is one key to an easy analogue life...
4. ...the other is practice.



Small Signal Output Resistance of a Simple Current Source



(a) Single transistor current source (PNP version shown).



(b) Single transistor current source small signal model (valid for both NPN and PNP).

Summing currents at the Emitter

$$i_b + g_m\, v_{be} + i_{ce} = i_e \tag{1}$$

$$\frac{v_{be}}{r_{be}} + g_m\, v_{be} + \frac{v_o - v_e}{r_{ce}} = \frac{v_e}{R_E} \tag{2}$$

but,

$$v_e = -v_{be} \tag{3}$$

so using this to eliminate v_e and collecting terms...

$$-\frac{v_o}{r_{ce}} = v_{be}\left[\frac{1}{r_{ce}} + g_m + \frac{1}{r_{be}} + \frac{1}{R_E}\right] \tag{4}$$

now sum the currents at the output node,

$$i_o = g_m\, v_{be} + i_{ce} \tag{5}$$

$$i_o = g_m\, v_{be} + \frac{v_o - v_e}{r_{ce}} \tag{6}$$

again we can use $v_e = -v_{be}$, and collecting terms,

$$v_{be} = \frac{i_o - \frac{v_o}{r_{ce}}}{\frac{1}{r_{ce}} + g_m} \tag{7}$$

eliminating v_{be} by substituting (7) into (4) and collecting terms,

$$\frac{v_o}{i_o} = r_{ce}\left[\frac{\frac{1}{r_{be}} + g_m + \frac{1}{r_{ce}} + \frac{1}{R_E}}{\frac{1}{r_{be}} + \frac{1}{R_E}}\right] \tag{8}$$

$$= r_{ce}\left[1 + \frac{g_m + \frac{1}{r_{ce}}}{\frac{1}{r_{be}} + \frac{1}{R_E}}\right] \tag{9}$$

Now,

$$g_m \approx \frac{1}{\text{10s to 100s } \Omega} \text{ and } r_{ce} \approx \frac{1}{\text{10s to 100s k}\Omega} \tag{10}$$

so,

$$g_m >> \frac{1}{r_{ce}} \tag{11}$$

$$\frac{v_o}{i_o} \approx r_{ce}\left[1 + \frac{g_m}{\frac{1}{r_{be}} + \frac{1}{R_E}}\right] \tag{12}$$

$$= r_{ce}\left[1 + g_m\left(r_{be}//R_E\right)\right] \tag{13}$$

If r_{be} dominates the $r_{be}//R_E$ combination,

$$\frac{v_o}{i_o} \approx r_{ce}\left[1 + g_m\, r_{be}\right] = r_{ce}\left(1 + \beta\right) \tag{14}$$

since

$$r_{be} = \frac{\beta}{g_m}$$

EEE225: Analogue and Digital Electronics

Lecture V

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This Lecture

1. Problems with the Basic Opamp
   - Differential Stage
   - VAS and OPS
   - Voltage amplification stage load resistance
   - The Output Stage's Input Resistance
   - The Output Stage's Output resistance
   - Crossover Distortion and the "amplified diode"
   - An Improved Opamp Design
   - Cascode
2. A Real Opamp
   - Texas Instruments LM741
3. Review
4. Bear

Differential Stage Problems

Problems with the input (differential) stage

1. Half of the differential signal is wasted. The collector of T_2 is connected to the negative supply. The output from the differential stage is ΔI for a given ΔV input (see lecture 3 slide 5) but we can do better...
2. The balance of collector current in T_1 and T_2 is difficult to maintain due to loading effect of T_3 - this leads to DC offset at the output.
3. The current flowing into the base of T_1 and T_2 is quite high. This input current has to be supplied by the signal source. The basic opamp has a low input resistance compared to a commercial opamp.
4. The effective load resistance of the differential stage (approximately // combination of R_1 and r_{be3}) is very low so the differential stage has low gain.

VAS and OPS Problems

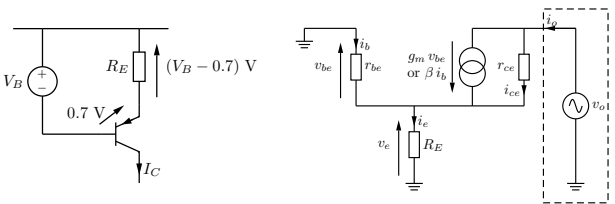
Problems with the voltage amplification stage

1. R_{VA} needs to be quite small to maintain correct DC (quiescent) conditions – the quiescent current of T_3 flows through R_{VA} – but the gain of the VAS is proportional to R_{VA} so a very large value is desirable which the DC current does not permit.

Problems with the output stage

1. The input resistance of T_4 and T_5 depends on the external opamp load resistance, this affects the effective load resistance of the VAS altering its gain.
2. The output resistance of the emitter follower is dependent on the source resistance driving it.
3. Without OPS biasing T_4 and T_5 will give rise to severe crossover distortion (as per Amplifier Lab).

From lecture 3, the resistance looking out of T_3's collector is $\approx R_{VA}$. Increasing the value of R_{VA} is desirable as it increases gain. However T_3's quiescent collector current has to flow through R_{VA} limiting its value. R_{VA} can be replaced by a current source (left) and its small signal model (right).



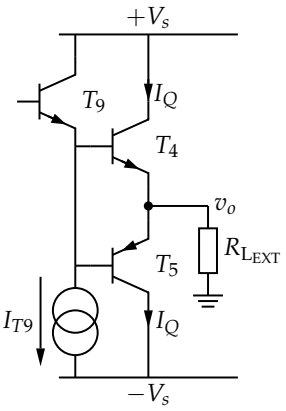
The effective resistance looking into the current source output – it's output resistance – will become the new R_{VA}. For analysis see handout "Small Signal Output Resistance of a Simple Current Source". In brief $r_o \approx r_{ce}(1+\beta)$.

The output stage's input resistance (looking into T_4 and T_5) is affected by the external load resistance $R_{L_{\rm EXT}}$. The VAS gain is affected as R_{VA} is now not so low as to be dominant. T_9 can be added to partially overcome this loading effect. T_9 forms a Darlington pair with whichever of T_4 or T_5 is conducting. The input resistance of T_4 is

$$r_{i4} = r_{be4} + (\beta_4 + 1)\, R_{L_{\rm EXT}} \quad (1)$$

The input resistance of T_9 is,

$$r_{i9} = r_{be9} + (\beta_9 + 1)\, r_{i4} \quad (2)$$

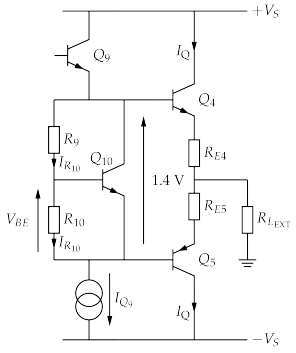


The now higher resistance looking towards T_3's collector acts to increase the output resistance of the amplifier as well. The output resistance of an emitter follower is

$$r_o = \frac{r_{be}}{\beta} + \frac{R_S}{\beta} \qquad (3)$$

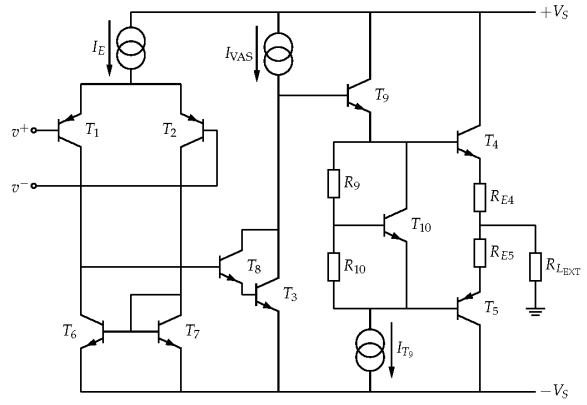
Without T_9 the R_S for T_4 is the collector load resistance of T_3 which has been made very large to maximise the VAS gain. This increases the OPS output resistance. Including T_9 allows the input resistance of the OPS (T_9, T_4 and T_5) to be large and the output resistance of the OPS to be small.

These two problems (firstly the low input resistance of the OPS, and secondly, having increased the source resistance driving the OPS, the OPS output resistance increases) unveil the true nature of the transistor – an imperfect impedance transformer. The ideal OPS would present infinite input resistance to its source and present zero output resistance to its load. Adding T_9 improves the resistance transforming property.



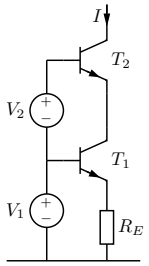
T_4 and T_5 don't conduct until $|V_{BE}| > 0.7\ V$.

When the bases of T_4 and T_5 are connected together there is a region in which the signal is permanently lost. A circuit to spread the bases by approximately $2\,V_{BE}$ is inserted between them. This is sometimes called an amplified diode. The V_{BE} of T_{10} appears across R_{10} causing a current $I_{R_{10}}$. Assume $I_{B_{(T_{10})}} = 0$ so $I_{R_{10}}$ must flow in R_9 also. Reducing R_{10} increases the current through it (voltage is very nearly fixed). The voltage across R_9 must increase... $I_{R_{10}}$ should be a fraction of I_{T_9}.

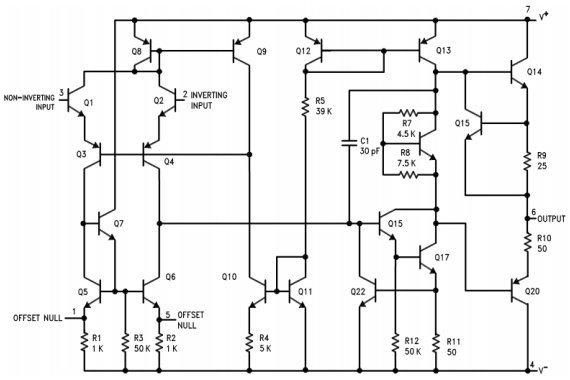


- I_E, I_{VAS} and I_{T_9} set up the DC or quiescent conditions by defining currents.
- Current sources are normally current mirror circuits with one or two additional components to set the DC conditions. The simple current source tends not to see much use.
- The current mirrors can be connected together to allow the ratio of supplied currents to be set. The simple current source has no similar advantage.
- I_E is typically $10 - 50\ \mu\text{A}$. I_{VAS} is typically $100 - 200\ \mu\text{A}$ and I_{T_9} is typically $1 - 5\ \text{mA}$
- This improved circuit reduces all of the problems. However it is one possible implementation of a simple opamp. Real opamps tend to be somewhat more complicated.
- Notice the general lack of resistors - transistors are easy to produce in ICs, resistors (especially precise values) are difficult and expensive. Designers will always use one or more transistors if possible.

- A common emitter amplifier (T_1) connected to the input of a common base amplifier (T_2).
- Prevents voltage swing on the collector of (T_1) by making the resistance looking into T_2's emitter small.



- Enhances the bandwidth of the CE stage by reducing the "Miller effect".
- Depletion capacitance of T_1's reverse biased CB junction couples signal voltages from the collector to the base developing undesirable negative feedback effect – overcome by preventing significant voltage swing on this node.
- The voltage swing on T_2's collector is OK because T_2's base is a fixed voltage - it does not have the input signal on it and is a low resistance path to ground for signals.



Review

- Introduced a one transistor current source
- Re-iterated concept of transistor as an active component for transforming resistances (a transfer-resistor) by looking at the OPS input and output impedances
- Introduced the amplified diode, and cascode circuit
- Briefly discussed a simplified schematic of a real opamp (circa 1968).

The key points about these integrated circuit building blocks are,

1. To understand the bigger circuits one must first be confident with all their various circuit blocks.
2. To put the circuit blocks together one must appreciate how they are likely to interact.
3. Reducing the problem to the components which are dominant is one key to an easy analogue life...
4. ...the other is practice, and reading!



EEE225: Analogue and Digital Electronics

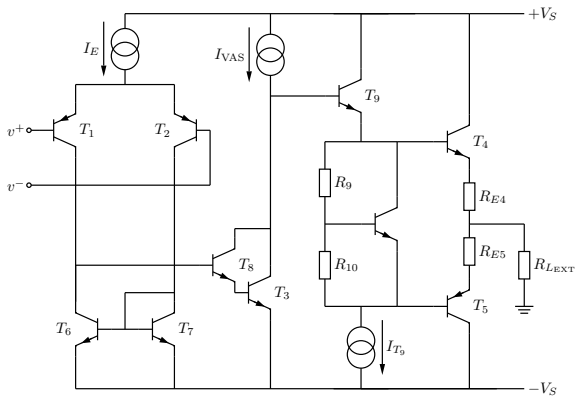
Lecture VI

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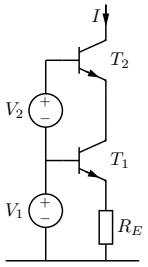
This Lecture

1. An Improved Opamp Design
   - Cascode
2. A Real Bipolar Opamp
   - Fulgar's 741
   - Simplified 741
   - Dual Electrode Transistors
3. Frequency Dependence in Operational Amplifiers
   - Outline
   - Opamp Intrinsic Frequency Response
   - Bode Plot of O/L Gain for a (fictional) Third Order Opamp
   - Reading the Bode Plot
   - Engineering a First Order Open Loop Response
4. Review
5. Bear



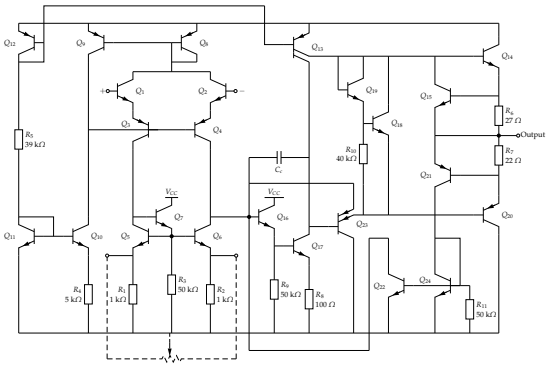
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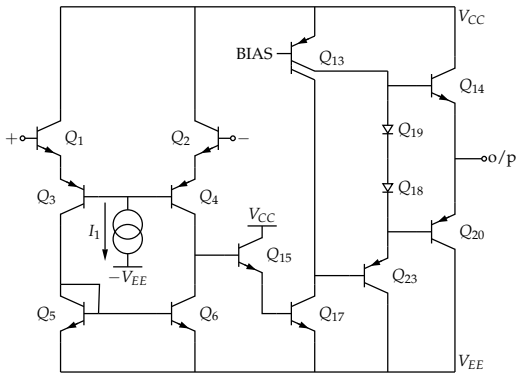
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"Full" 741 Schematic[1]



[1] A little history: http://goo.gl/SpvgZL

Simplified 741



Qualitative 741 Description I

- The input transistors Q1 and Q2 are emitter followers that maintain high input resistance, and low input current.
- Q1 and Q2 drive Q3 and Q4 which are a *common base* differential pair of pnp transistors.
- Q5 and Q6 are a current mirror that actively loads Q3 and Q4.

These six devices perform three key functions of an opamp.

1. They provide the differential input with high r_{in}, with high CMRR and some gain. A little gain in the input stage is desirable from a noise and offset perspective.
2. Level shifting. pnp transistors in standard bipolar IC tech. are slow[2]. We would like to use only npn, but this limits the available output voltage. In the 741 lateral pnps Q3 and Q4 are placed in the signal path, their emitter is near the input voltage but their collectors are almost on the negative rail.

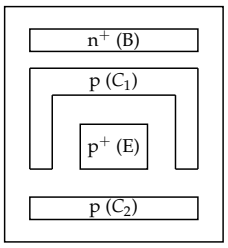
[2] Gray, Hurst, Lewis & Meyer, 4th Ed. Section 2.5.2.

Qualitative 741 Description II

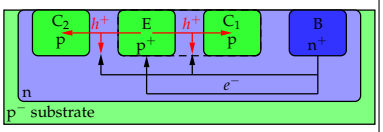
1. Differential input and single ended output. Most modern opamps are differential input single ended output. A simple approach would be to take the output from Q3's collector and resistively load the Q3 & Q4 pair but this lowers the differential pair gain and lowers cripples the CMRR therefore the active load (current mirror) of Q5 and Q6 are used.

- Q16 is an emitter follower (Q16 and Q17 are *not* a Darlington pair). Q16 stops Q17 loading Q4's collector appreciably.
- Q17 is a common emitter amplifer actively loaded by Q13. Q17 provides most of the voltage gain.
- Q23 is also an emitter follower which mitigates the loading effect of the ouptut stage on Q17's collector.
- Q14 and Q20 are a push-pull Class AB output stage (a pair of npn and pnp emitter followers) which provides current gain and a low output impedance.

Dual Electrode Transistors[3,4]



- Collector ring split into two. One facing 3/4 of the emitter the other 1/4 of the emitter.
- essentilly two transistors that share a base and emitter where the saturation current, I_s, is split in the ratio of the collecting area.



- Q13 is a two collector latteral pnp.

[3] IC taredown with pictures at: http://goo.gl/KMNFnW
[4] Camenzind, "Designing Analog Chips", www.designinganalogchips.com

Frequency and Time Domain Limitations of Opamps

In this part of the course we will consider some (but not all) non-idealities of opamps. We will consider the opamp as having an *intrinsic* frequency response and this response will be *first order*. In the frequency domain, we will,

- Introduce the concept of a frequency response.
- Make use of the Bode plot to illustrate the frequency response.
- Discuss the practical significance of poles and zeros.
- Introduce the gain bandwidth product as a measure of small signal performance for an Opamp.
- Briefly touch on the Miller transform.

In the time domain, we will,

- Introduce the idea of slew rate limiting for sine and triangle wave-shapes.

Opamps with Frequency Dependent Feedback

In this part of the course we will consider some circuits which have feedback formed from capacitors and resistors. These circuits will be limited to *first order* problems.

- Integrator circuit
- Differentiator circuit
- Pole-zero circuits

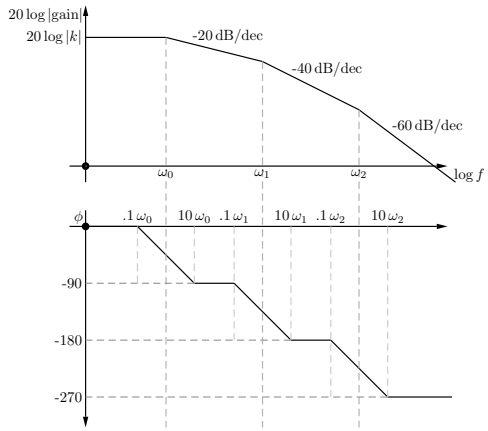
Opamp circuits having higher order feedback, or having first order feedback and a first order intrinsic frequency response (making them second order) are discussed in EEE224 or EEE227 and include second order passive circuits, some types of oscillator, Butterworth and Cheblychev (among other) filters and other non-linear and trans-linear circuits such as mixers and PLLs.

Opamp Intrinsic Frequency Response

- In EEE118 we always assumed A_V was ∞ or a constant real value.
- Making the open loop gain frequency dependent is a way of expressing the intrinsic frequency response of the opamp.
- In EEE225 we assume that A_V is first order, low pass response. Many opamps are designed to "look" first order.
- This design choice is made in order that engineers find opamps easy to work/design with (amplifier lab...).
- To see what effect this design choice has on the performance we will first assume that the opamp is 3rd order.

$$A_v = k \cdot \frac{1}{1+j\frac{\omega}{\omega_0}} \cdot \frac{1}{1+j\frac{\omega}{\omega_1}} \cdot \frac{1}{1+j\frac{\omega}{\omega_2}} \qquad (1)$$

in which k is the frequency independent part of the open loop gain, A_0, and ω_0, ω_1 and ω_2 are the frequencies of three real poles. The lowest is the dominant pole.

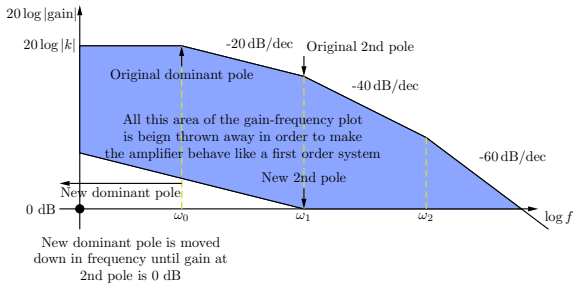


Reading the Bode Plot

Passing a pole when moving from low to high frequencies...

- yields an additional 20 dB/decade roll-off (decrease in amplitude)
- yields an additional 90° phase lag.
- The phase lag at the pole frequency will be 45°.
- The amplitude at the pole frequency will be -3 dB less than the low frequency value.
- The effects of phase shift will extend approximately 10× above and below the pole frequency.

Passing a zero when moving from low to high frequencies yields the same effects but amplitude increases and phase leads. All other points are valid.



The dominant pole is moved down in frequency (sometimes called "slugging") until the 2nd pole frequency is at the unity gain point (0 dB). The blue area is open loop gain which is *lost*.

Review

- Introduced the cascode circuit
- Briefly discussed three simplified schematics of some real opamps.
- Introduced the second section of the course (it's about opamps...)
- Described the open loop gain with a frequency dependence for the first time
- Reminded ourselves how to read a Bode plot
- Discussed how the higher order opamp is made to "look" first order



EEE225: Analogue and Digital Electronics

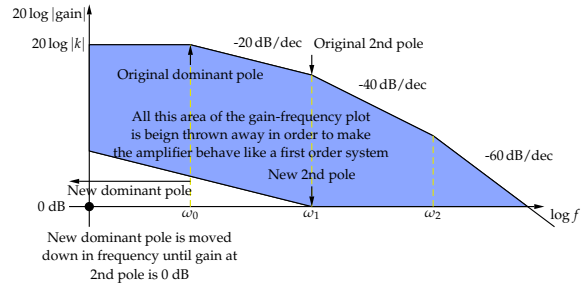
Lecture VII

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This Lecture

1. Frequency Dependence in Operational Amplifiers
   - Engineering a First Order Open Loop Response
2. First Order Opamp Model
   - Model 'Derivation'
   - First Order Bode Plot
   - Key points about the Model
   - 'Easy' example of GBP in a Calculation
   - Exam style example of GBP in a Calculation
3. Miller Transform
   - The Murky tale of Miller Multiplication and Amplifier "Compensation"
4. Review
5. Bear



The dominant pole is moved down in frequency (sometimes called "slugging") until the 2nd pole frequency is at the unity gain point (0 dB). The blue area is open loop gain which is *lost*.

First Order Opamp Model

In EEE118 we developed an equation for the opamp's operation

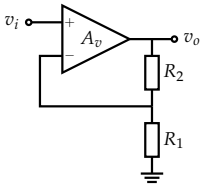
$$V_o = A_v \left(v^+ - v^-\right) \tag{1}$$

We now have an expression for A_v as well

$$A_v = \frac{A_0}{1 + j\frac{\omega}{\omega_0}} \text{ where } \tau = \frac{1}{\omega_0} = \frac{1}{2\pi f_0} \text{ or } f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\tau} \tag{2}$$

where A_0 is the DC open loop gain and ω_0 is the angular corner frequency of the first order system (rads^{-1}).

- A_0 is usually between 10^4 and 10^7
- ω_0 is typically $2\pi \cdot 10$ Hz.



Consider a non-inverting amplifier, we can use the opamp equation (1) to solve for v_o/v_i,

$$\frac{v_o}{v_i} = \frac{1}{\frac{1}{A_v} + \frac{R_1}{R_1+R_2}} = \frac{A_v}{1 + \frac{A_v R_1}{R_1+R_2}} \tag{3}$$

Use an equation for A_v (2) and seek a standard form,

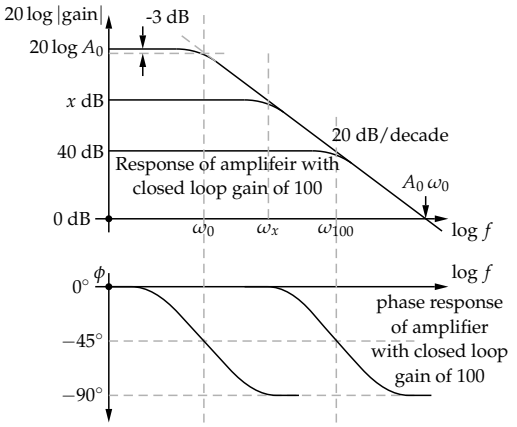
$$\frac{v_o}{v_i} = \frac{\frac{A_0}{1+\frac{A_0 R_1}{R_1+R_2}}}{1 + j\frac{\omega}{\omega_0\left(1+\frac{A_0 R_1}{R_1+R_2}\right)}} \equiv \frac{k_1}{1 + j\,\omega\, k_2} \equiv \frac{k_1}{1 + j\,\frac{\omega}{\omega_2}} \tag{4}$$

$$\text{where } k_1 = \frac{A_0}{1 + \frac{A_0 R_1}{R_1+R_2}} = \text{new d.c. gain} \approx \frac{R_1 + R_2}{R_1} \text{ for } A_0 >> 1 \tag{5}$$

The product $\omega_2\, k_1$ is called the gain-bandwidth product of the amplifier.

$$\omega_2\, k_1 = \omega_0 \left(1 + \frac{A_0\, R_1}{R_1 + R_2}\right) \cdot \frac{A_0}{1 + \frac{A_0 R_1}{R_1+R_2}} = A_0\, \omega_0 \tag{6}$$

So $A_0\,\omega_0$ is constant for a particular opamp. This is a very important result. It means that the product of the d.c. gain and the -3dB bandwidth for a single pole op-amp is independent of the feedback resistor values (and hence closed loop gain) and therefore is a properly of the op-amp itself. We can use this idea to make rapid estimates of bandwidth for a given gain or *vice versa*. The consequence of this constant gain bandwidth product can be visualised in a graph showing amplifiers having several different gains.



Key points about the Model

- The only information given by manufacturers is the gain bandwidth product or the unity gain frequency. Anything else can be calculated by remembering the opamp is assumed to be first order.
- All the roll-offs follow the open loop curve
- Each of the three responses shown exhibits first order behaviour
- For the open loop response, the product of the DC gain and the -3 dB bandwidth is equal to the product of gain and -3 dB frequency for both closed loop gains shown in the last slide.
- For the closed loop gains shown, the product of DC gain and -3 dB frequency is constant and is equal to the unity gain bandwidth of the open loop response.

DC gain × -3 dB bandwidth
= open loop unity gain frequency = constant

Yet more... Key points about the Model

- The first order approximation only applies to non-inverting amplifiers which the manufacture describes as unity gain compensated.
- Real opamps are generally not actually first order. There is often one or more poles associated with each stage (3 stages = 3 poles). If, over the range of frequencies where $A_v > 1$, only one pole dominates then the response will be first order.
- The manufacture often chooses to make the VAS stage pole the dominant one by adding a capacitance between the collector and base of the VAS transistor often between 10 pF and 30 pF.
- The effect of this capacitance is magnified from the VAS's perspective by Miller multiplication.
- Miller multiplication can be described by the Miller Transform.

'Easy' example

You require a gain of 100 from a TL081 (the opamp in the amplifier lab). It has a gain bandwidth product of 3 MHz. What will be the rise time of the circuit be in response to a 10 mV step input?

$$f_{-3\text{dB}} = \frac{3\text{ MHz}}{100} = 30\text{ kHz} \quad (7)$$

$$\text{time constant, } \tau = \frac{1}{\omega_0} = \frac{1}{2\pi f_0} \quad (8)$$

$$= \frac{1}{2\,\pi\,30\text{ kHz}} \quad (9)$$

$$\text{rise time } = 2.2\,\tau \quad (10)$$

$$\text{rise time } = 2.2 \cdot 4 = 11.17\ \mu\text{s} \quad (11)$$

Exam style example - part 1

A particular amplifier with a dc gain of 100 V/V is observed by experiment to behave like a first order system. Measurement shows that the magnitude of amplifier gain has dropped to -6 dB at a frequency of 120 kHz. Calculate the -3 dB frequency.

The amplifier is first order so it will obey

$$\frac{v_o}{v_i} = k\,\frac{1}{1 + j\,\frac{\omega}{\omega_0}} \text{ where } k = 100. \quad (12)$$

$$\left|\frac{100}{1 + j\,\frac{120\times10^3}{f_0}}\right| = 50 \text{ or } \frac{1}{1 + \left(\frac{120\times10^3}{f_0}\right)^2} = \left(\frac{1}{2}\right)^2 \quad (13)$$

$$\sqrt{4-1} = \frac{120\times10^3}{f_0} = 1.73,\ f_0 = \frac{120\times10^3}{1.73} = 69.4\text{ kHz} \quad (14)$$

$$\text{GBP} = 100 \cdot 69.4\text{ kHz} = 6.94\text{ MHz} \quad (15)$$

Exam style example - part 2

A different amplifier also having a dc. gain of 100 V/V has a GBP of 100 kHz. Evaluate the |gain| and phase shift of this amplifier at 75 kHz.

We can use the GBP to get the -3 dB frequency. $f_0 = 100$ kHz / 100 $\therefore f_0 = 1$ kHz.

$$\frac{v_o}{v_i} = k\,\frac{1}{1 + j\,\frac{\omega}{\omega_0}} = \frac{100}{1 + j\,\frac{f}{1\times10^3}} \quad (16)$$

$$\text{At 75 kHz, } |A| = \left|\frac{v_o}{v_i}\right| = \frac{100}{\left[1+\left(\frac{75}{1}\right)^2\right]^{\frac{1}{2}}} \tag{17}$$

$$\left|\frac{v_o}{v_i}\right| = 1.333\dot{3} \text{ V/V or } 2.498 \text{ dBV} \tag{18}$$

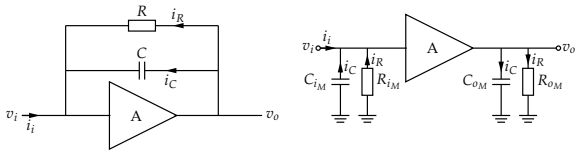
$$\text{The phase shift, } \theta = \angle\left(\frac{v_o}{v_i}\right) = -\tan^{-1}\left(\frac{f}{f_0}\right) \tag{19}$$

$$= -\tan^{-1}\left(\frac{75}{1}\right) = -89.236^\circ \tag{20}$$

Where does the minus sign come from in (19)? "Proper" derivation of argument of complex number needed... Biscuits for correct answers!

Miller Transform

For the two generic amplifier circuits with RC feedback (below), the Miller transform aims to find the effective value of C and R from the point of view of the amplifier's input source and the amplifier's load. The effective values of C and R become C_{o_M} and R_{o_M} for the output and R_{i_M} and C_{i_M} for the input. In other words, find a value of C_{i_M} and R_{i_M} which makes $\frac{v_i}{i_i}$ the same for both circuits. Similar arguments with R_{o_M} and C_{o_M} for $\frac{v_o}{i_o}$.



In the feedback amplifier,

$$i_R = \frac{v_o - v_i}{R} \text{ and } i_C = (v_o - v_i)\, j\omega C \tag{21}$$

In the Miller transformed amplifier, for i_R,

$$i_R = \frac{0 - v_o}{R} = -\frac{v_i}{R_{i_M}} \text{ or } \frac{A\,v_i - v_i}{R} = -\frac{v_i}{R_{i_M}} \tag{22}$$

$$\text{so } R_{i_M} = \frac{R}{1-A} \tag{23}$$

and for i_C

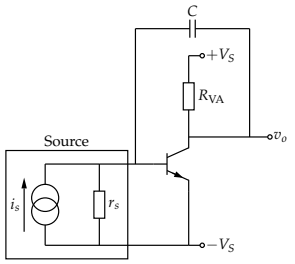
$$i_C = (v_o - v_i)\, j\omega C = -v_i\, j\omega C = -v_i j\omega C_{i_M} \tag{24}$$

$$\text{so } C_{i_M} = C\,(1-A) \tag{25}$$

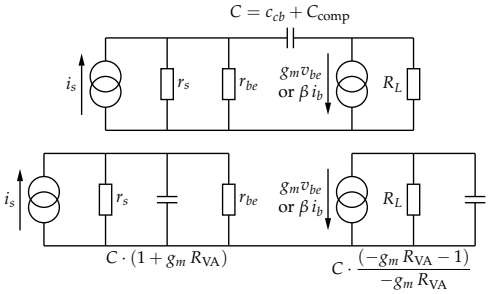
Using a similar analysis, the value of R to ground at the output is $R_{o_M} = (A/(A-1)) \cdot R$ and the value of C to ground is $C_{o_M} = ((A-1)/A) \cdot C$.

Miller Multiplication and the VAS

From the point of view of the signal source, the feedback impedance is $(1-A)$ times lower than the component face value. In the amplifier on the right, the feedback capacitor's value is effectively multiplied by $(1-A)$. This is the Miller multiplication. The gain of this amplifier is approximately $-g_m R_{\text{VA}}$, so the apparent value of the capacitor is increased by $(1 - -g_m R_{\text{VA}})$. For 500 μA quiescent current and R_{VA} a quite conservative 50 kΩ, if $C = 33$ pF its apparent value will appear as 326 nF. We use the Miller effect to our advantage when lowering the pole frequency of the VAS...



- $(1 - -g_m R_{\text{VA}})$ is usually large, especially if the VAS is a Darlington (could be > 50000).
- If the VAS *is* a Darlington then r_{be} will be very large, this gives rise to a very long time constant, τ, as seen from the output of the differential stage.



Review

- Reminded ourselves how to read a Bode plot.
- Discussed how the higher order opamp is made to "look" first order.
- Developed an expression for the open loop gain as a first order low pass system.
- Introduced the idea of gain bandwidth product.
- Did a simple example GBP / rise time calculation.
- Noted some key points about the first order model.
- Developed the idea that the VAS's c_{cb} is increased in order to compensate the amplifier.
- Introduced the Miller Transform, considered the advantage brought by the Miller Effect for dominant pole positioning.



EEE225: Analogue and Digital Electronics

Lecture VIII

James E. Green

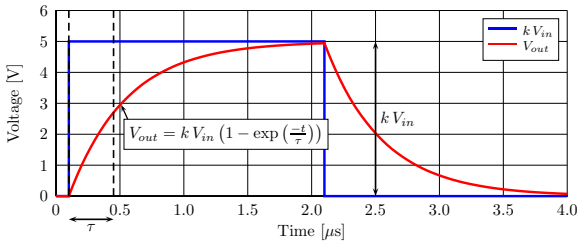
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This Lecture

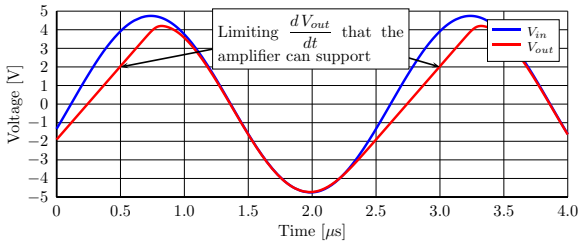
1. Non-Linear Effects
   - Slew Rate Limiting
   - Slew Rate Limiting: Square
   - Slew Rate Limiting: Sine
   - Slew Rate Limiting: Triangle
2. Opamps with Frequency Dependent Feedback
   - Integrator
   - Integrator: Frequency Domain
   - Integrator: Time Domain
   - Problems with Integrators
   - Differentiator
3. Review
4. Bear

Slew Rate Limiting

- Slew rate limiting is *non-linear*, the ratio of v_o and v_i *depends on the magnitude of* v_i. It is a limit on the maximum rate of change of output voltage.
- It is particularly prevalent in problems where large signals and high frequencies are in use.
- It is often caused by the differential pair and VAS current source's inability to charge or discharge the compensation capacitor sufficiently quickly.
- Manufacturers specify in $V/\mu s$. (TL081 8 $V/\mu s$). Specific opamps can manage 5000 $V/\mu s$.
- Opamp manufacturers artificially increase the value of c_{cb} to obtain stability and a first order response. But increasing c_{cb} increases the current needed from the differential stage and VAS current source. It's a *compromise*, greater stability (esp. at lower closed loop gain) comes at the expense of lower slew rate.



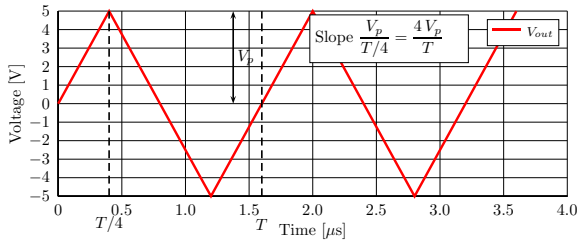
The square input signal interacts with the (low pass) opamp as if the opamp was an RC network. The result is an exponential rise to maximum of the form $V_o = k\,V_{in}\,(1 - \exp t/\tau)$ where $t = 0$ is the rising edge of the square signal, k is the system gain and τ is the time-constant of the opamp. Max rate of change $= (k\,V_{in})/\tau$. If the initial rate of change was maintained the output waveform would cross the setpoint at τ.



Max rate of change of a sinusoid,

$$V_{in}\sin(\omega t) = \left.\frac{d\left(V_{in}\sin(\omega t)\right)}{dt}\right|_{max} = V_{in}\,\omega\cos(\omega t)|_{max} \qquad (1)$$

Max when $cos(\omega\, t) = 1$. Max dV/dt for sinusoid is $V_{in}\,\omega$.



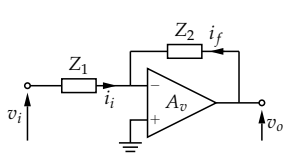
For the triangle the rate of change of voltage is constant. In the graph above the amplifier must change it's output voltage by V_p in a time, $T/4$ where T is the period. For example if $V_p = 5$ V and $T = 1.6$ μs the slew rate must be $\geq \frac{4\times5}{1.6\times10^{-6}}$V/s or 12.5 V/$\mu$s

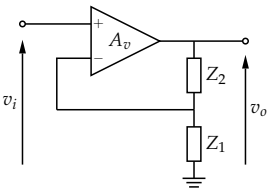
Opamps with Frequency Dependent Feedback

Part II of the second section of the course...

- Introduction of simple general opamp amplifier (Z_1, Z_2, not R_1, R_2)
- An analogue integrator
  - Freq domain analysis
  - Time domain analysis
  - Problems with integrators
  - Analogue circuit to solve 1st order differential equation (printed notes)
- An analogue differentiator
  - Freq domain analysis
  - Time domain analysis
  - Problems with differentiators
- Pole-Zero Circuits.
  - Description of first order circuits (HP, LP, PZ)
  - Example with defined components
  - Example of intrinsic freq response type problem

Some Standard opamp circuits





Inverting design gain...

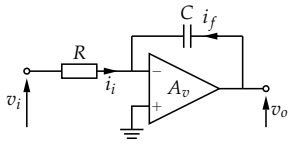
$$\frac{v_o}{v_i} = -\frac{Z_2}{Z_1} \quad (2)$$

Non-inverting design gain...

$$\frac{v_o}{v_i} = \frac{Z_1 + Z_2}{Z_1} \quad (3)$$

Provided closed loop gain is not dependent on open loop gain (i.e. if $A_v \to \infty$). Z_n is an arbitrary impedance (could be R, L and C).

Opamp Integrator

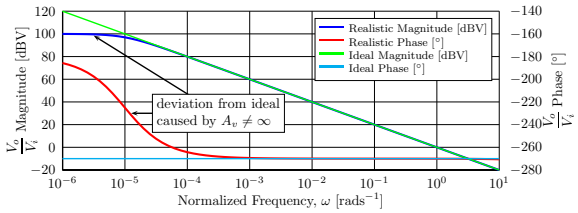


In the frequency domain.

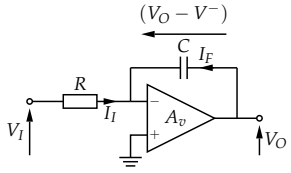
$$\frac{v_o}{v_i} = -\frac{Z_2}{Z_1} \quad (4)$$

$$\frac{v_o}{v_i} = -\frac{\left(\frac{1}{j\,\omega\,C}\right)}{R} = -\frac{1}{j\,\omega\,C\,R} \quad (5)$$

- Integrators used in filters, instrumentation circuits and in control systems, but not often implemented using an opamp.
- Often $j\,\omega = s$ where 's' is the same as appears in the Laplace transform. So (5) becomes $1/(s\,C\,R)$.
- As ω approached 0 (i.e. DC) the gain $\to \infty$. This can not actually happen as the gain can not rise above A_v



The finite A_v affects performance by moving the pole up from zero frequency to some finite frequency. The graph above is normalised i.e. $C\,R = 10^0$. The usable range of the integrator is about $10^{-3} \to 10^1$ Hz normalised but it depends on the value of A_v to some extent. Care should be taken to avoid phase errors as well as magnitude errors.



In the time domain (notice upper case letters)

$$I_I + I_F = \frac{V_I - V^-}{R} + C\frac{d\,(V_O - V^-)}{dt} = 0 \quad (6)$$

Assuming $V^- \approx 0$

$$\frac{V_I}{R\,C} = -\frac{dV_O}{dt} \quad (7)$$

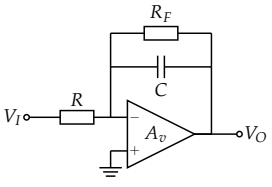
integrating both sides,

$$V_O = -\frac{1}{R\,C}\int V_I\,dt + A \quad (8)$$

A is a constant proportional to the voltage across the capacitor prior to the start of the integration.
Integrators have a major problem however, called "wind-up".

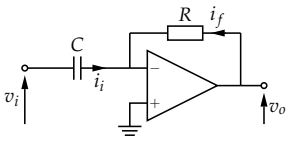
- There is no DC feedback between output and input.
- Any small voltage (offset of the opamp or offset of the signal source) is integrated over time.
- Eventually the integrator output will saturate against one of the power supply rails.

This can be avoided by providing DC feedback either as part of a larger system or more directly using a resistor.



The result of the DC pathway (R_F) is to change the gain of the circuit from $-A_0$ at DC to $-R_F/R$. This moves the pole up in frequency, decreasing the useful frequency range of the integrator.

Opamp Differentiator



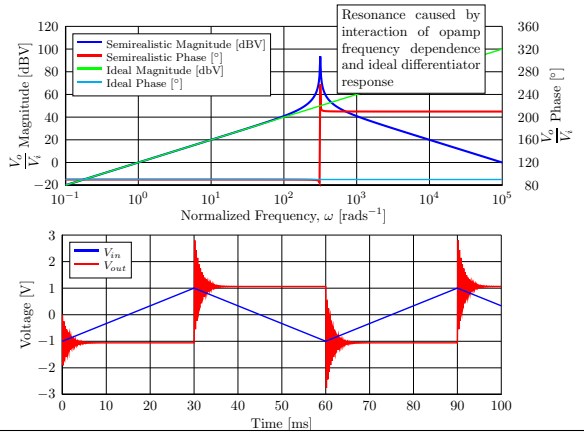
In the frequency domain.

$$\frac{v_o}{v_i} = -j\,\omega\,C\,R = -s\,C\,R \quad (9)$$

In the time domain,

$$V_O = C\,R\,\frac{dV_I}{dt} \quad (10)$$

- Key components interchanged. Same assumptions as for integrator. Same style of analysis.
- The capacitance and intrinsic frequency response of the opamp (A_v) interact with each-other forming (in the case of first order opamp assumptions) a second order circuit. This makes the differentiator unusable for a few decades of frequency around resonance.



Review

- Discussed slew rate limiting, a non-linear effect which depends on signal magnitude. Examples for square, sine and triangle given.
- Introduced two opamp circuits for integration and differentiation of signals using resistors and capacitors as gain setting components.
- Considered some limitations and impracticalities of both circuits including the interaction between the intrinsic frequency response of the opamp and the frequency dependent feedback.



EEE225: Analogue and Digital Electronics

Lecture IX

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This Lecture

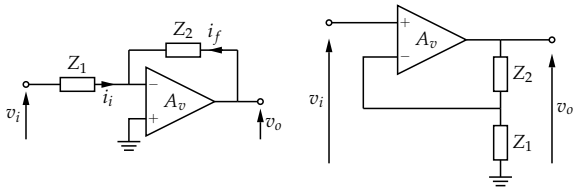
1 Opamps with Frequency Dependent Feedback
- Pole-Zero Circuits
- Passive and Active First Order Circuits: Standard Forms
- Passive and Active First Order Circuits: Low Pass with 'k'
- Low Pass with 'k': Time and Frequency Domain Response
- Passive and Active First Order Circuits: High Pass with 'k'
- High Pass with 'k': Time and Frequency Domain Response
- Pole-Zero Response
- Passive PZ example: Getting the Standard Form...
- Active PZ example: Getting the Standard Form...

2 Review

3 Bear

Pole-Zero Circuits

Pole-zero circuits aim to adjust the magnitude and phase response of an analogue system. They are constructed from the standard amplifier blocks but with Z_1 or Z_2 having some frequency dependent components - almost always capacitors. Inductors are too imperfect[1]



[1] If an inductance is required, it may be manufactured with a capacitance and an opamp or two forming a gyrator, a kind of impedance transformer. See http://sound.westhost.com/articles/gyrator-filters.htm for examples.

Standard Forms

First order transfer functions fall into one of three standard forms, low pass,

$$\frac{v_o}{v_i} = k\frac{1}{1+s\tau} = k\frac{1}{1+j\frac{\omega}{\omega_0}} = k\frac{1}{1+j\frac{f}{f_0}} \tag{1}$$

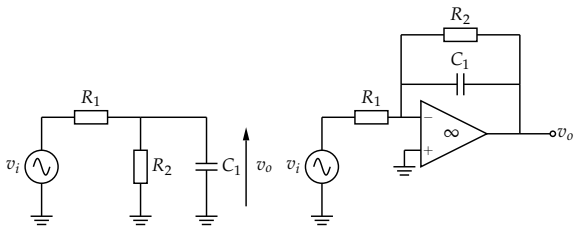
high pass,

$$\frac{v_o}{v_i} = k\frac{s\tau}{1+s\tau} = k\frac{j\frac{\omega}{\omega_0}}{1+j\frac{\omega}{\omega_0}} = k\frac{j\frac{f}{f_0}}{1+j\frac{f}{f_0}} \tag{2}$$

and pole zero,

$$\frac{v_o}{v_i} = k\frac{1+s\tau_1}{1+s\tau_0} = k\frac{1+j\frac{\omega}{\omega_1}}{1+j\frac{\omega}{\omega_0}} = k\frac{1+j\frac{f}{f_1}}{1+j\frac{f}{f_0}} \tag{3}$$

Passive and Active First Order: Low Pass with 'k'



For the passive circuit:

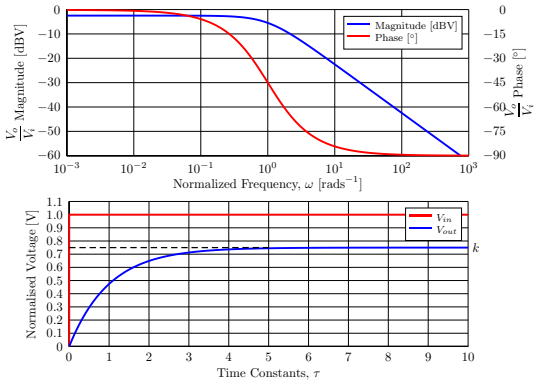
$$\frac{R_2}{R_1+R_2}\cdot\frac{1}{s\,C_1\,(R_1//R_2)+1} \tag{4}$$

For the active circuit:

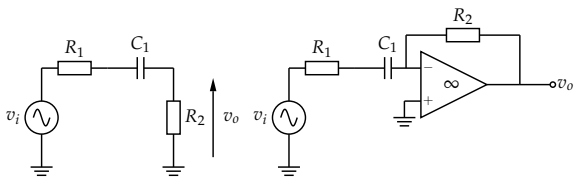
$$-\frac{R_2}{R_1}\cdot\frac{1}{s\,C_1\,R_2+1} \tag{5}$$

They are not identical! but they are similar in the shape of the frequency response.

Time and Frequency Domain Response (Passive Version)



Passive and Active First Order: High Pass with 'k'



For the passive circuit:

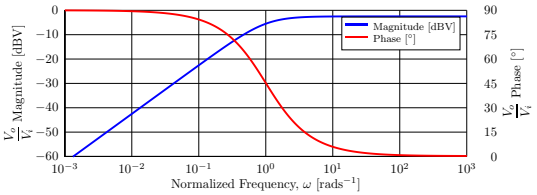
$$\frac{R_2}{R_1+R_2}\cdot\frac{s\,C_1\,(R_1+R_2)}{s\,C_1\,(R_1+R_2)+1} \tag{6}$$

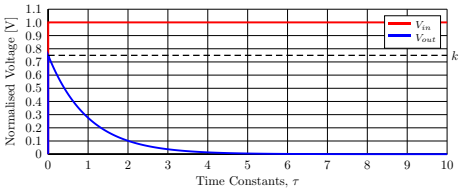
For the active circuit:

$$-\frac{R_2}{R_1}\cdot\frac{s\,C_1\,R_1}{s\,C_1\,R_1+1} \tag{7}$$

They are not identical! but they are similar in the shape of the frequency response.

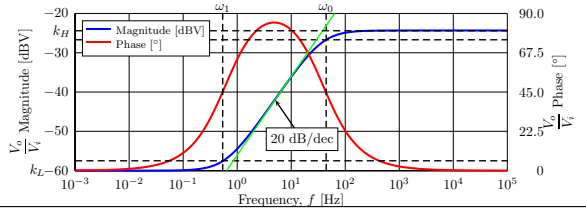
Time and Frequency Domain Response (Passive Version)





Passive and Active First Order: Pole-Zero (or Zero-Pole)

- The PZ system is the linear sum of HP and LP
- There is one pole and one zero.
- The pole may appear at a lower or higher frequency than the zero. The circuit is called pole-zero regardless!
- The pole determines the time constant, τ
- Occasionally may be called lead or lag compensator in control systems discussion.



- There are two "gains" a low frequency (or DC, $f \to 0$) gain and a high frequency ($f \to \infty$) gain, k_L and k_H respectively.
- If zero frequency (ω_1) < pole frequency (ω_0) then $k_L < k_H$ and phase "leads" (+ ve) between the pole and zero. This is the case in the last slide.
- If the zero frequency (ω_1) > pole frequency (ω_0) then $k_L > k_H$ and phase "lags" (- ve) between the pole and zero.
- Magnitude slope tends to $\pm$20 dB/dec as the system is first order. Phase tends to +90 or -90 depending on PZ or ZP but often does not make it all the way.

Standard Forms:
frequency domain:

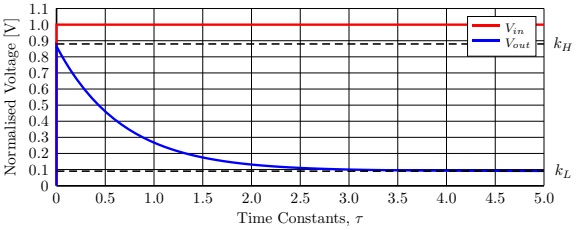
$$k\,\frac{1+s\,\tau_1}{1+s\,\tau_0} \tag{8}$$

Alternatively:

$$k\cdot\frac{1}{1+s\,\tau_0}+k\cdot\frac{\tau_1}{\tau_0}\cdot\frac{s\,\tau_0}{1+s\,\tau_0} \tag{9}$$

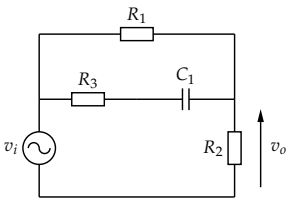
- The high frequency gain, $k_H = k\cdot\frac{\tau_1}{\tau_0}$ and $k = k_L$.

The step response depends on which of the pole or zero are at the lower frequency but for zero frequency < pole frequency we have something that is broadly HP looking but v_{out} does not fall to zero, it tends towards k_L. For zero frequency > pole frequency we have something broadly LP but also having a finite k_H.



Passive Pole-Zero Example

Find the transfer function of the following PZ circuit.



- Notice k is at the front and has no ω dependence.
- The s^0 (unity) coefficient is 1 in the numerator and denominator.
- The highest power of s is one.
- Always ask yourself, what is HF gain? what is LF gain? (good sanity check)...

$$k\cdot\frac{s\,\tau_1+1}{s\,\tau_0+1}=\frac{R_2}{R_1+R_2}\cdot\frac{s\,C_1\,(R_1+R_3)+1}{s\,C_1\left(\frac{R_2\,R_1+R_2\,R_3+R_1\,R_3}{R_1+R_2}\right)+1} \tag{10}$$

It's a potential divider with R_2 developing the output voltage,

$$v_o = \frac{R_2\, v_i}{R_2 + R_1 \,//\, \left(R_3 + \frac{1}{s\,C_1}\right)} \tag{11}$$

Expanding,

$$\frac{v_o}{v_i} = \frac{R_2}{R_2 + \frac{R_1\left(R_3 + \frac{1}{s\,C_1}\right)}{R_1 + R_3 + \frac{1}{s\,C_1}}} \tag{12}$$

Need to head towards $1 + s\,\tau$ on the bottom. Multiply top (numerator) and bottom (denominator) by $R_1 + R_3 + \frac{1}{s\,C_1}$

$$\frac{R_2\left(R_1 + R_3 + \frac{1}{s\,C_1}\right)}{R_2\left(R_1 + R_3 + \frac{1}{s\,C_1}\right) + R_1\left(R_3 + \frac{1}{s\,C_1}\right)} \tag{13}$$

Multiplying out the brackets (expanding),

$$\frac{R_2\,R_1 + R_3\,R_2 + \frac{R_2}{s\,C_1}}{R_2\,R_1 + R_3\,R_2 + \frac{R_2}{s\,C_1} + R_1\,R_3 + \frac{R_1}{s\,C_1}} \tag{14}$$

Multiplying top and bottom by $s\,C_1$,

$$\frac{(R_2\,R_1 + R_3\,R_2)\,s\,C_1 + R_2}{s\,C_1\,R_2\,(R_1 + R_3) + R_2 + R_1\,R_3\,s\,C_1 + R_1} \tag{15}$$

The unity term (coefficient of s^0) in the denominator is $R_1 + R_2$. So lets divide top and bottom by $R_1 + R_2$ to get $s\,\tau + 1$ on the bottom.

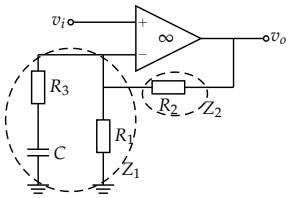
$$\frac{s\,C_1\frac{R_2(R_1+R_3)}{R_1+R_2} + \frac{R_2}{R_1+R_2}}{s\,C_1\frac{(R_2\,R_1+R_2\,R_3+R_1\,R_3)}{R_1+R_2} + 1} \tag{16}$$

Having found the desired form of the denominator we know the pole has a time-constant, $\tau_0 = C_1\frac{(R_2\,R_1+R_2\,R_3+R_1\,R_3)}{R_1+R_2}$. The numerator is still not in the right form though as it must be $1 + s\,\tau_1$. We need to divide the numerator by the numerator's present coefficients of s^0, which are $\frac{R_2}{R_1+R_2}$. We can't change the denominator though, it is already in the desired form, so we are unbalancing our expression. k, the frequency independent gain, will restore balance by becoming the unity coefficients of the numerator, $\frac{R_2}{R_1+R_2}$.

$$\frac{\frac{R_2}{R_1+R_2}\cdot\left(s\,C_1\cdot\frac{\cancel{R_2}\,\cancel{(R_1+R_3)}}{\cancel{R_1+R_2}}\cdot\frac{\cancel{R_2}}{\cancel{R_1+R_2}} + \frac{\cancel{R_2}}{\cancel{R_1+R_2}}\right)}{s\,C_1\frac{(R_2\,R_1+R_2\,R_3+R_1\,R_3)}{R_1+R_2} + 1} \tag{17}$$

Performing the cancellations in (17) and bringing k outside of the fraction yields (10).

Active Pole-Zero Example



HF gain: (at HF, C $\to$ 0 Ω)

$$\frac{v_o}{v_i} = \frac{R_2 + (R_1//R_3)}{R_1//R_3} \tag{18}$$

LF gain: (at LF, C $\to \infty$ Ω)

$$\frac{v_o}{v_i} = \frac{R_2 + R_1}{R_1} \tag{19}$$

This is a standard non-inverting amplifier which has the gain expression:

$$\frac{v_o}{v_i} = \frac{Z_2 + Z_1}{Z_1} = \frac{R_2 + R_1 \,//\, \left(R_3 + \frac{1}{j\,\omega\,C}\right)}{R_1 \,//\, \left(R_3 + \frac{1}{j\,\omega\,C}\right)} \tag{20}$$

$$\frac{R_2 + \frac{R_1\left(R_3+\frac{1}{j\,\omega\,C}\right)}{R_1+R_3+\frac{1}{j\,\omega\,C}}}{\frac{R_1\left(R_3+\frac{1}{j\,\omega\,C}\right)}{R_1+R_3+\frac{1}{j\,\omega\,C}}} \tag{21}$$

Multiply top and bottom by $j\,\omega\,C$,

$$\frac{R_2 + \frac{R_1\,(R_3\,j\,\omega\,C+1)}{1+j\,\omega\,C(R_1+R_3)}}{\frac{R_1\,(R_3\,j\,\omega\,C+1)}{1+j\,\omega\,C(R_1+R_3)}} \tag{22}$$

Multiply top and bottom by $1 + j\,\omega\,C\,(R_1 + R_3)$,

$$\frac{R_2\,(1 + j\,\omega\,C\,(R_1 + R_3)) + R_1\,(1 + j\,\omega\,C\,R_3)}{R_1\,(1 + j\,\omega\,C\,R_3)} \tag{23}$$

Collecting terms,

$$\frac{R_1 + R_2 + j\,\omega\,(R_2\,R_1 + R_2\,R_3 + R_1\,R_3)\,C}{R_1\,(1 + j\,\omega\,C\,R_3)} \tag{24}$$

Taking k outside, and comparing terms with the standard form,

$$\frac{R_1 + R_2}{R1}\cdot\frac{1 + j\,\omega\,C\left(\frac{R_2\,R_1+R_2\,R_3+R_1\,R_3}{R_1+R_2}\right)}{1 + j\,\omega\,C\,R_3} \equiv k\frac{1 + j\,\omega\,\tau_1}{1 + j\,\omega\,\tau_0} \equiv k\,\frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_0}} \tag{25}$$

$$f_1 = \frac{R_1 + R_2}{2\,\pi\,C\,(R_1\,R_2 + R_2\,R_3 + R_1\,R_3)} \tag{26}$$

$$f_0 = \frac{1}{2\pi\,C\,R_3} \tag{27}$$

$$k = \frac{R_1 + R_2}{R_1} \tag{28}$$

when $\omega >> 2\pi f_1$ and $2\pi f_0$ (i.e. at high frequencies), the 1s are negligible compared to the f terms,

$$\left|\frac{v_o}{v_i}\right| = k\left|\frac{\cancel{1^2} + \left(\frac{f}{f_1}\right)^2}{\cancel{1^2} + \left(\frac{f}{f_0}\right)^2}\right|^{\frac{1}{2}} = k\,\frac{\frac{f}{f_1}}{\frac{f}{f_0}} = k\,\frac{f_0}{f_1} \tag{29}$$

$$k\,\frac{f_0}{f_1} = \frac{\cancel{R_1 + R_2}}{R_1} \cdot \frac{\frac{1}{\cancel{2\pi C} R_3}}{\frac{\cancel{R_1+R_2}}{\cancel{2\pi C}(R_1 R_2 + R_2 R_3 + R_1 R_3)}} \tag{30}$$

$$\frac{R_1 R_2 + R_2 R_3 + R_1 R_3}{R_1 R_3} = \frac{R_1 R_2 + R_2 R_3}{R_1 R_3} + 1 \tag{31}$$

$$R2\left(\frac{R_1 + R_2}{R_1 R_3}\right) + 1 = \frac{R2}{R_1 // R_3} + 1 = \frac{R_2 + R_1 // R_3}{R_1 // R_3} \tag{32}$$

Compare (32) with (18). At low frequencies, $\omega << 2\pi f_1$ and $2\pi f_0$, the 1s dominate the f terms, and gain $\rightarrow k$.

Review

- Revisited some EEE117 material on frequency and time domain response of first order LP and HP systems.
- Noted that the Pole-Zero circuit is a combination of the LP and HP first order circuits.
- Enumerated some key points about the pole zero circuit/system including:
  - There is one pole and one zero
  - The pole can be found at a lower frequency than the zero or *vice versa*.
  - The pole determines the time constant, τ.
  - sometimes called "lead/lag compensation circuits".
- Examined a passive network pole zero circuit similar to EEE117
- Examined an active, opamp based, pole zero circuit.



EEE225: Analogue and Digital Electronics

Lecture X

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This Lecture

1. Introduction to Electronic Noise
   - Books About Noise in Circuits
   - Noise Overview
   - Sources of Noise
   - Quantifying Noise: Amplitude Distribution
   - Quantifying Noise: Frequency Distribution
   - Internal Noise Sources: Johnson-Nyquist Noise
   - Internal Noise Sources: Shot Noise
   - Internal Noise Sources: Flicker Noise
2. Noise in Circuits
   - Maximum Available Noise Power
   - Combining Noise Sources
   - Effect of a parallel RC network on White Noise
   - Noise Temperature
3. Review
4. Bear

Books/Papers about Noise

No need to buy any of these but good idea to know they exist.

1. Motchenbacher, C. D., and Connelly, J. A., Low-Noise Electronic System Design.
2. Books authored by Albert Van der Ziel (e.g. "Noise" and "Noise in Solid State Devices and Circuits" (1950's - 1980's try Abebooks)
3. Leach Jr., W. M., Fundamentals of Low-Noise Electronics[1]
4. W. M. Leach, Jr., Fundamentals of Low-Noise Analog Circuit Design, Proceedings of the IEEE, Vol. 82, No. 10, pp. 1515-1538, Oct. 1994. `http://dx.doi.org/10.1109/5.326411`.

[1] Quite inexpensive (as text books go) and comprehensive. Buy direct from publisher, Kendal-Hunt, 2012. Avoid the e-book! `www.kendallhunt.com`.

In this part of the course we will discuss

- Sources of noise in circuits/devices
- Methods for quantifying noise
- Limits on the available noise power
- Methods of combining noise sources in circuit analysis
- The effects of RC circuits on noise
- Noise in systems of circuits
  - Signal to noise ratio
  - Noise figure & noise factor
- Equivalent circuits for performing circuit analysis with noise sources
- Noise in Opamps

Note: Nothing will be said about BJTs or FETs and nothing about the effects of noise in oscillators. This is not an exhaustive treatment...

Noise produced by Human Activity

Noise is a term used to describe an unwanted signal regardless of origin. In general there are three sources of noise. First: Noise produced by human activity ("man-made"), this includes:

- Radio signals that are accidentally picked up.
- EMI from machines (especially brushed or AC machines)
- Poorly designed or laid out power electronics systems
- Switching Converters
- Hum Loops: poor current return path design/layout etc.

Noise produced by humans can be reduced by cunning design methods. Legislation (OFCOM, FCC etc.) exists to define how much EMI may be generated by certain devices and how much interference certain electronic systems must be able to withstand and still work properly (medical electronics especially).

Natural Sources of Electronic Noise

Natural External:

- Environmental sources such as lightning strikes (produces copious EMI)
- High energy cosmic rays.

External sources may be treated with the same methods as noise produced by human activity

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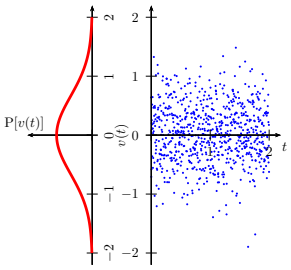
Natural Internal: This is the hiss one hears when an audio amplifier is turned up to 11 without any program material being played. It is caused by the random motion of individual electrons in components and it's what concerns us in this course. Resistors, diodes and transistors are sources of noise. *Imperfect* capacitors and inductors are also sources of noise however we do not usually treat them except in special circumstances.

Noise Amplitude Distribution

On a CRO noise is an irreducible fuzz. It doesn't have any period. Changing the timebase doesn't change its shape. As we approach the CRO bandwidth the noise appears to possess some coherence but this is a limitation of the measurement equipment and is not real. A CRO can't be meaningfully triggered from a noise signal.

$$\frac{1}{t}\int_0^t v_n(t)\,\mathrm{d}t. \to 0 \text{ as } t \to \infty$$

The value of the noise at any time provides no information about other times. The idea of "amplitude" as a metric of noise is therefore not very helpful.



- Despite having an average value of zero, the instantaneous value may not be zero so noise signals can dissipate *power*. We use this to express the quantity of noise in a meaningful way.
- Power dissipated is proportional to the "mean square" value of the noise voltage v_n or noise current i_n, $\overline{v_n^2}$ and $\overline{i_n^2}$ which have units of V^2 or A^2.
- The root mean square can also be used $\sqrt{\overline{v_n^2}}$ with units of V. (square it first, then mean, then root...)
- Occasionally you may read[2] about "crest factor". Crest factor is used as a statistical measure of the likelihood of finding a noise value above a certain threshold from the mean. For example, a Gaussian noise amplitude distribution has a peak value more than 4.9 times the RMS value only 0.0001% of the time. This is only a statistical measure, noise may take any instantaneous value.

[2] yes, you have to *read* about electronics.

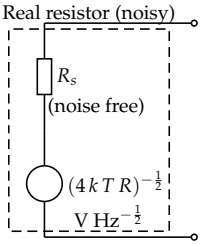
Noise Frequency Distribution

- Certain noise processes inside electronic devices are effective at different frequencies.
- That is to say, the mean square value of noise changes as a function of f.
- This is not related to the amplitude distribution (Gaussian, Poison etc.)
- To assess the effect of frequency dependent noise we use "noise power spectral density" - think spectrum as in radio spectrum and spectrum analyser.
- Power spectral density is the mean squared noise amplitude *per Hz* (i.e. in one unit of frequency or bandwidth). Measured in V^2/Hz "volts squared per Hertz" or $V/\sqrt{Hz}$ "volts per root Hertz". It is how we commonly describe noise sources.

Johnson noise is caused by the random motion of electrons in resistive media. It has constant power spectral density - "white" because all frequencies are represented equally, as in white light and can be modelled by a Thévenin source, in which the voltage represents the noise v_n and the series resistor is a noise free equivalent of the resistance being modelled.

$$\overline{v_n^2} = 4\,k\,T\,R \ \ \mathrm{V^2/Hz} \quad (1)$$
$$= 4\,k\,T\,R\,\Delta f \ \ \mathrm{V^2} \quad (2)$$

where k is Boltzmann's constant, T is the absolute temperature, R is the resistance and Δf is the bandwidth of the measurement. Thermal noise is *not* generated by incremental resistances such as r_{be}.

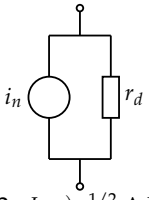


Shot Noise

Shot noise is caused by the discontinuous nature of current flowing in pn junctions and thermionic valves. It has a constant power spectral density (it is "white"). and is modelled by a Norton source in parallel with a resistance which models the dynamic resistance of the pn junction. Since it is an incremental resistance it is noise free.

$$\overline{i_n^2} = 2\,q\,I_{DC} \ \ \mathrm{A^2/Hz} \quad (3)$$
$$= 2\,q\,I_{DC}\,\Delta f \ \ \mathrm{A^2} \quad (4)$$

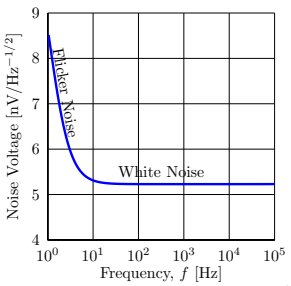
where q is the magnitude of the electron charge, I_{DC} is the quiescent or large signal current in the junction and Δf is the bandwidth of the measurement.



$$i_n = (2\,q\,I_{DC})^{-1/2}\ \mathrm{A\,Hz^{-1/2}}$$

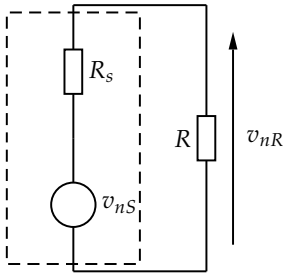
Flicker noise also called 1/f affects both resistors and semiconductor devices as well as many other physical processes. The magnitude of 1/f noise is proportional to the magnitude of the DC current flowing in a component and its power spectral density approximately obeys a 1/f relationship. Manufacturers specify 1/f by means of a graph, and often a "corner frequency" where 1/f gives way to white noise. This corner lies at the frequency where $\sqrt{\overline{v_n^2}}$ has risen to 1.4 times it's high frequency value.

It's origins are not properly understood. It appears to be related to process quality as 1/f has reduced as silicon processing has matured in the last 60 years.



Maximum Available Power

Find the maximum power that can be transferred from a noisy resistor to a noise free resistor. Optimum value of R?



$R_s = R$ to yield maximum power transfer. This is from EEE118 lecture 2.

The voltage across R is,

$$v_{nR} = v_{nS}\frac{R}{R+R_s} = \frac{v_{nS}}{2} \quad (5)$$

Power is then,

$$P_R = \frac{\overline{v_{nS}^2}}{4\,R_s} = \frac{4\,k\,T\,R_s}{4\,R_s} = k\,T \quad (6)$$

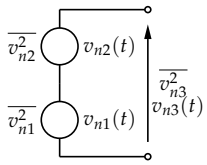
W/Hz or $P_R = k\,T\Delta f$ W.

Power available is therefore independent of R_s.

Combining Noise Sources

We often need to combine several sources of noise to find the total noise voltage between a given node and ground or the total noise current flowing through a branch.

Adding $v_{n2}(t)$ to $v_{n1}(t)$ would be correct, but wouldn't help much...



$$\overline{v_{n3}^2} = \overline{v_{n3}^2(t)} = \overline{(v_{n1}(t)+v_{n2}(t))^2}$$
$$= \overline{v_{n1}^2(t)} + 2\overline{v_{n1}(t)\,v_{n2}(t)} + \overline{v_{n2}^2(t)} \quad (7)$$

$$\overline{v_{n1}^2(t)} = \overline{v_{n1}^2},\ \overline{v_{n2}^2(t)} = \overline{v_{n2}^2} \quad (8)$$

since $v_{n1}(t)$ and $v_{n2}(t)$ are *uncorrelated*,

$$\overline{v_{n1}(t)v_{n2}(t)} = \overline{v_{n1}(t)}\cdot\overline{v_{n2}(t)} \quad (9)$$

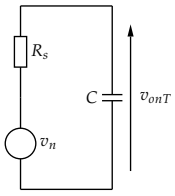
$\overline{v_{n1}(t)}$ & $\overline{v_{n2}(t)} = 0$, $\overline{v_{n1}(t)v_{n2}(t)} = 0$

$$\overline{v_{n3}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} \quad (10)$$

Effect of a Parallel RC network on White Noise

The noise expression $\overline{v_n^2} = 4\,k\,T\,R$ implies an $R_s = \infty\ \Omega \rightarrow \overline{v_n^2} = \infty\ \mathrm{V}^2$, which is not what we observe[3].

$$\overline{v_{onT}^2} = \frac{k\,T}{C} \quad (11)$$



- If v_n is the thermal noise of the resistor, the mean square output is independent of the value of resistance.
- All real resistors have some capacitance in parallel with them. Approximately 1 pF for a 0.25 W resistor.
- Considering only the capacitor, it is in parallel with a resistance of $\infty\ \Omega$.
- Expect $kT/C\ \mathrm{V}^2$ across its terminals.
- Charge transfer can be found from $\overline{q_n^2} = C^2\,\overline{v_n^2}$ because $\overline{q_n^2} = k\,T\,C\ \mathrm{C}^2$.

[3] See pp. 7 of the noise handout or pp. 31 of Motchenbacher & Connelly.

Noise Temperature

- Often devices display more noise than the theory predicts, due to physical manufacturing constraints.
- In resistors (and some other places) this is called "excess noise" (EEE118, Lecture 1).
- One way to account for the extra noise is to adjust the temperature we use in the calculations to a higher value to make up for the extra noise.
- This new temperature is the *effective noise temperature*, T_e.
- Noise temperature often used as a metric of quality for low noise amplifiers esp. in satellite and other microwave applications.
- To obtain the effective noise temperature equate $\overline{v_n^2} = 4\,k\,T_e\,R_s\ \mathrm{V}^2$ so $T_e = \frac{\overline{v_n^2}}{4\,k\,R_s}\ \mathrm{K}$. where $\overline{v_n^2}$ is the combination of all of the noise sources in series with R_s. If it's only R_s, and R_s is noisy but otherwise ideal, $T_e = T$.

Review

- Enumerated some sources of noise.
- Introduced the idea of electronic noise as a random disturbance due to electron motion.
- Considered the problems associated with quantifying noise.
- Introduced the amplitude distribution and the frequency distribution.
- Listed three noise sources commonly found in electronic circuits, discussed colour.
- Derived the total available noise power from a resistance in a specified measurement bandwidth.
- Derived how uncorrelated noise sources should be combined.
- Discussed the effect of low pass filtering a white noise source, and showed something interesting about the noise across a capacitor due to other sources.
- Introduced the concept of effective noise temperature.



EEE225: Analogue and Digital Electronics

Lecture XI

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This Lecture

1. Noise in Electronic Systems
   - Signal to Noise Ratio: A Power Ratio
   - Noise Factor: A Power Ratio
   - Noise Figure
   - Noise Factor of a Two Stage Impedance Matched System
2. Matched System Example
   - Question
   - Solution
3. Review
4. Bear

Noise in Electronic Systems

- Resistors, transistors and diodes add noise to circuits. Inductors and capacitors can shape that noise, but ideal capacitors and inductors do not generate their own noise.
- To combine the contribution for every one using Thévenin and Norton sources is time-consuming and quickly becomes impractical even for small circuits.
- A method of representing the electronic system's observed noise using some simple metrics and a couple of "equivalent" noise generators is highly desirable.
- This lecture focuses on metrics of noise performance in impedance matched systems, which are usually operated above 30 MHz. Unmatched systems in Lecture 12.
- In high frequency work, amplifiers are often thought of in terms of their effect on the signal power, not voltage and current.

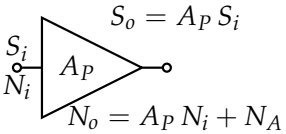
Signal to Noise Ratio: A Power Ratio

- Signal to Noise Ratio is expressed in dB
  $10 \log_{10} \left(\frac{S}{N}\right)$
- 10 log because it is a ratio of powers.
- It is a measure of the signal quality at the point in the system where it is computed. It varies throughout a system.
- It gives no information about the actual quantity of the noise (in $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ for example). It's just a ratio.

- To assess noise performance of a system, compare the Signal to Noise Ratio at the input and output.

$$\frac{S_i}{N_i} = \frac{\text{input signal power}}{\text{input noise power}} \quad (1)$$

$$\frac{S_o}{N_o} = \frac{\text{output signal power}}{\text{output noise power}} \quad (2)$$



Noise Factor: A Power Ratio

Noise Factor is the quotient of the SNR at the input and the SNR at the output

$$F = \frac{\text{signal to noise ratio at input}}{\text{signal to noise ratio at the output}} = \frac{S_i/N_i}{S_o/N_o} \quad (3)$$

If the power gain of the system is A_p:

$$F = \frac{N_o}{A_p N_i} = \frac{\text{output noise power of the real amp.}}{\text{output noise power if the amp. was noiseless}} \quad (4)$$

- The idea of noise factor is useful for multi-stage impedance matched systems (satellite up/downlinks, radar, radio astronomy, cable TV).
- The noise power available at the output of an *ideal* impedance matched system is the input noise power multiplied by the system power gain.

Noise Factor in Unmatched Systems

- In unmatched systems including transistor and operational amplifier systems the idea of "power gain" is not very useful.
- Instead work out the mean square noise voltage (or current) at the nodes of interest - the ratio of mean square voltages is the same as power.
- When working with mean square voltages, the system voltage gain (should it appear) must also be squared or dimensional inconsistency will result.
- The input noise is the mean squared noise voltage (or current) at the input due to the source.
- If noise factor is used in LF systems, it's important to consider if minimising the noise factor is the most desirable outcome - it's not straight forward.

Noise Factor in Matched Systems

The output noise N_o is composed of the amplifier noise N_A and the input noise N_i multiplied by the power gain, A_P. And an ideal amplifier has no noise so its output would be the noise signal entering its input multiplied by its power gain.

$$F = \frac{A_P\, N_i + N_A}{A_P\, N_i} = 1 + \frac{N_A}{A_P\, N_i} \tag{5}$$

If $N_A = 0$, $F = 1$. For an impedance matched system N_i is the available noise input power[1] and F can be written as

$$F = 1 + \frac{N_A}{A_P\, N_i} = 1 + \frac{N_A}{A_P\, k\, T\, \Delta f} \tag{6}$$

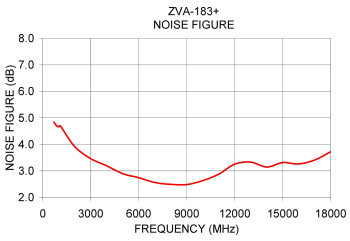
[1] Remember Lecture 10, regarding the maximum available power from one resistor into another.

Noise Figure

The noise figure is simply the noise factor, F, expressed in dB.

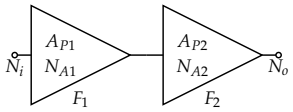
$$\text{Noise Figure, } NF = 10\, \log_{10}\, F \text{ dB} \tag{7}$$

Noise Figure tends to appear on datasheets more often than noise factor for example the RF amplifier datasheet handout. To use this information it is first necessary to convert it to noise factor.



Noise Factor of a Two Stage Impedance Matched System

Many electronic systems consist of a cascade of circuits. This analysis holds for matched systems, but the underlying idea - that the noise of the first stage is the most important - holds generally.



- The available noise at the input is

$$N_i = k\, T\, \Delta f \tag{8}$$

- The noise factor of amplifiers 1 and 2 are

$$F_1 = 1 + \frac{N_{A1}}{A_{P1}\, k\, T \Delta f}\ ,\ F_2 = 1 + \frac{N_{A2}}{A_{P2}\, k\, T \Delta f} \tag{9}$$

The output noise, N_o, has three components:

- Output noise due to the available input noise, N_i

$$N_o|_{N_i} = A_{P1}\, A_{P2}\, N_i = A_{P1}\, A_{P2}\, k\, T\, \Delta f \tag{10}$$

- Output noise due to the noise of amplifier 1, N_{A1}

$$N_o|_{N_{A1}} = A_{P1}\, N_{A1} = A_{P2}\, (F_1 - 1)\, A_{P1}\, k\, T\, \Delta f \tag{11}$$

- Output noise due to the noise added by amplifier 2, N_{A2}

$$N_o|_{N_{A2}} = N_{A2} = (F_2 - 1)\, A_{P2}\, k\, T\, \Delta f \tag{12}$$

- Total *real* amplifier noise N_o (10) + (11) + (12) is,

$$A_{P1}\, A_{P2}\, k\, T\, \Delta f + A_{P1}\, A_{P2}\, (F_1 - 1)\, k\, T\, \Delta f + (F_2 - 1)\, A_{P2}\, k\, T\, \Delta f \tag{13}$$

Which simplifies to,

$$A_{P1}\, A_{P2}\, k\, T\, \Delta f \left(F_1 + \frac{(F_2 - 1)}{A_{P1}}\right) \tag{14}$$

- The noise output from the *ideal* amplifier is just (10).
- so the noise factor is

$$F = \frac{A_{P1}\, A_{P2}\, k\, T\, \Delta f \left(F_1 + \frac{(F_2 - 1)}{A_{P1}}\right)}{A_{P1}\, A_{P2}\, k\, T\, \Delta f} = F_1 + \frac{(F_2 - 1)}{A_{P1}} \tag{15}$$

Conclusions:

- System noise factor is at least equal to the noise factor of the first stage - it is *the* most important.
- The noise factor of the second stage is reduced by a by an amount equal to the first stage power gain before it adds any noise to the system.

Always try to design the first stage to have low noise and high power gain! Much of the noise design effort of LF ICs and microwave components is focused on the first stage. It is where SNR is won and lost.

Matched System Example Question

A wideband amplifier in a matched 50 Ω system is made from two thin film amplifier modules Minicircuits ZVA-183+ followed by ZRON-8G+ with gains of 26.64 dB and 25.64 dB and noise figures of 2.56 dB and 4.29 dB respectively. The amplifier bandwidth of interest spans 1 GHz centred on 7 GHz.

- What is the gain of the series combination?
- What is the noise factor of each amplifier module?
- What is the noise figure of the combination if the ZVA-183+ module is at the input end of the amplifier?
- What is the total added noise power delivered to the load?
- What is the output signal to noise ratio if the input power is 1 pW.
- What is the effective noise temperature of the 50 Ω source resistance?

The maximum available noise power is $k\, T\, \Delta f$ W where Δf is as defined in the question.

Gain and Noise Factor

The gain of the combination is found by adding the individual gains in dB or by converting the gains in dB to linear and then multiplying.

$$A_P = 10\log_{10}\left(10^{(26.64/10)} \cdot 10^{(25.64/10)}\right) \quad (16)$$

$$= 461.32 \cdot 366.44 \quad (17)$$

$$= 1.69045 \times 10^5 \text{ W/W} = 52.28 \text{ dB} \quad (18)$$

The noise factor of the ZVA-183 @ 7 GHz is

$$F_1 = 10^{(2.56/10)} = 1.80302 \quad (19)$$

The noise factor of the ZRON-8G+ @ 7 GHz is

$$F_2 = 10^{(4.29/10)} = 2.6853 \quad (20)$$

Noise Figure of the Combination & Noise Power to the Load

To find the noise figure, first find the noise factor of the combination and then convert to dB. Use,

$$F = F_1 + \frac{F_2 - 1}{A_{P1}} = 1.80302 + \frac{2.6851 - 1}{461.32} = 1.80667 \quad (21)$$

Notice how little effect the noise factor of the second stage ZRON-8G+ has compared to the first stage. The noise figure is,

$$NF = 10\log(1.80667) = 2.5688 \text{ dB} \quad (22)$$

To obtain the noise power to the load we can transpose,

$$F = 1 + \frac{N_A}{A_P N_i} \rightarrow N_A = A_P N_i (F - 1) \quad (23)$$

Noise Power to the Load (continued) & SNR at the Output

F = 1.80667, A_P = 169045, T = 298.15 K (25°C) &
$N_i = k\,T\,\Delta f = 1.38 \times 10^{-23} \cdot 298.15 \cdot 1 \times 10^9 = 4.11447$ pW.
Substituting into (23) yields,

$$N_A = A_P N_i (F - 1) \quad (24)$$

$$N_A = 169045 \cdot 4.11447 \times 10^{-12} \cdot (1.80667 - 1) \quad (25)$$

$$= 5.6519 \text{ nW} \quad (26)$$

To put this in perspective the signal power of the GPS system at the earth's surface is about 10 nW.
The SNR at the output can be obtained by a number of methods (as can many of these solutions), we can use,

$$F = \frac{S_i/N_i}{S_o/N_o} \quad (27)$$

SNR at the Output (continued)

We already know the noise power available at the input is $k\,T\,\Delta f = 4.11447$ pW and the question gives the input power as 1 pW. Compute the SNR at the input,

$$\frac{S_i}{N_i} = \frac{1 \times 10^{-12}}{4.11447 \times 10^{-12}} = 0.24304 \quad (28)$$

Now transpose (27) and substitute in F and (28) to yield,

$$\frac{S_o}{N_o} = \frac{S_i/N_i}{F} = \frac{0.24304}{1.80667} = 0.13452 \quad (29)$$

Comparing the input and output SNR we find the signal more corrupted when leaving the amplifier than when it entered. This is reassuring as it means the amplifier must have added some noise... and we know that it did. 0.13452 = -8.7119 dB (SNR $<$ 1 means the noise is larger than the signal)

Noise Temperature of the Amplifier Cascade

When a resistor equal to the value of the characteristic impedance (50 Ω) is heated to a certain temperature above 0 K it will add to the signal the same noise as our amplifier cascade adds. This temperature is the effective noise temperature of the amplifier. We can take a short-cut (the proof of which I leave to you)...

$$F = 1 + \frac{T_E}{T_A} = 1 + \frac{T_E}{298.15} \quad (30)$$

where T_E is the effective noise temperature of the amplifier and T_A is the actual temperature.

$$T_E = (1.80667 - 1) \cdot 298.15 = 240.508 \text{ K} \quad (31)$$

So if we had a 50 Ω resistor at -32.642°C it would have the same noise power as our amplifier within the bandwidth under discussion.

Review

- Introduced the idea of Signal to Noise Ratio
- Discussed Noise Factor as a ratio of powers and a metric of amplifier noise performance.
- Noted some key points and restrictions of noise factor in matched and unmatched systems.
- Developed Noise Figure as noise factor expressed in dB.
- Derived the Noise factor of a two stage impedance matched electronic system.
- Drew some key conclusions 1) First stage gain should be high. First stage noise should be low. 2) Effect of second stage noise is reduced by the gain of the first stage.
- Provided a real example of the use of SNR, noise figure & Noise factor based on two MiniCircuits amplifiers.



EEE225: Analogue and Digital Electronics

Lecture XII

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This Lecture

1. Equivalent Noise Generators
   - The Noise Equivalent Circuit
   - Quantifying The Noise Generators
2. Noise in Operational Amplifiers
   - Opamp Noise Model
   - Opamp Noise Model in a Circuit
   - Conclusions from the Noise Model
3. A Simplified Opamp Noise Model
   - Example with the Simplified Opamp Noise Model
4. Review
5. Bear

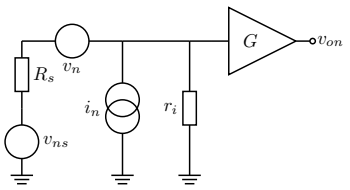
Equivalent Noise Generators

Representing noise using two or three noise sources is very attractive.

- It is a simple representation of the noise elements of large/complex circuits/systems.
- It is 'standard' – we can compare two systems performance by comparing their input noise generators.
- It provides a standard approach (we make the same analytical steps to compute the noise irrespective of the individual circuit details).
- The parameters the model needs to represent a real system are (quite) easy to measure in the lab.

The Noise Equivalent Circuit

- The added noise, N_A is represented by two generators a series voltage generator, v_n, and a parallel current generator i_n.
- Two generators are required to make the model independent of source impedance.
- These represent the voltage noise that would be in series with real resistances in the system and current noise that would be in parallel with forward biased pn junctions.



v_{ns} – noise of R_s
v_n – amplifier input noise voltage
i_n – amplifier input noise current
r_i – input resistance of the amplifier (noiseless)
G – is the gain of the amplifier.

- The equivalent noise generators can be found for a real system by selecting values of R_s and measuring the output noise.
- A true RMS voltmeter is needed with a known bandwidth Δf.
- To obtain v_n set $R_s = 0$. It can be shown using standard circuit analysis that if $R_s = 0$, i_n has no effect and $v_{on} = \sqrt{G^2 \overline{v_n^2} \Delta f}$.
- Having obtained v_n any value of $R_s > 0$ can be used to find i_n as everything else is already known. With finite R_s:

$$\overline{v_{on}^2} = G^2 \left[\overline{v_n^2} \left(\frac{r_i}{R_s + r_i} \right)^2 + \overline{v_{ns}^2} \left(\frac{r_i}{R_s + r_i} \right)^2 + \overline{i_n^2} \left(\frac{r_i R_s}{R_s + r_i} \right)^2 \right] \Delta f \quad (1)$$

$$\overline{v_{on}^2} = G^2 \left(\frac{r_i}{R_s + r_i} \right)^2 \left[\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_n^2} R_s^2 \right] \Delta f \quad (2)$$

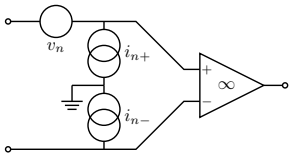
- Sometimes r_i is very large $10^{12}\ \Omega$ or so. In this case a finite R_s is necessary for i_n to flow through (and in so doing generate a noise voltage at the input w.r.t ground).
- This is often the case in FET input opamps. In a FET input opamp $\overline{i_n^2}$ is often very small say 0.01 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and $\overline{v_n^2}$ almost always dominates. Very small i_n^2 can often be neglected safely.
- If r_i is not very large say less than 10 MΩ, then R_s can be removed and (1) reduces to:

$$v_{on} = \sqrt{\left(G^2 \overline{i_n^2} r_i^2 \Delta f \right)} \quad (3)$$

assuming v_n has already been dealt with.

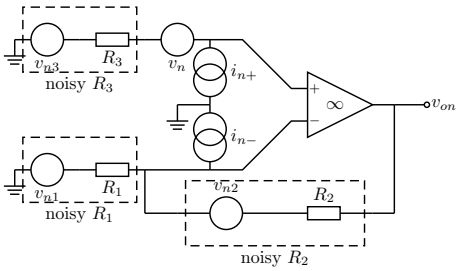
Noise in Operational Amplifiers

- Opamps can be quite complicated circuits. It's not practical to work out the noise of each resistor and transistor, and then combine them appropriately.
- SPICE does this, but having the numerical result doesn't tell the designer (you) what the dominant noise source is.
- Opamp noise is modelled in a similar way to the general unmatched amplifier.



The amplifier is ideal. v_n, i_{n+} and i_{n-} represent its noise. Other components are added around this model as if everything shown here is contained within the opamp.

A non-inverting *or* inverting amplifier with resistive feedback can be represented by



where the opamp and all resistors are replaced by their noise equivalent circuits.

- For an inverting amplifier the signal source is in series with R_1
- For a non-inverting amplifier the signal is in series with R_3

This leads to:

$$\overline{v_{on}^2} = G^2 \left[\overline{i_{n+}^2} R_3^2 + \overline{i_{n-}^2} \left(\frac{R_1 R_2}{R_1 + R_2} \right)^2 + \overline{v_n^2} + \overline{v_{nf}^2} + \overline{v_{n3}^2} \right] \quad (4)$$

- G – closed loop gain $(R_1 + R_2)/R_1$.
- $\overline{v_{n3}^2}$ – noise due to R_3, $4\,k\,T\,R_3$ V^2/Hz.
- $\overline{v_{nf}^2}$ – noise due to the feedback resistors R_1 and R_2, $4\,k\,T\,R_1\,R_2/(R_1 + R_2)$ V^2/Hz.
- $\overline{v_n^2}$ – opamp noise voltage generator
- $\overline{i_{n+}^2}$ – opamp noise current generator at the non-inverting input
- $\overline{i_{n-}^2}$ – opamp noise current generator at the inverting input

It would be good if you could derive this... try superposition. G is sometimes called the "noise gain" because it affects all the terms in the square braces irrespective of inverting or non-inverting feedback configuration.

Conclusions from the Noise Model

Eq. 4 can tell us if we can improve our circuit noise given a certain opamp and closed loop gain requirement.

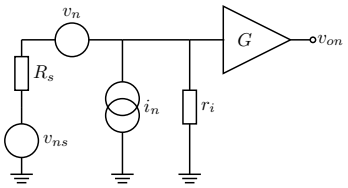
1. $i_{n+}^2\,R_3^2$ is due to the voltage across R_3 due to i_{n+}. If $R_3 = 0$ this noise goes away, but R_3 may be the source resistance or it may be there to reduce DC offset in the amplifier. If R_3 can not be reduced look for an opamp with low i_{n+}.
2. $\overline{i_{n-}^2} \left(\frac{R_1 R_2}{R_1 + R_2} \right)$ is the voltage appearing across the parallel combination of R_1 and R_2. R_1 and R_2 set the closed loop gain. Lowering both values – and keeping the ratio – is only possible to some extent. The opamp can not supply very large current and DC offset will be affected.
3. $\overline{v_n^2}$ is the opamp's noise voltage. It is irreducible – choose a different opamp.

4. $\overline{v_{nf}^2} = \frac{4\,k\,T\,R_1\,R_2}{R_1 + R_2}$ – this represents the thermal noise of the feedback resistors. R_1 and R_2 are in parallel from the point of view of v_{n1} and v_{n2}. Reducing R_1 and R_2 – but keeping the ratio – is possible but has same problems as for point 2. If the gain is high $R_1 // R_2 \approx R_1$...
5. $\overline{v_{n3}^2}$ – this is the noise due to R_3. The same constraints apply as in point 1.

- A standard opamp may have $v_n = 20\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$.
- At room temperature this is the same as the noise from about 24 $k\Omega$.
- If $R_1 // R_2$ and R_3 can be reduced below 24 kΩ points 4 and 5 (above) diminish
- FET input opamps have small current noise 0.01 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ c.f. 0.4 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for a BJT. Choose a FET opamp to reduce points 1 and 2 (above).

A Simplified Opamp Noise Model

Assume that an opamp circuit has been designed so that: it's non-inverting. The thermal noise associated with R_1 and R_2 is no longer significant (points 2 and 4 above). r_i is the input resistance – noiseless because it's accounted for by v_n and i_n



$$\overline{v_{on}^2} = G^2 \left(\overline{v_n^2} \frac{r_i^2}{(r_i + R_s)^2} + \overline{v_{ns}^2} \frac{r_i^2}{(r_i + R_s)^2} + \overline{i_{ns}^2} \frac{r_i^2\,R_s^2}{(r_i + R_s)^2} \right) \quad (5)$$

Example Simple Opamp Model Question

A particular amplifier has an input resistance of 100 kΩ, a voltage gain of 100 V/V and equivalent input noise voltage generator of 6 nV$\sqrt{\text{Hz}}$ and 0.0075 pA$\sqrt{\text{Hz}}$ respectively. The amplifier is fed by a noisy source resistance of 1 kΩ. What is the noise at the output?

$$v_{on}^2 = G^2 \frac{r_i^2}{(r_i + R_s)^2} \left(\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_{ns}^2} R_s^2 \right) \tag{6}$$

$$v_{on}^2 = 100^2 \frac{(100 \times 10^3)^2}{((100 \times 10^3) + (1 \times 10^3))^2} \left((6 \times 10^{-9})^2 + 4\,k\,T\,R_s + (0.0075 \times 10^{-12})^2 \cdot (1 \times 10^3)^2 \right) \tag{7}$$

Review

- Introduced the idea of equivalent noise generators
- Proposed a noise equivalent circuit consisting of two generators, making it independent of source impedance.
- Proposed a method to find the value of the noise generators for a real amplifier.
- Introduced a noise equivalent circuit for an opamp and added the noise sources of likely resistors.
- Developed an expression for the noise output in terms of the individual sources, and used this to investigate methods of minimising the noise output.
- Found a method to reconcile the simple noise equivalent circuit with the "full" opamp noise model provided some constraints are met.
- Did a quick example of a possible question using the simple model.

Thus ends this [course] on the minority field in the world of semiconductors. A field past glamour, often neglected, but undeniably essential. And a field of great satisfaction for those who know it.[1]

– Hans Camenzind (Designer 555 Timer)

[1] www.designinganalogchips.com



(Some) Past Exam Papers

Written Solutions on-line

Data Provided: None

The University Of Sheffield.

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Spring Semester 2014-15 (3.0 hours)

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Boltzmann's constant:	$k = 1.381\times10^{-23}$ JK^{-1}
Melting point of ice:	0^{o}C = 273.2 K
Permittivity of free space:	$\varepsilon_0 = 8.854\times10^{-12}$ Fm^{-1}
Permeability of free space:	$\mu_0 = 4\pi\times10^{-7}$ Hm^{-1}

PART A

1. Describe with the aid of a diagram the operation of a single-bit SRAM cell, based upon two inverters and two n-channel pass transistors. Explain how both *read* and *write* operations are achieved. **(8)**

2. **a.** Show how a transmission gate can be formed from a pmos and nmos transistor.

b. What is the reason for using complementary transistors in a transmission gate?

c. Show how a 2-to-1 multiplexer could be formed using transmission gates. **(8)**

3. **a.** With the aid of block diagrams, compare the structure of a TTL logic gate with that of a CMOS logic gate.

b. How would you increase the fan-in for each technology? **(8)**

4. **a.** For the pole-zero circuit of figure 4a, write down the low frequency gain and the high frequency gain, v_o/v_i, in terms of circuit components. **(2)**

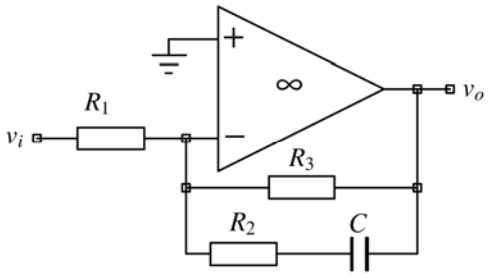


Figure 4a

b. The transfer function of the pole-zero circuit of figure 4a is

$$\frac{v_o}{v_i} = -k\frac{1+j\dfrac{\omega}{\omega_0}}{1+j\dfrac{\omega}{\omega_1}}$$

Where $k = \dfrac{R_3}{R_1}$, $\omega_0 = \dfrac{1}{CR_2}$ and $\omega_1 = \dfrac{1}{C(R_2+R_3)}$.

Sketch a bode plot of the transfer function assuming that ω_1 is much lower in frequency than ω_0. Label the plot with key frequencies, gains and phase shifts. **(6)**

5. A particular amplifier has an infinite input resistance, a voltage gain of 50 V/V and equivalent input noise voltage generator of 4 nV $Hz^{-1/2}$ and 0.01 pA $Hz^{-1/2}$ respectively. The amplifier is fed by a noisy source resistance of 0.6 kΩ. The noise voltage of a resistor R, is $V_n = \sqrt{4\,k\,T\,R}\cdot\Delta f$ nV_{RMS} where the symbols have their usual meanings.

a. Draw a noise equivalent circuit of the amplifier and source. **(4)**

b. With an input signal amplitude of zero, the amplifier output voltage is measured using a true RMS voltmeter with a noise bandwidth of 20 kHz. What RMS noise voltage would you expect the meter to indicate? **(4)**

6. A particular operational amplifier used with negative feedback applied is observed to have a closed loop gain of 1 and behave like a first order system in terms of its frequency response and output when driven by a step input.

a. State the equations in the time and frequency domain that the amplifier obeys. **(2)**

b. Describe the unity gain compensation scheme that the operational amplifier designer has used in order to achieve this response. *(Hint: To obtain full marks your description must include a sketch of the open loop bode plot before and after compensation.)* **(6)**

7. Starting from the charge neutrality condition and assuming that the acceptor and donor doping densities in a semiconductor are known, derive expressions from which the equilibrium majority and minority carrier concentrations can be estimated for,

i) an n-type extrinsic doped semiconductor, and

ii) a compensated near-intrinsic doped structure.

(Hint: State any assumptions that you make. You must show the derivation for full marks) **(8)**

8. Show clearly the conduction band, valence band and Fermi-level positions of a semiconductor p-n junction laser under lasing conditions.

Draw a typical light output versus junction current characteristic for this device and identify the different regions.

Sketch the typical spectral output (as a function of wavelength) of such a device when it is biased well below the lasing threshold current. **(8)**

9 Draw the band diagram for an ideal metal- n-type semiconductor junction in equilibrium for the cases when:

i) the junction rectifies

ii) the junction is ohmic

Make clear the relative work functions for the metal and semiconductor in both cases, the position of the Fermi levels and the magnitude of any potential barrier.

State the direction of majority and minority current flow for the case of the rectifying junction when it is forward and reverse biased. **(8)**

PART B

10. a. A 4-bit Digital-to-Analog Converter is shown in **Figure 10.**

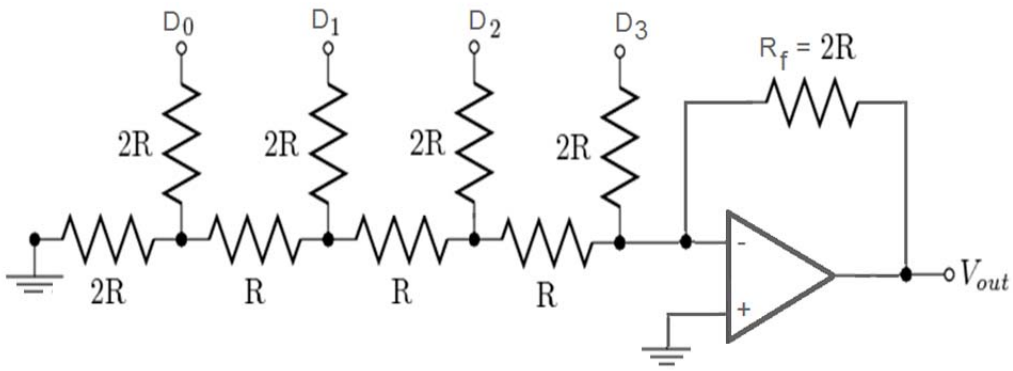


Figure 10. R-2R ladder DAC.

For input voltage levels of 3.3V, calculate the output voltage for the input $D_0D_1D_2D_3 = 1101$. **(8)**

b. The following Verilog code describes a certain logic gate at the switch-level.

```
module mygate(Y,A);
input A;
output Y;
supply1 POWER;
supply0 GROUND;
pmos t1 (Y, POWER, A);
nmos t2 (Y, GROUND, A);
endmodule
```

Draw a transistor-level circuit diagram for this logic gate. Produce a table indicating the state of each of the transistors for all possible combinations of the input **A**. Hence, deduce the logic function of the gate.

A 500Ω resistive load is connected between the output of the gate (Y) and GROUND. The supply (POWER) is set to 3.3V and the input (A) is set to 0V.

Calculate the current flowing through the resistive load and the voltage at the output (Y) of the gate.

You may assume that the *on* resistance (R_{DS}) of a pmos transistor is 75Ω and that of an nmos transistor is 25Ω. The *off* resistance for both transistors is 500,000 Ω. **(12)**

11. a.

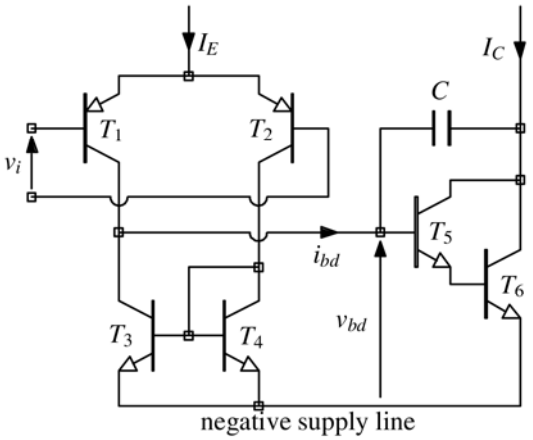


Figure 11a

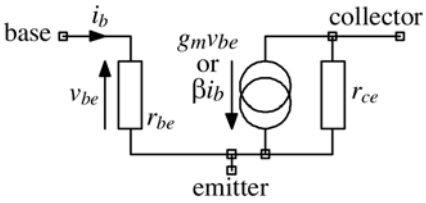


Figure 11b

Figure 11a shows the simplified circuit diagram of the input stages of a typical operational amplifier. All the transistors used have large signal and small signal current gains of 250.

i) State the main purposes of the transistor pairs (T_1 and T_2), (T_3 and T_4) and (T_5 and T_6). **(6)**

ii) Using the small signal equivalent circuit of figure 11b show that the input resistance of the T_5, T_6 combination, $r_i = v_{bd}/i_{bd}$, is

$$r_i = r_{be5} + (\beta_5 + 1) r_{be6}$$

(5)

You can assume here that r_{ce} is so large that its effects can be neglected.

You may find the relationships $g_m = \frac{eI}{kT}$, $r_{be} = \frac{\beta}{g_m}$, $h_{FE} = \frac{I_{Coll}}{I_{Base}}$ useful in this question. Assume that $kT/e = 0.026$ V.

b. **i)** A particular amplifier with a dc gain of 100 V/V is observed by experiment to behave like a first order system. Measurement shows that the magnitude of amplifier gain has dropped to 50 V/V at a frequency of 120 kHz. Calculate the -3dB frequnecy. **(4)**

ii) A different amplifier, also having a gain of 100 V/V, has a GBP = 100 kHz. Evaluate the |gain| and phase shift of this amplifier at a frequency of 75 kHz. **(2)**

iii) It was also observed that at 0.05 MHz the biggest sinusoidal signal that could be obtained at the amplifier output without evidence of slew rate limiting was 3 V_{RMS}. Calculate the amplifier slew rate. **(3)**

12. a. An n-type semiconductor with work function 3eV is sandwiched between two metal contacts, M1 with work function 4eV, and M2 with work function 1eV. The resistance of the bulk semiconductor between the contacts is 2Ω. When a DC voltage of +1.5V is applied across the two metal contacts, a large current of 500mA flows. When the polarity of the voltage is reversed, the current that flows is reduced significantly.

Identify the type of metal-semiconductor we have with M1 and M2.

Calculate the magnitude of the reduced current that flows when the voltage was reversed. **(10)**

b. The unsaturated drain characteristic of an induced channel enhancement mode metal-oxide-silicon-transistor (MOST)device can be represented by:

$I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right]V_{ds}$, where the symbols have their usual meaning.

How does I_d vary with V_{gs} when $V_{gs} - V_{ds} - V_T < 0$?

The source terminal of such a MOST is grounded and the drain terminal is connected directly to the gate terminal. If $\mu_e C_g / l^2 = 4 \times 10^{-4}$ A V^{-2} and $V_T = 2.0$V. Find I_d when V_{ds} =1V, 3V and 4V. **(10)**

JPRD/NJP/JEG/JSN

Data Provided: None

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Permittivity of free space:	$\varepsilon_0 = 8.854 \times 10^{-12}$ Fm^{-1}
Permeability of free space:	$\mu_0 = 4\pi \times 10^{-7}$ Hm^{-1}

PART A

1. **i)** Explain, with the aid of a diagram, the operation of a two-input open-drain NAND gate. **(4)**

ii) A multisource bus is required with four data inputs and enable. Show how this can be achieved using open-drain NAND gates. **(4)**

2. The following Verilog code describes a certain logic gate at the switch-level.

```
module mygate(Y, A, B, C);
input A, B, C;
output Y;
supply1 POWER;
supply0 GROUND;
wire W1, W2;
pmos t1 (W1, POWER, A);
pmos t2 (W2, W1, B);
pmos t3 (Y, W2, C);
nmos t4 (Y, GROUND, A);
nmos t5 (Y, GROUND, B);
nmos t6 (Y, GROUND, C);
endmodule
```

i) Draw a transistor-level circuit diagram for this logic gate. **(4)**

ii) Produce a truth table for all possible combinations of the inputs **A**, **B**, **C**. Hence, deduce the logic function of the gate. **(4)**

3. **i)** Explain the difference between static power consumption and dynamic power consumption in a CMOS device. In your explanation, clearly describe the three components of power dissipation in such a device. **(5)**

ii) What do you understand by the term ‘activity factor’ when related to power dissipation. **(3)**

4. The transfer function of the circuit of Figure 4a is given by:

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1} \cdot \frac{1 + j\omega C(R_1 + R_3)}{1 + j\omega C R_3}$$

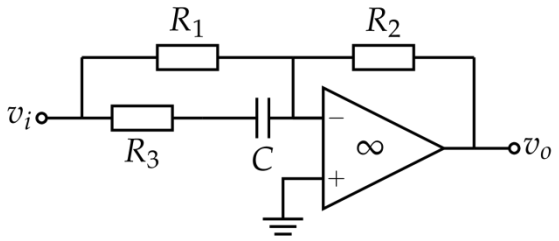


Figure 4a

a. Using the expression above, or otherwise, derive expressions for the low frequency and high frequency gain of the circuit. Briefly justify your results with arguments based on the physical behaviour of the components. **(3)**

b. The component values in the circuit are R_1 = 10 kΩ, R_2 = 20 kΩ, R_3 = 2.5 kΩ and C = l0 nF. Sketch the response of the circuit to a 0 V to 100 mV step input and label your sketch with initial and final amplitudes together with the time constant of the exponential change from one to the other. Your sketch should cover a time period of a few time constants. **(5)**

5. Describe concisely the cause of crossover distortion in class B push - pull output operational amplifiers. Use sketches to show the effects of crossover distortion on a triangular waveform, taking particular care with your representation of the crossover region. Show by sketching a circuit diagram how appropriate circuit design can largely overcome the crossover problem. **(8)**

6.

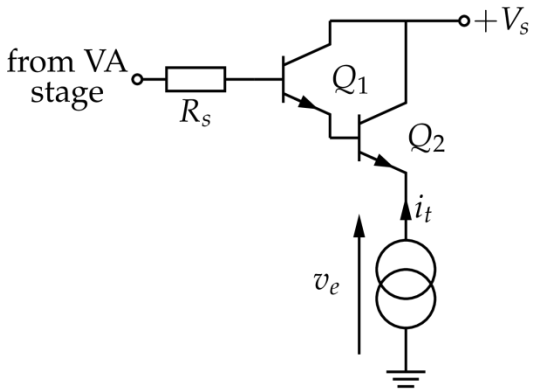


Figure 6a

The Darlington pair in Figure 6a is part of a Class B output stage of an operational amplifier. Show that the output resistance, r_o, is,

$$r_o = \frac{v_e}{i_t} = \frac{1}{g_{m2}} + \frac{\frac{1}{g_{m1}} + \frac{R_s}{\beta_1}}{\beta_2}$$

assuming $\beta_1 >> 1$ and $\beta_2 >> 1$.

g_{m1} and β_1 are small signal parameters of Q_1, g_{m2} and β_2 are small signal parameters of Q_2, v_e is the voltage on the emitter of Q2 with respect to ground and i_t is a 'test' current. *(Hint: it may be useful to draw and solve a small signal model composed of Q_2 and the resistance looking out of Q_2's base.)* **(8)**

7. Sketch a cross-sectional diagram of an induced channel enhancement mode metal-oxide-silicon-transistor (MOST). Describe briefly how a conducting channel is formed and how it can work to amplify a signal.

Identify all the significant parts of the device in the diagram paying particular attention to the position of the gate with respect to the conducting channel. **(8)**

8. Assuming that the change in drain current with drain voltage in a MOST is given by:-

$$\frac{dI_d}{dV_d} = \frac{\mu_e C_g}{l^2}\left[V_g - V_T - V_d\right]$$

where the symbols have their usual meaning, derive expressions for:

i) the drain current in the unsaturated region,

ii) the value of drain voltage when saturation of the drain current occurs, and the value of the saturation current, and

iii) the transconductance in the saturated region. **(8)**

9. A p-n junction made of silicon (E_g = 1.1 eV), is used as a solar cell to generate power. Draw the conduction band, valence band and the Fermi-level of this p-n junction when it is open circuit with;

i) light of wavelength 1550 nm falling on its surface, and with

ii) visible wavelength light falling on its surface.

Give a brief justification for the way you have drawn these.

What is the voltage you can expect across this p-n junction in both these cases? **(8)**

PART B

10. a. Explain with the aid of a diagram the operation of a 4-bit successive-approximation Analogue-To-Digital Converter (ADC). **(6)**

A particular successive-approximation ADC uses reference values of 16 V for bit 2^3, 8 V for bit 2^2, 4 V for bit 2^1 and 2 V for bit 2^0. Determine the sequence of binary states in the register for the conversion of a constant input of 11.7 V. Explain each step. **(4)**

b. A Digital-to-Analog Converter (DAC) is required to interface a Field Programmable Gate Array to a VGA display. The circuit shown in Figure 10 is to be used for each channel.

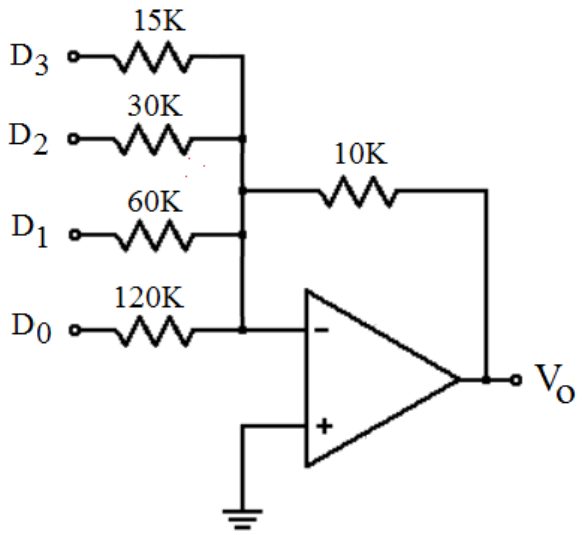


Figure 10. Weighted Binary DAC.

i) Briefly explain the operation of the circuit. **(3)**

ii) For input voltage levels of 3.0 V for logic '1', 0.0 V for logic '0' and the resistance values shown, calculate the output voltage for the input $D_3D_2D_1D_0 = 1101$. **(3)**

iii) In practice, the DAC structure shown in Figure 10 would not be used in higher resolution applications e.g. for an 8-bit converter. Explain the reason for this. **(4)**

11. a. Figure 11a shows a network consisting of noisy resistors, a noise voltage generator and a noise current generator.

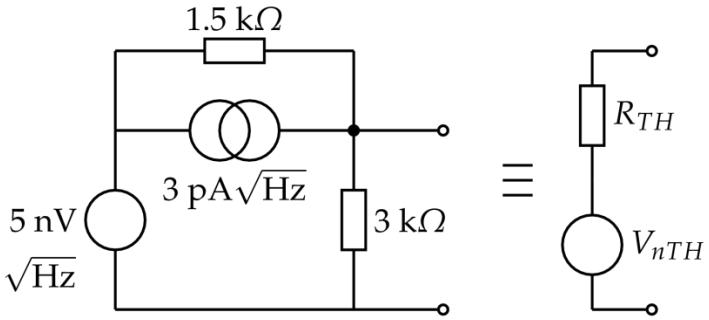


Figure 11a

Find the noise free resistance R_{Th} and the rms noise voltage V_{nTh} which form the Thevenin equivalent of the noisy network. **(10)**

b. The amplifier of Figure 11b has an equivalent input noise voltage, v_n of 15 nV $Hz^{-1/2}$, a negligible input current noise generator, and noisy resistors R_1, R_2 and R_s. The noise at the inverting input due to R_1 and R_2 is:

$$\overline{v_{nf}^2} = 4kT\frac{R_1R_2}{R_1+R_2}\ \mathrm{V^2Hz^{-1}}$$

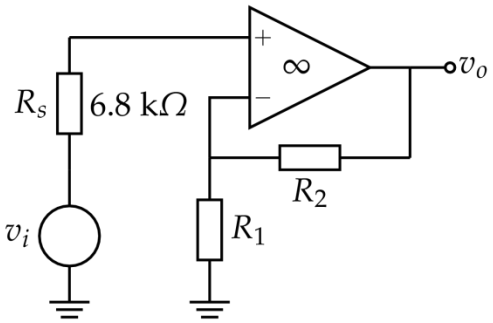


Figure 11b

i) If the noise power at the output of the amplifier due to R_1 and R_2 must not exceed 10% of that due to v_n, what are the maximum values of R_1 and R_2 that can be used to achieve an amplifier gain of 20? **(6)**

ii) A true rms voltmeter with a bandwidth of 10 kHz is connected to the amplifier output. What reading would you expect it to display with no input signal and R_1 and R_2 as calculated in part **(b) (ii)**? **(4)**

The mean square thermal noise voltage generated by a resistor R is $4kTR$ V^2 Hz^{-1} where $k = 1.38 \times 10^{-23}$ J K^{-1} and T may be taken as 300 K.

12. a. The Fermi-Dirac function is given by:-

$$P(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}$$

where the symbols have their usual meaning.

Using this, show that the built-in voltage (V_0) of a p-n junction is given by:-

$$V_0 = \frac{kT}{e} \ln\left(\frac{n_n}{n_p}\right)$$

where n_n and n_p are the electron concentrations in the n-type and p-type semiconductor respectively. **(8)**

i) Starting with a p-type silicon semiconductor (E_g = 1.1eV) doped to 2×10^{16} cm^{-3}, you create a p-n junction by diffusing in n-type dopants to a level of 1×10^{17} cm^{-3}. Given that n_i at 300K is 1×10^{10} cm^{-3}, what is the built in voltage of this junction at room temperature? **(4)**

ii) Describe qualitatively what happens to this built in voltage as the junction temperature increases to 450K and explain why. **(2)**

iii) Light from a 633 nm He-Ne laser with a 1 mW output falls on this silicon p-n junction when it is reverse biased. Assuming that it is 100% efficient in converting all of the light into current, what is the maximum current that would flow in this junction under this illumination? **(6)**

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Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2016-17 (3.0 hours)

EEE225 Analogue and Digital Electronics

In **Part A**, answer **FIVE** questions. **No marks will be awarded for solutions to a sixth question. In Part B,** answer **all questions**. Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Physical constants:

Charge on electron:	-1.602×10^{-19} C
Free electron rest mass:	$m_0 = 9.110 \times 10^{-31}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{8}$ m s^{-1}
Planck's constant:	$h = 6.626 \times 10^{-34}$ Js
Boltzmann's constant:	$k = 1.381 \times 10^{-23}$ JK^{-1}
Melting point of ice:	0 °C = 273.2 K
Permittivity of free space:	$\varepsilon_0 = 8.854 \times 10^{-12}$ Fm^{-1}
Permeability of free space:	$\mu_0 = 4\pi \times 10^{-7}$ Hm^{-1}

PART A

1. With reference to digital logic gates, explain what is meant by the terms *Noise Margin* and *Fan-Out*. **(4)**

2. Figure 2 shows a diode logic circuit. Produce a truth table for all combinations of the input variables A and B.

The input voltage level is 5V and the diode forward voltage drop is 0.7V. What is the logic function of this circuit? What is the HIGH output voltage level?

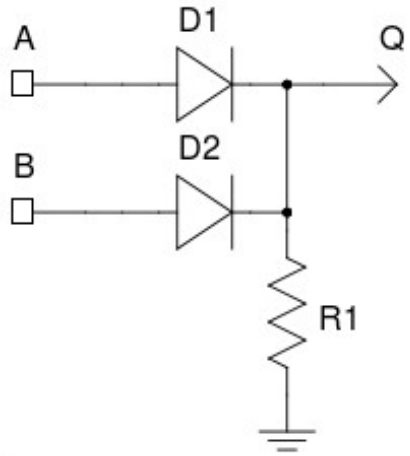


Figure 2. Diode Logic **(4)**

3. With the aid of a diagram, briefly explain the operation of a 4-bit successive-approximation Analogue-To-Digital Converter (ADC). **(4)**

4. Show that the output resistance of the one transistor current source in Figure 3 is given by

$$r_o = r_{ce}[1 + g_m(r_{be} /\!/ R_E)] \quad ,$$

where the symbols have their usual meaning and // signifies a parallel combination.

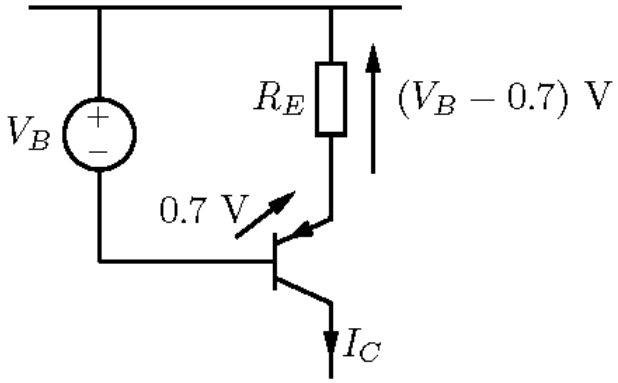


Figure 3. One transistor current source. **(4)**

5. A wideband amplifier in a matched 50 Ω system is made from two thin film amplifier modules with gains of 25 dB and 15 dB and noise figures of 4.50 dB and 7.00 dB, respectively, such that the overall amplifier bandwidth, Δf, is 1000 MHz.

a. What is the gain of the series combination? **(1)**

b. What is the noise factor of each amplifier module? **(1)**

c. What is the noise figure of the combination if the higher gain module is at the input end of the amplifier? **(2)**

6. An operational amplifier is configured as a non-inverting voltage amplifier with a dc gain of approximately 500 V/V using two resistors R_1 = 250 kΩ and R_2 = 500 Ω. The measured gain at low frequencies is 496 V/V. The -3dB frequency is observed by experiment to be 20 kHz. The roll-off above 20 kHz is 20 dB/decade, and the phase shift at 20 kHz is -45°.

You have determined, by circuit analysis, that the closed loop voltage gain expression is,

$$\frac{V_o}{V_i} = \frac{1}{\frac{1}{Av} + \frac{R_2}{R_1 + R_2}},$$

where the symbols have their usual meaning.

Determine the dc open loop gain, A_0, of this amplifier. **(4)**

7. Give 4 advantages that silica based optical fibres have over copper cables for transmitting data. **(4)**

8. With the aid of energy versus momentum (E-p) diagrams of a direct and indirect band-gap semiconductor, explain why one is preferred for making light emitting diodes. Mark the axes clearly and identify the band-gap energy. **(4)**

PART B

9. a. When considering signal conditioning at the input stage of a sampled system:

What do you understand by the term aliasing? **(3)**

An analogue signal is to be digitised. Describe any necessary circuitry which is required before the Analog-to-Digital Converter (ADC). **(5)**

b. Figure 9 shows a 6-bit digital to analog converter with resistance values in Ohms.

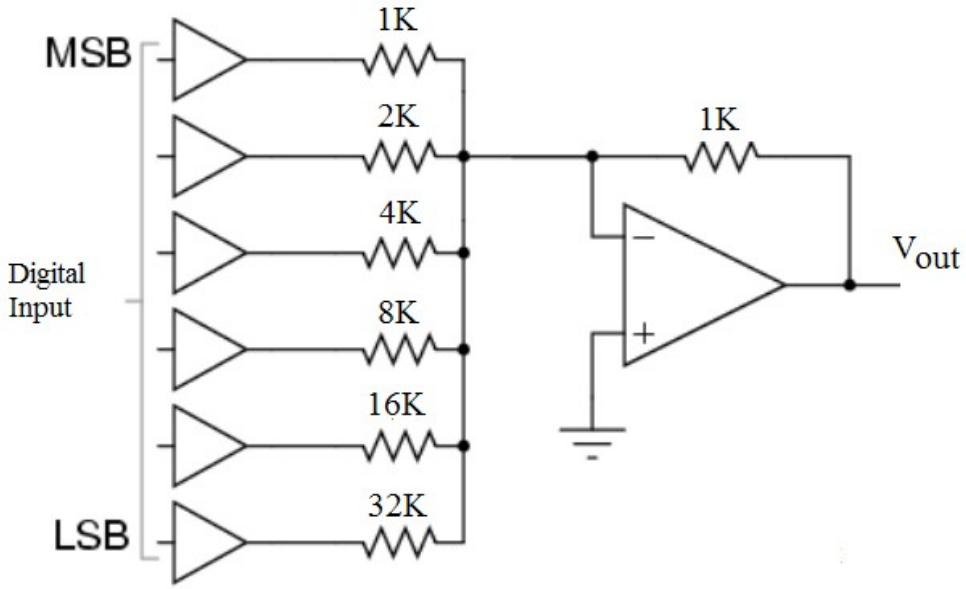


Figure 9. Digital-to-Analog Converter

i) Briefly explain the operation of the circuit. **(4)**

ii) Calculate the output voltage for a binary value of 110001 assuming a voltage of 5V for a high input logic level. **(4)**

iii) In practice, the DAC shown in Figure 9 would not be used in higher resolution applications e.g. for a 16-bit converter. Explain the reason for this. **(4)**

10. a.

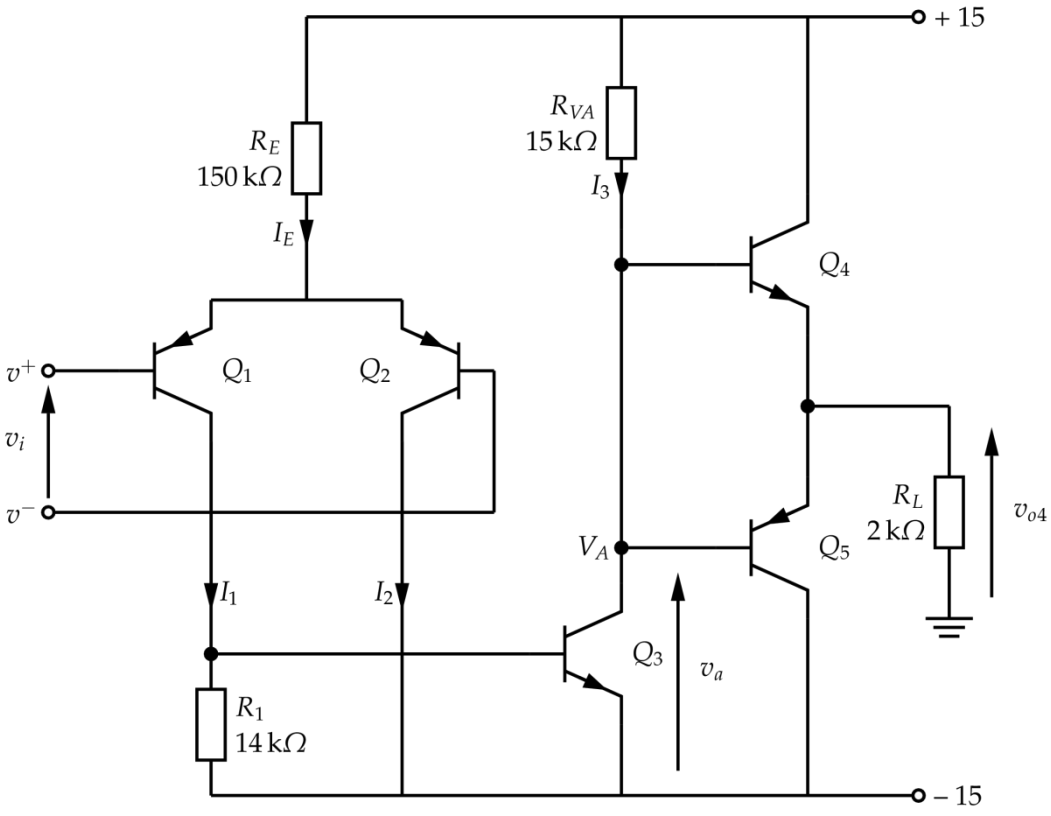


Figure 10

a. Figure 10 shows the simplified circuit diagram of a typical operational amplifier. All the transistors used have large signal and small signal current gains of 100.

i) Describe (with a diagram and some equations), how the circuit of Q1 and Q2 could be improved by a current mirror. Include the effect of the mirror on I_1 and I_2 by considering a small change in current and compare this with the resistively loaded case shown in Figure 10. **(9)**

ii) List some advantages of using a mirror in place of R_1. **(4)**

b. **i)** The circuit in Figure 10 may be improved by adding another transistor before Q3 to form a Darlington pair. Draw the circuit diagram of a Darlington pair and label the new transistor Q6. **(1)**

ii) Using a small signal equivalent circuit show that the input resistance of the your Darlington pair combination is approximately,

$$r_i \approx r_{be6} + \beta_6 r_{be3}$$

Where the symbols have their usual meanings. **(6)**

You can assume throughout this question that r_{ce} is so large that its effects can be neglected. The relation $\beta = g_m r_{be}$ may be useful.

11. You apply a bias to a semiconductor p-n junction such that it works as a photodiode.

i) Draw the p-n junction under this bias condition. Mark clearly on the diagram the band-gap, the conduction and valence bands, the Fermi-levels, and the voltage that is being applied. **(6)**

ii) What is the minimum level of doping needed to achieve this p-n junction? **(6)**

iii) Will you dope it with acceptors or donors? **(1)**

You decide to use a level of doping that ensures that the conductivity of the p-type top layer you created is ten times that of the original n-type semiconductor.

iv) Estimate the electron concentration in this top layer. **(5)**

v) What is the longest wavelength of light this photodiode can detect and why is there this limit? **(2)**

The resistivity of intrinsic silicon at room temperature is 5×10^{3} Ω-m, and $\mu_e = 0.12\ m^2\ V^{-1}\ s^{-1}$, $\mu_h = 0.05\ m^2\ V^{-1}\ s^{-1}$ and $E_g = 1.1$ eV. (Note: all the symbols have their usual meaning.)

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