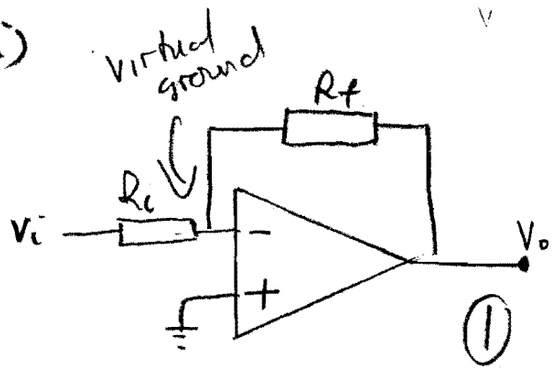
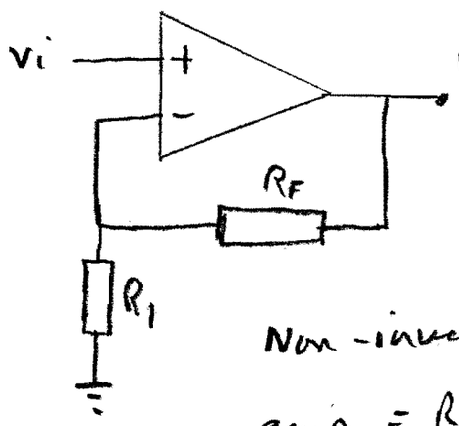
1(a)



(1)

Inverting gain $= -R_F/R_i$ (1)



(1)

Non-inverting gain $= \frac{R_f + R_1}{R_1}$ (1)

Virtual ground

$A_V \to \infty$ so $V_i^- \approx V_i^+$ V_i^+ is directly connected to ground so V_i^- becomes a virtual ground (close to the potential of V_i^+). Effectively this is grounded through the op-amps internal circuitry

1(b) $V_o = V_o|_{V_1} + V_o|_{V_2}$ by superposition. (1)

$= -\frac{R_2}{R_1} V_1 + \left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_1+R_2}{R_1}\right) V_2$ (1)

inverting gain

non-inverting gain

$V_o = -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2 = \frac{R_2}{R_1}(V_2 - V_1)$ (1)

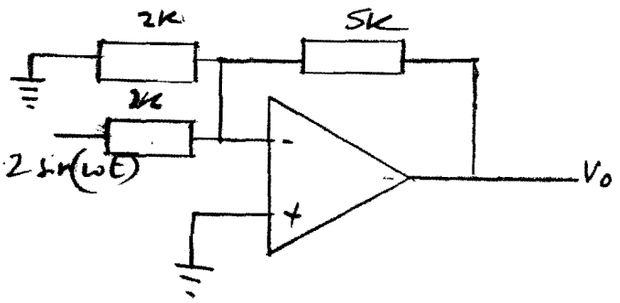
$\frac{R_2}{R_1} = 50$ $V_2 - V_1 = 22mV$ So $0.022 = 1.1V$ (1)

1c Can use superposition, including splitting the ac and dc components.

When using superposition we short out the other terminals to ground. (1)

AC components:

$V_o|_{V_2}$



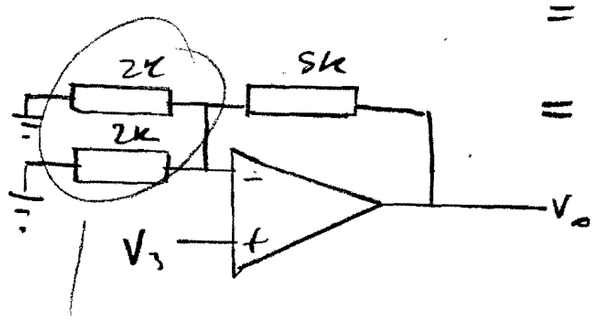
(1)

into inverting input so $V_o = -\frac{R_f}{R_1} V_2$

$= -\frac{5}{2} V_o$ (1)

$= -\frac{5}{2} \cdot 1.2 = -3 \sin(\omega t)$

$V_o|_{V_3}$



(1)

2 × 2k resistors in parallel $R_{11} = \frac{2 \times 2}{2+2} = 1k\Omega$

Into non inverting input. Like a 1kΩ to earth.

$V_o = = \frac{R_f + R_{11}}{R_{11}} V_3 = \frac{5+1}{5} V_3 = \frac{6}{5} \times 1.8 \sin(\omega t)$ (1)

$= 2.16 \sin(\omega t)$.

$V_o|_{\text{Total ac}} = (2.16 - 3) \sin(\omega t)$

$= -0.84 \sin(\omega t)$ (1)

DC component.

following same approach

$$V_o|_{V_1} = -3 \frac{5}{2} = -7.5V$$

$$V_o|_{V_3} = \frac{6}{5} \times 1.8V = 2.16$$

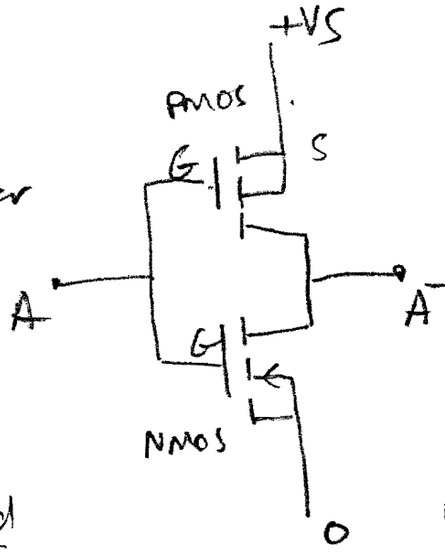
$$V_o|_{\substack{TOTAL \\ DC}} = 2.16 - 7.5V = -5.34V \cdot (1)$$

$$V_{o\,Total} = -5.34 - 0.84^{sin}(\omega t) \quad (1)$$

$-0.84\sin(\omega t)$ - phase is 180° out compared to input (1)

1d

CMOS inverter



MOS - field based device no switching current (cf BJT due to insulating gate - Only current is due to charging/discharging of gate capacitance (1)

OV applied

V_{gs} for the PMOS is $-V_S$ - device turns ON

V_{gs} for the NMOS is 0V - device is OFF

output → +VS (1)

using a pair of NMOS + PMOS transistors avoids the problem of non ideal (i.e 0Ω) ON state resistance, which would otherwise dissipate power (1)

Digital '1' applied (must be greater than V_T and $V_S - V_i$ must be less than V_T for the PMOS)

V_{gs} for the NMOS is $> V_T$ - device turns on

V_{gs} for the PMOS is $< V_T$ - device is off

0V is connected through the NMOS transistor to the output (1)

Output is 0V

Device is an inverter (1)

Digital '1' must be $\geq V_T$ i.e. $\geq 0.8V$

V_s must have $V_s - V_{in} < V_T$ V_s has a maximum of 0.6V (approx $2 \times V_T$). (1)

The University Of Sheffield.

Data Provided: None

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

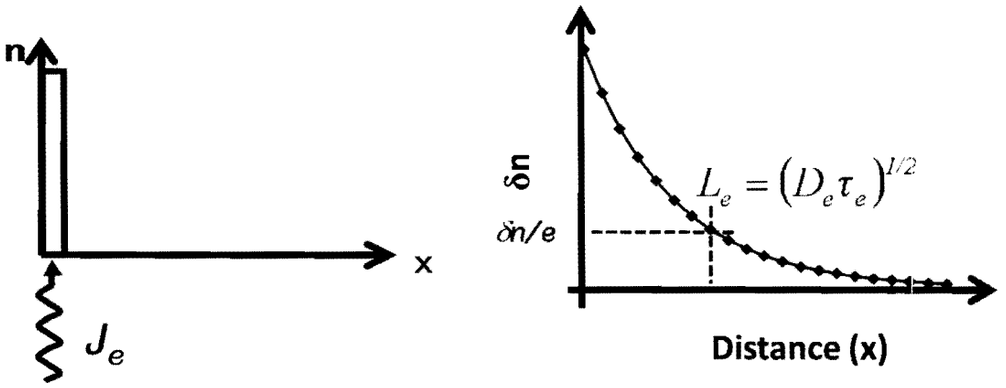
Spring Semester 2011-12 (3.0 hours)

EEE118 Electronic Devices & Circuits

SOLUTIONS

Question 2

(a) *When minority electrons are injected into one face of a cube of semiconductor the concentration varies exponentially with distance. Explain fully the mechanisms which result in this variation with distance. Note that there is no electric field applied to the cube.*



- Excess electrons produced at one side of a p-type block of semiconductor
- Carrier concentration gradient brings about carrier diffusion causing electrons to move from left to right
- As they move they recombine with the majority holes and reduce in number
- Get exponential variation with distance as shown

(b) *Write down the exponential expression describing this process (found at the beginning of this paper) and identify all the parameters. What material parameters might influence the distance that the minority electrons penetrate into the semiconductor?*

$$\partial n(x) = \partial n_0 \, exp\left(-\frac{x}{L_e}\right)$$

L_e is minority carrier diffusion length for electrons

x is the distance into the cube

δn_o is the steady state injected electron concentration at x = 0

Distance affected by value of L_e - increased mobility and increased recombination lifetime (less p-doping) both increase L_e (or temperature !) (or defects)

(c) *Instead of this injection into one face, the cube is uniformly radiated with light of energy greater than the crystal bond strength energy throughout its volume. Explain physically what happens during illumination and when the light is suddenly switched off. By analogy with the expression for distance variation, write down an equivalent equation for the time variation of the excess carriers in the material from the time the light is switched off, defining each parameter.*

- During illumination the generation rate of electron hole pairs exactly balances the recombination rate $\therefore \frac{dn}{dt} = G - R = 0$
- When to light is switched off $G = 0$ and

$$\therefore \frac{dn}{dt} = -R$$

and the excess electron density decreases exponentially with time

$$\partial n(t) = \partial n_0 \exp\left(-\frac{t}{\tau_e}\right)$$

τ_e is minority carrier diffusion length for electrons

t is the time period from switching the light off

δn_o is the steady state injected electron concentration at $t = 0$

(d) *In a light intensity measuring device based on the cube in section c, an electric field is applied across opposite faces of the cube. A light source with photon energy greater than the band-gap and intensity of 10^{17} photons per second illuminates the cube. What is the extra current produced in the device due to the light, assuming 100% conversion efficiency of the light into charge.*

The light creates electron hole pairs in the cube. When a field is applied the charges separate and contribute to a current which is proportional to the light intensity.

Since the process is 100% efficient each photon produces one electron-hole pair there are 10^{20} e-h pairs per second. 10^{17}

This represents 10^{17} electrons per second flowing in the external circuit due to the light.

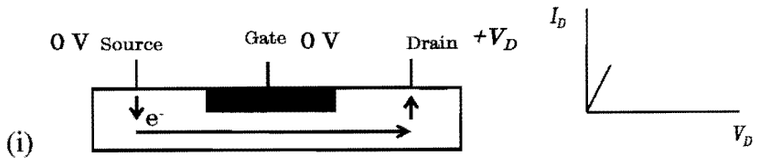
i.e. 10^{17} electrons/s = 10^{17} x 1.6 x 10^{-19} C/s = **16 mA** (assuming equal velocity).

each charge produces $\frac{qV}{W}$

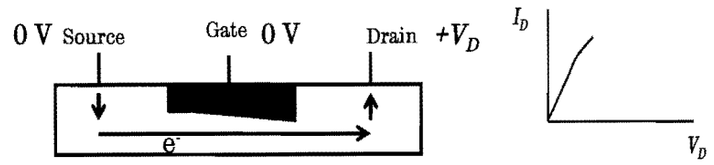
If e and h have the same velocity 16mA is correct.

Question 3

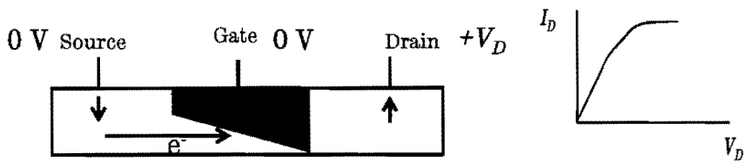
(a) *Briefly explain the operation of a planar junction field effect transistor (as used in integrated circuits) using sketches where appropriate but without derivation. Describe how it works as both an amplifier and as a switch.*



(i)



(ii)



(iii)

(i) Zero gate voltage – small voltage between source and drain gives electron drift and hence drain current – behaves as a resistor.

(ii) Zero gate voltage - as V_D and I_D increases further, the positive voltage at the drain increases the p^+n junction reverse bias at the drain end – increasing the depletion width there and so constricting the channel. As the resistance of the constricted channel is higher (reduced slope) – *I/V* plot is no longer linear.

(iii) At higher V_D the depletion region closes the channel completely (called **pinch-off**) – the current I_D cannot increase with increasing V_D and it saturates

Amplifier operation – change in gate (input) voltage results in a change in drain current which can generate an output voltage change across a suitable load which is greater than the change in gate voltage, hence get gain.

Switching operation – when the gate voltage (negative) exceeds the pinch-off voltage, the drain current is zero. When the gate voltage is zero, the channel is open and maximum current flows i.e. on when $V_g = 0$; off when $V_g = V_{pinch\text{-}off}$.

(b) *Using the expression for the depletion depth dependence on reverse bias of a "one-sided" (i.e. $p^+ >> n$) abrupt junction given on page 1 of this paper, calculate the pinch-off voltage for a Si device with a channel thickness of 1 μm and donor density of 1×10^{22} m^{-3}. Assume the built-in potential for the junction is 0.7 V. Would this design be suitable for a digital circuit with a supply voltage of 5V?*

From the equations given on the exam paper

with $\varepsilon = \varepsilon_o \varepsilon_r$

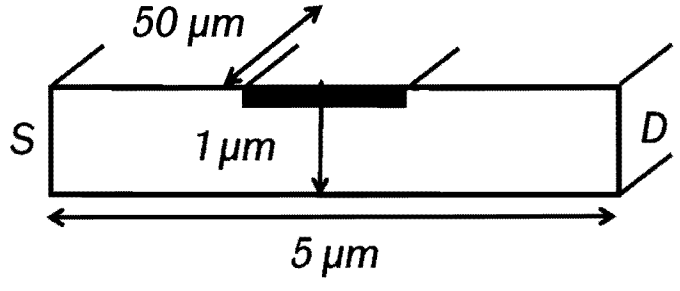
$$d_j = \left(2\varepsilon V_j / eN_d\right)^{0.5}$$

Re-arranging —

Putting in the values given V_p = **6.8 V**

Since the pinch-off voltage is greater than the supply voltage of 5 V, putting the FET into an "off" state would not be possible hence a 5 V supply is not suitable.

(c) *Calculate the channel resistance (resistance between the source and the drain) for this device for a source-drain spacing of 5 μm and gate width (long dimension) of 50 μm. Ignore the thickness of the p-gate region in your calculation.*



Resistivity —

Resistance between source and drain — = $(0.0143 \times 5 \times 10^{-6})/(50 \times 10^{-6} \times 1 \times 10^{-6})$

= 286Ω

(d) *Calculate the gate capacitance of this device with an applied gate voltage greater than the pinch-off value, assuming a gate length of 1 μm.*

The capacitance of the gate is given by $C = \frac{\varepsilon A}{d}$

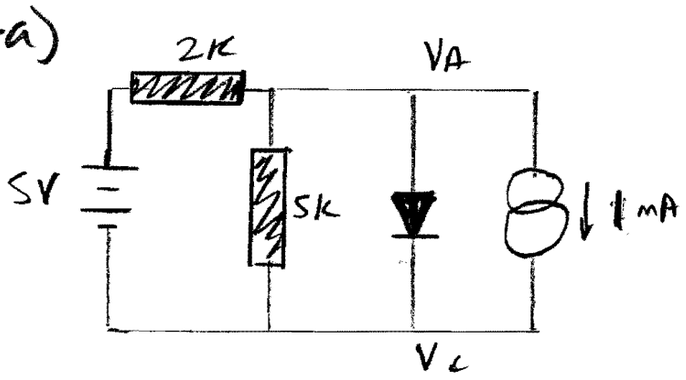
$A = 50\text{x}10^{-6}$ x $1\text{x}10^{-6}$ m^2

$d = 1\text{x}10^{-6}$ m

$\varepsilon = 8.85\text{x}10^{-12}$ x 12 Fm^{-1}

Putting in these values gives $C =$ **$5.3\text{x}10^{-15}$ F = 5.3 fF**

4a)



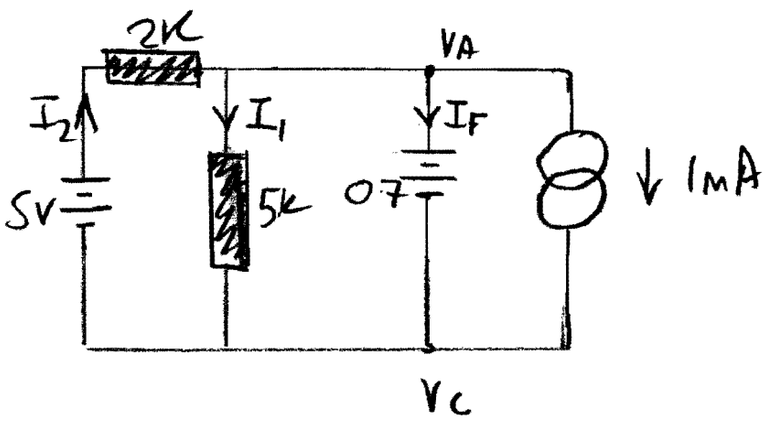
Assume diode is non conducting - replace with open circuit

$$V_A - V_C = 5V \times \frac{2}{2+7} - 1mA \times \frac{2+5}{2\times 5} = \frac{10}{9} - 2\times10^{-3} \times \frac{7}{10}$$

$$= 1.1111 - 0.0007 = 1.109\,V$$

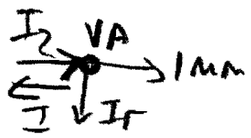
This is greater than the 0.7 V needed to turn on the diode, so diode is conducting

Conducting diode - replace with 0.7V voltage source across $V_A - V_C$ (3)



$$I_2 = \frac{5-0.7}{2k} = 2.15mA$$

$$I_1 = \frac{0.7}{5k} = 0.14mA$$



Sum current at V_A node

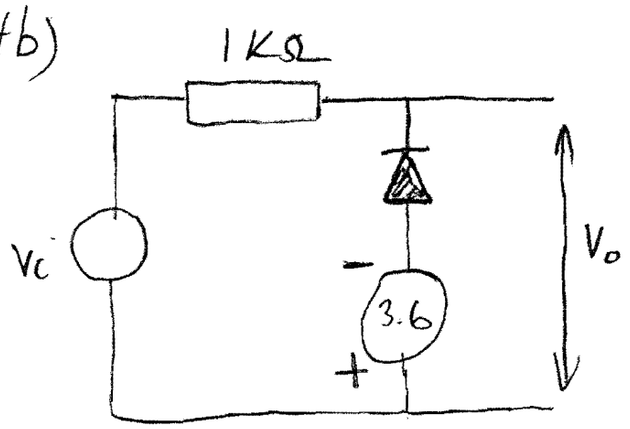
$$I_2 = I_1 + I_F + 1mA.$$

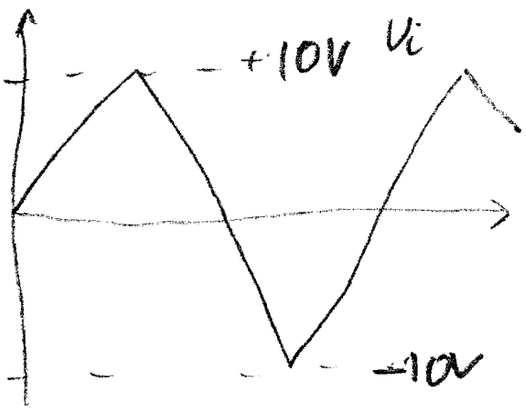
$$I_F = I_2 - I_1 - 1mA = 2.15 - 0.14 - 1$$

$$= 1.01mA$$

(3)

4b)

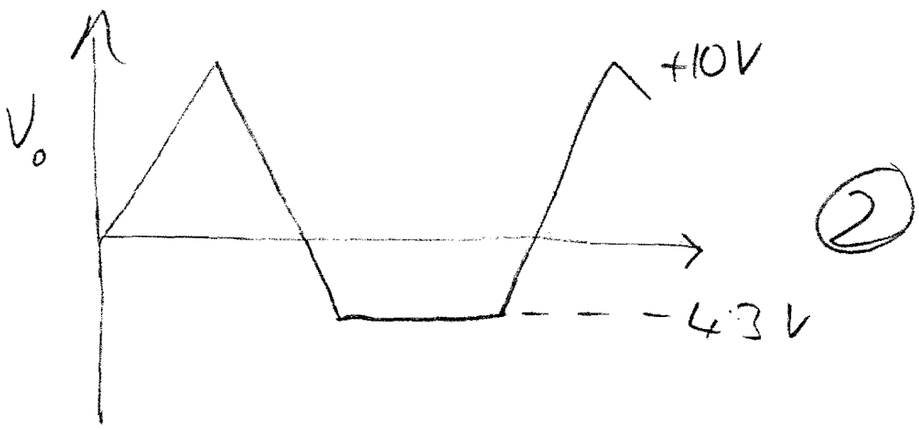




Diode will conduct when $V_i < 3.6 + 0.7$ $V_i < 4.3V$

At less than -4.3V the diode will conduct and the output will remain constant

At more than -4.3V the diode is non conducting and V_o just follows V_i (1)

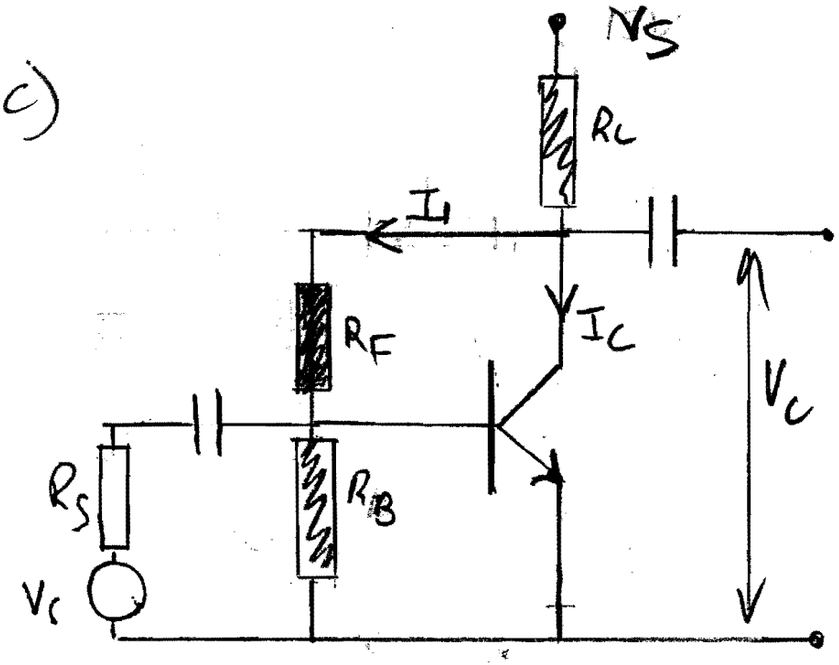


(2)

Maximum current is when the largest V is present across R. This occurs when $V_i = +10V$. But in this case an additional 4.3V is dropped across the resistor

$$\text{If max} = \frac{10 - (-4.3V)}{1k\Omega} = 14.3mA$$ (2)

4c)



$V_{BE} = 0.7$

$\beta = 400$

$R_F = 100k\Omega$.

$R_L = 5.8k\Omega$.

$R_B = 12k\Omega$.

$V_S = 12V$

$$V_S = I_1(R_F + R_B) + (I_1 + I_C) R_L \quad (1)$$

$$I_1 R_B = V_E + V_{BE} \qquad V_{BE} \cong 0.7 \quad V_E = 0V \quad (1)$$

$$I_1 R_B = 0.7V \qquad I_1 = \frac{0.7}{R_B} \quad (1)$$ substitute into (1)

$$V_S = \frac{0.7}{R_B}(R_F + R_B) + \left(\frac{0.7}{R_B} + I_C\right) R_L$$

$$V_S = 0.7\frac{R_F}{R_B} + 0.7 + 0.7\frac{R_L}{R_B} + I_C R_L \quad (1)$$

$$I_C = \frac{V_S - \frac{0.7}{R_B}(R_F + R_L + R_B)}{R_L}$$

$$\frac{12 - \frac{0.7}{12\times10^3}(100 + 5.8 + 12)\times10^3}{5.8\times10^3}$$

$$I_C = \frac{12 - 6.82}{5.8\times10^3} = 6.84\times10^{-4} = 884\mu A$$

$$I_1 = \frac{0.7}{R_B} = 58.3\mu A.$$

$V_C = 12 - (I_1 + I_C) R_L$

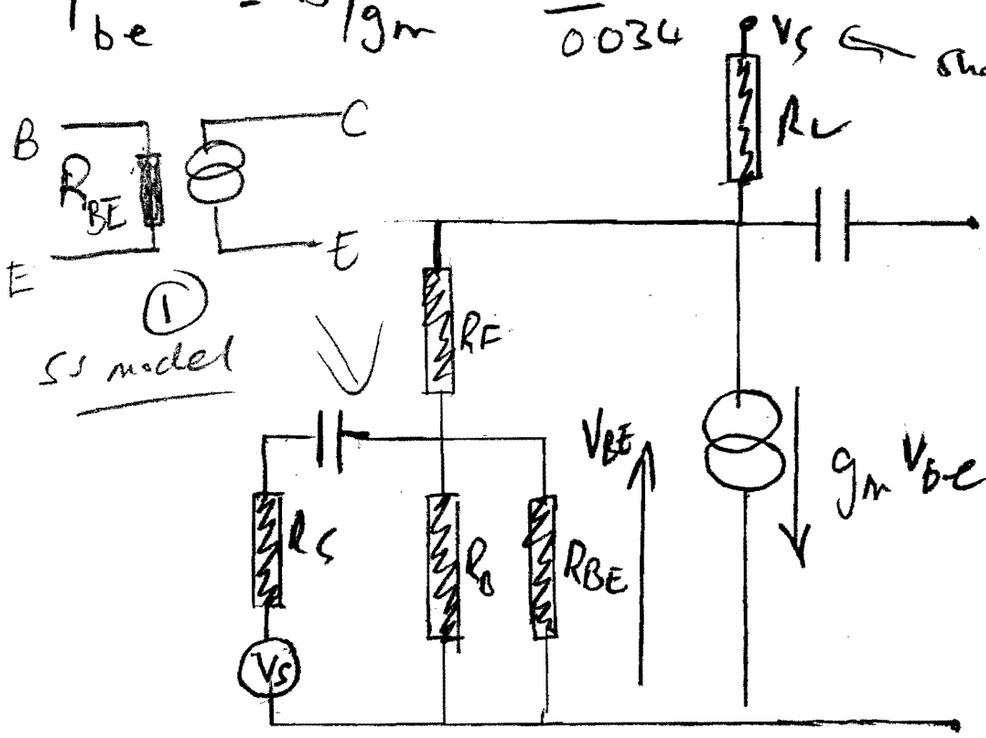
$= 12 - (684 + 587) \times 10^{-6} \times 5.8 \times 10^3$

$12 - 942 \times 5.8 \times 10^{-3}$

$12 - 5.46 = 6.54V$ (2)

$g_m = \frac{eI_C}{kT} = \frac{8.14 \times 10^{-4}}{0.026} = 0.034 A.V^{-1}$ (2)

$r_{be} = \beta / g_m = \frac{40}{0.034} = 1176 K\Omega.$ (2)

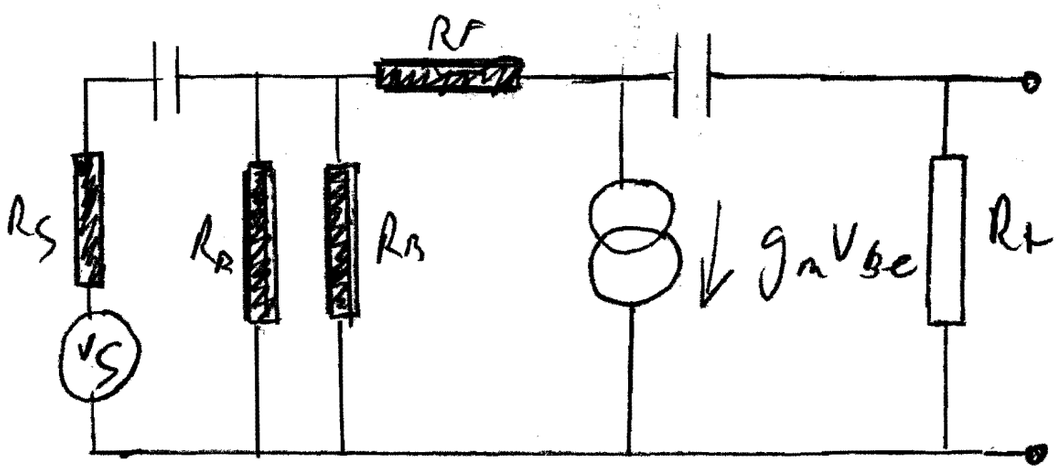


(1) SS model

$C_1 + C_2$ are to block DC bias and allow signals to pass

(2)

~



(1)

Question 5

(a) Using the equations for diode current density and saturation current density from page 1, derive the ratio of electron to hole current across the junction. In what three-terminal device is this ratio important and why?

From the given equations

$$J_0 = J_{e0} + J_{h0} = e\left[\frac{L_e n_p}{\tau_e} + \frac{L_h p_n}{\tau_h}\right] \qquad J = J_0\left[exp\left(\frac{eV}{k_B T}\right) - 1\right]$$

Since the square bracket term in the expression for J is the same for electron and hole flow across the junction, the ratio of electron and hole currents is given by

$$\frac{J_{e0}}{J_{h0}} = \frac{L_e n_p}{\tau_e} \cdot \frac{\tau_h}{L_h p_n} = \frac{L_e \tau_h}{L_h \tau_e} \cdot \frac{n_n}{p_p}$$

(Using $n_p p_p = n_n p_n = n_i^2$)

This means the ratio of currents depends heavily on the ration of doping.

This is important in the **bipolar transistor** where the **emitter is usually more heavily doped than the base to ensure minimal current from the base to the emitter** which appears as base current and reduces the gain of the transistor.

(b) *The current flowing in a certain Si p-n junction diode at room temperature is 10 μA when a reasonably large reverse bias voltage (not exceeding breakdown) is applied. Find the applied junction voltage corresponding to a forward current of 50 mA. The diode is constructed with p-type material of conductivity 2000 Sm^{-1} and n-type of 500 Sm^{-1}. Each region either side of the junction is 1 mm long and 0.5 mm^2 in cross-sectional area. Calculate the total voltage drop across the terminals of the diode when 50mA flows.*

Modifying current density equation for current

$$I = I_0\left[\exp\left(\frac{eV}{kT}\right)-1\right] = 5x10^{-2} = 10^{-5}\left[\exp\left(\frac{V}{0.025}\right)-1\right]$$

Re-arranging

$$\frac{5x10^{-2}}{10^{-5}} = \left[\exp\left(\frac{V}{0.025}\right)\right]$$

$$V = 0.025\ln\frac{5x10^{-2}}{10^{-5}} = 0.213\ \mathbf{V}$$

Resistance of n region = $L/\sigma A = 1x10^{-3}/(500 \times 0.5x10^{-6}) = 4\ \Omega$

Resistance of p region = $L/\sigma A = 1x10^{-3}/(2000 \times 0.5x10^{-6}) = 1\ \Omega$

Total resistance = 5 Ω

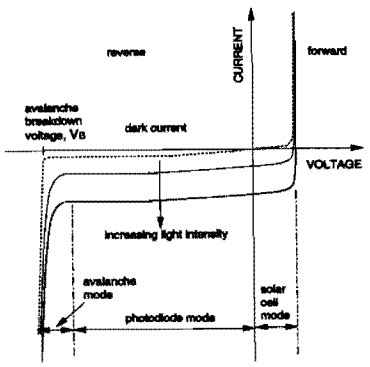
Voltage drop across this resistance = $5 \times 5x10^{-2} = 0.25$ V

Therefore total voltage drop across the diode terminals = 0.25 + 0.213 = **1.538 V** 0.463 V

(c) *Identify the term in the equation for J_0 that signifies the importance of the crystal bond strength for determining the reverse saturation current density.*

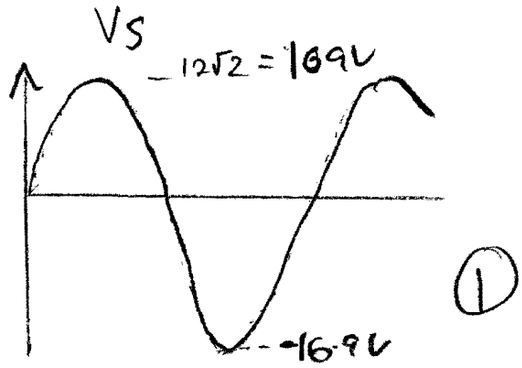
$n_p p_p = n_n p_n = n_i^2$ and n_i reflects the bandgap (bond strength) magnitude i.e. n_i smaller for larger bond strength (more difficult to create e-h pairs). Hence, for given doping, the minority carrier densities, n_p and p_n, are both small if n_i is small (small bond energy) and hence J_0 small for high bond strength or large bandgap.

(d) *Sketch two I/V characteristics covering forward and reverse bias for a diode with and without light shining on it, clearly labelling which is which. Assume that the light can produce electron hole pairs in the device.*

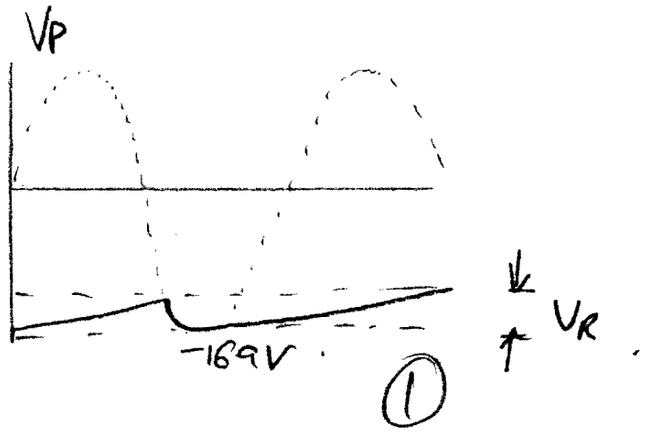


Two curves only required – light on and off – other details not needed.

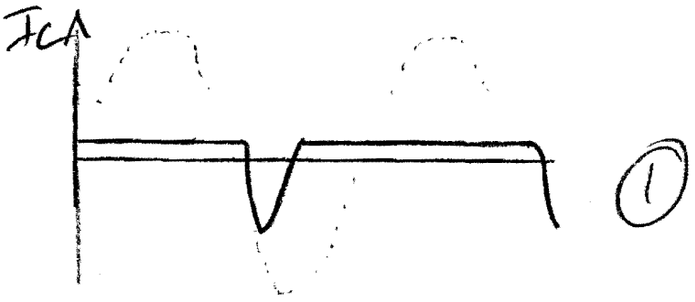
6a)



(1)

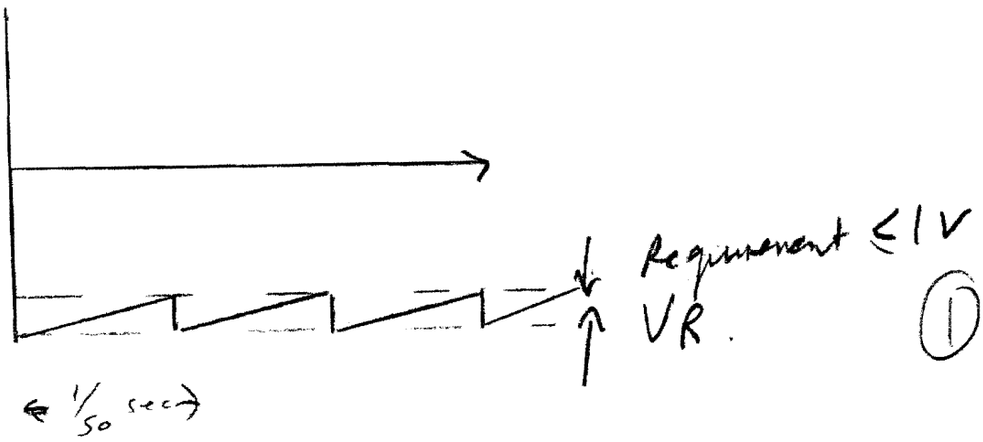


(1)



(1)

unattractive because Ic peaks once per cycle generating noise harmonics (1)



(1)

$$I = C\frac{dV}{dt} = C\frac{\Delta V}{\Delta t} = C\frac{V_R}{(1/50)}$$ (1)

if small Δ

$$I_{pk} = \frac{V_P}{R_L} \quad \therefore \quad \frac{V_P}{R_L} = C\frac{V_R}{(1/50)}$$

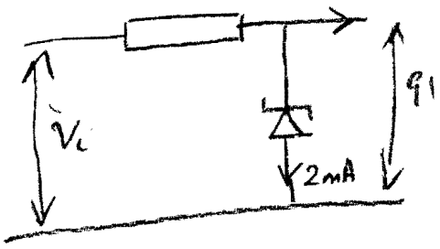
This is rather a large value - large and relatively expensive

$$C = \frac{V_P}{R_L V_R \times 50} = \frac{16.9V}{50 \times 1 \times 50} = 6.76 \times 10^{-3}$$

$$6.7mF$$ (2)

6b)

Need to find worse case scenario.



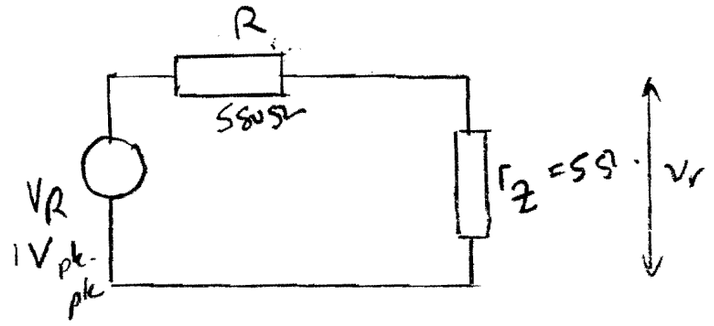
minimum $V_i = V_S\sqrt{2} - V_R$ (1)

maximum $I_L = 10mA$ (1)

$$R_{max} = \frac{V_S\sqrt{2} - V_R - 9}{10mA + 2mA} = 580\Omega \quad (1)$$

Assumption - 0.7V voltage drop is neglected. (1)

Ripple eq. circuit

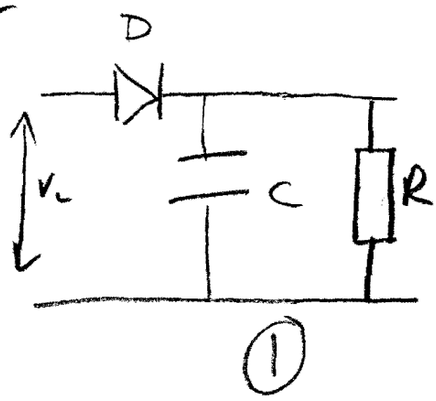


V_r is just voltage divided.

$$V_r = 1 \times \frac{5}{580 + 5} = \frac{5}{585} = 8.55mV \quad (2)$$

6c)

peak detector

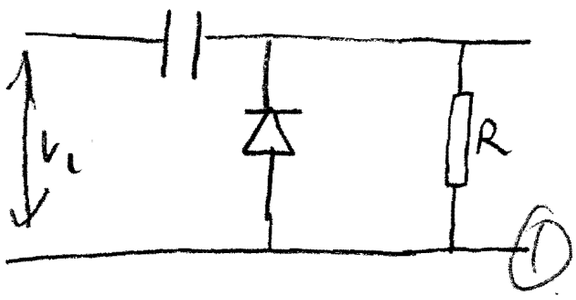


When V_i is positive Diode D is conducting C charges up to $V_i - 0.7V$ (1)

When V_i is negative D does not conduct C discharges to the load. (1)

If $RC >> \frac{1}{f}$ then the rate of discharge is negligable - peak is held (1)

clamp



(1)

On the first positive cycle the +ve V_i will drive current through V_i to V_o. The diode here is reverse biassed

On the first negative part of the cycle the diode becomes conducting and holds V_o at $-0.7V$. C charges up. Finally V_i begins to increase again, but D will not support current flow in this direction. There is only a small change in the voltage across C due to a small current through R (1)

6d) - Peak - output V is equal (or almost eq) to the peak of the input

- Clamp - clamps one extreme of the input to a defined value.

Voltage multiplier

