The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2011-12 (3.0 hours)

EEE118 Electronic Devices & Circuits

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

You may require the following:

Electronic charge, e =1.6x10^{-19}C

Permittivity of free space, ε_0 = 8.85x10^{-12} Fm^{-1}

Boltzmann's constant, k =1.38x10^{-23} JK^{-1}

Planck's constant, h=6.6x10^{-34} Js

Energy of a photon $=hc/\lambda$

Poisson's Equation $\frac{d^2V}{dx^2} = -\frac{ne}{\varepsilon}$

$$E = -\frac{dV}{dx}$$

$$d_j = \left(2\varepsilon_0\varepsilon_r V_j / eN_d\right)^{0.5}$$

$$J = eD\frac{dn}{dx}$$

$$J_0 = \frac{eL_e n_p}{\tau_e} + \frac{eL_h p_n}{\tau_h} \quad and \quad J = J_0\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

$n_p p_p = n_n p_n = n_i^2$

$$\beta = \frac{\alpha_B}{1-\alpha_B}$$

$$\partial p = \partial p_0 \exp\left(\frac{-x}{L_h}\right)$$

$$L = \sqrt{D\tau}$$

$$\alpha_B = \gamma_E \alpha$$

$$C = \frac{\varepsilon A}{d}$$

$$D = \frac{kT}{e}\mu$$

$$R = \rho L/A$$

Resistivity $\rho = \frac{1}{ne\mu}$

For silicon: relative permittivity ε_r =12 built-in voltage =0.7V

electron mobility=0.07m^2/Vs hole mobility=0.045m^2/Vs

band gap=1.12eV

1. **a.** Draw the circuits for the inverting and non-inverting Op-amp amplifier, which make use of an op-amp and two resistors. Indicate which circuit is which. Give an expression for the gain in both cases.

One of these amplifier circuits has a terminal which becomes a 'virtual ground'. Indicate this terminal on your drawing. Why does this terminal, which is not directly connected to ground, become a so called 'virtual ground'?

(5)

b. Derive an expression for the output v_o in terms of the inputs v_1 and v_2 for the Op amp. circuit in fig.1. Use this to calculate the output v_o when v_1= 100mV and v_2= 122mV. The resistor values used are R_1= 50kΩ and R_2=2kΩ.

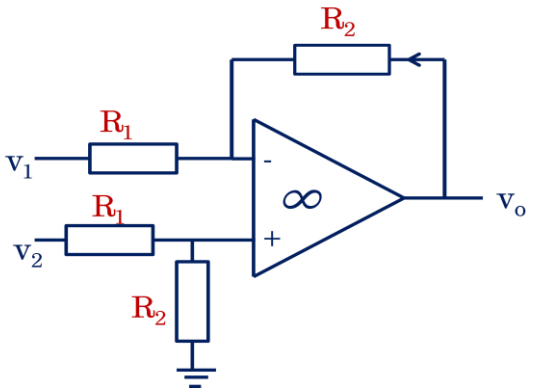


Fig.1 Op-amp circuit **(4)**

c. The op amp circuit of fig.2 has the following mixed signal + DC input voltages:

v_1= 3 V, v_2= 1.2sin(ωt) V
v_3= 2 + 1.8sin(ωt) V

where ω is the frequency and t is the time. Assume ω is the same for all inputs

Calculate the output voltage v_o, which has the form a+ bsin(ωt).. What is the phase of the output signal compared to the input signal?

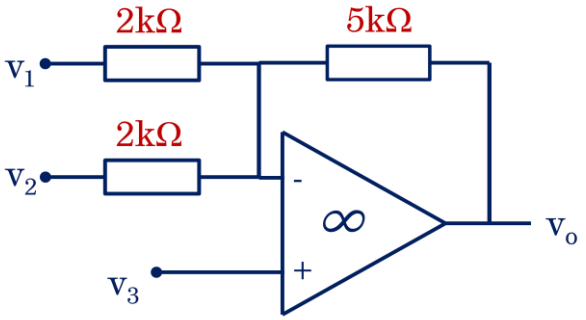


Fig 2: Op amp circuit

(9)

d. The circuit in fig.3 *(overleaf)* forms the basic building block of CMOS technology. What are the advantages of using (i) MOS transistors and (ii) a pair of NMOS and PMOS transistors over alternative approaches for digital processing?

If signal voltages appropriate for a digital '0' (=0V) and a digital '1' are applied to the input (v_i) what digital values appear on the output? Explain the operation of the circuit in both cases. If the threshold voltages for both devices are around 0.3V in modern CMOS, what is the minimum value of the voltage v_i required for digital '1' signal. What is the maximum value of the supply voltage V_s? **(7)**

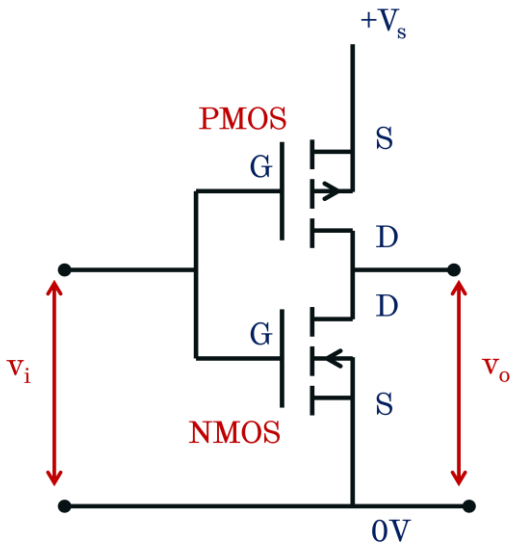


Fig.3. Basic CMOS circuit

2. **a.** When excess minority electrons are injected into one face of a cube of p-type semiconductor the concentration varies with distance. Sketch the variation of minority electrons with distance and explain fully the mechanisms which result in this dependence. Note that there is no electric field applied to the cube.

(8)

b. Write down the exponential expression describing this process (found at the beginning of this paper) and identify all the parameters. List two factors that can influence the distance that the minority electrons penetrate into the semiconductor?

(5)

c. Instead of this injection into one face, the cube is uniformly radiated with light of energy greater than the crystal bond strength (semiconductor bandgap) energy throughout its volume.

(i) Explain physically what happens during constant illumination and soon after the light is suddenly switched off.

(ii) By analogy with the expression for distance variation, write down an equivalent equation for the time variation of the excess carriers in the material from the time the light is switched off, defining each parameter.

(8)

d. In a light intensity measuring device based on the cube in section (c), an electric field is applied across opposite faces of the cube. A light source with photon energy greater than the band-gap and intensity of 10^{17} photons per second illuminates the cube. What is the extra current produced in the device due to the light assuming 100% conversion efficiency of the light into charge. **(4)**

3. **a.** (i) Briefly explain the operation of a planar junction field effect transistor (as used in integrated circuits) using sketches where appropriate but without derivation.

(ii) Describe how it works as both an amplifier and as a switch.

(10)

b. Using the expression for the depletion depth dependence on reverse bias of a "one-sided" (i.e. $p^+ >> n$) abrupt junction given on page 1 of this paper, calculate the pinch-off voltage for a Si junction field effect transistor with a channel thickness of 1 μm and donor density of 1×10^{22} m^{-3}. Assume the built-in potential for the junction is 0.7 V. Would this design be suitable for a digital circuit with a supply voltage of 5 V?

(6)

c. Calculate the channel resistance (resistance between the source and the drain) for this device for a source-drain spacing of 5 μm and gate width (long dimension) of 50 μm. Ignore the thickness of the p-gate region in your calculation. **(6)**

d. Calculate the gate capacitance of this device with an applied gate voltage greater than the pinch-off value, assuming a gate length of 1 μm. **(3)**

4. **a.** Determine the conduction state of the diode in the circuit of fig.4 . Depending on the conduction state, find *either* the forward current or the reverse bias voltage across, the diode. You may assume the diode has a forward voltage drop of 0.7V, but is otherwise ideal.

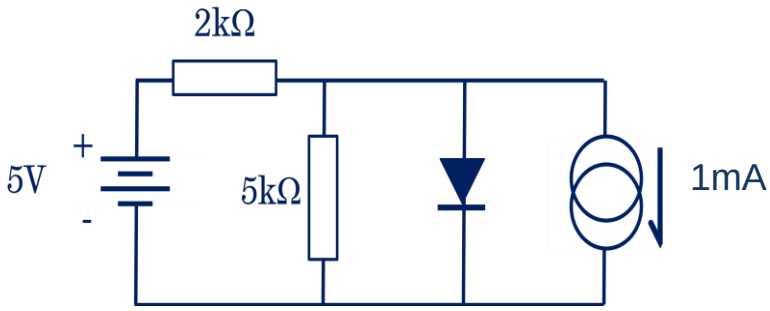


Fig.4 Diode Circuit

(6)

b. Consider the circuit in fig.5.

Draw the output voltage waveshape you would observe if v_i has a triangular waveshape between +10 and -10V .

What is the largest value of forward current through the diode?
(*Note: you may assume the usual voltage drop for a silicon diode)*

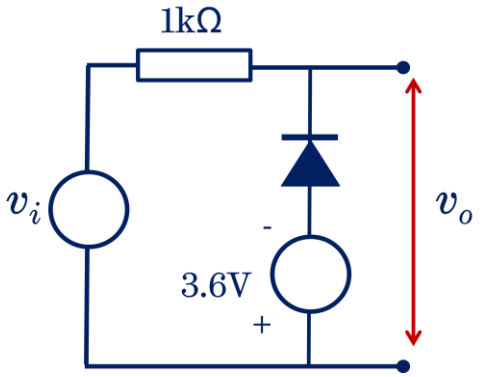


Fig. 5 Diode circuit

(5)

c. Calculate the DC parameters V_C and I_C for the circuit shown in fig.6, using the parameters shown in table 1. Note β is the transistor DC current gain.

What is the purpose of the capacitors C1 and C2 in the circuit?

Draw the small signal equivalent circuit for a transistor. Using your calculations above and the following expressions, work out the values for g_m and r_{be} used in this model.

$$g_m = \frac{eV}{kT} \qquad r_{be} = \frac{\beta}{g_m}$$

Re-draw the circuit of figure 1 into a small signal equivalent circuit (which includes the small signal transistor model).

Parameter	Value
R_F	100kΩ
R_L	5.8kΩ
R_b	12kΩ
V_s	12V
V_{BE}	0.7V
β	400

Table 1

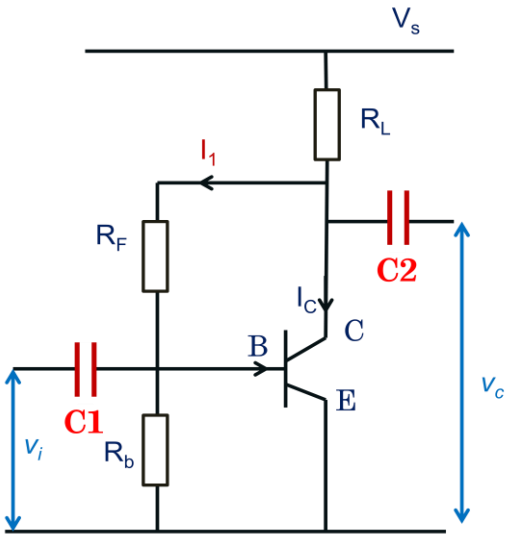


Fig.6 Transistor Circuit **(14)**

5. a. (i) Using the equations for diode current density and saturation current density from page 1, derive the ratio of electron to hole current across the junction.

(ii) In what three-terminal device is this ratio important and why?

(8)

b. The current flowing in a certain Si p-n junction diode at room temperature is 10 μA when a reasonably large reverse bias voltage (not exceeding breakdown) is applied.

(i) Find the junction voltage corresponding to a forward current of 50 mA.

(ii) The diode is constructed with p-type material of conductivity 2000 Sm^{-1} and n-type of 500 Sm^{-1}. Each region either side of the junction is 1 mm long and 0.5 mm^2 in cross-sectional area. Calculate the total voltage drop **(10)**

across the terminals of the diode when 50 mA flows in the forward direction.

c. Identify the terms in the equation for J_0 on page 1 that signifies the importance of the crystal bond strength for determining the reverse saturation current density. **(4)**

d. Sketch two current-voltage characteristics for a diode with and without light shining on it, clearly labelling which is which. Assume that the light can produce electron hole pairs in the device. **(3)**

6. a. Fig.7 shows a rectified power supply in which a transformer reduces the mains supply down to a voltage (V_s) of 12V RMS. The supply drives a load of resistance (R_L) = 50Ω.

Draw the time dependent voltages that you would expect for V_S, V_O and I_C.

Estimate the minimum value of C that can be used to give a ripple voltage of less than 1V peak to peak. You may assume the ripple voltage follows a simple saw tooth waveform. Comment on the value of capacitance you obtain.

Why is this circuit unattractive for applications requiring a stable low noise supply?

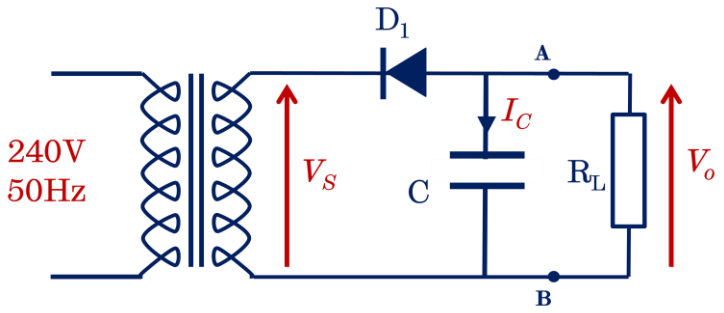


Fig.7 Rectifier circuit

(8)

b. A Zener diode regulator circuit, as shown in fig.8, is inserted in the above circuit at positions A& B. This is used to derive a stable 9V output voltage.

The input ripple voltage is 1V peak to peak. The load may draw a current anywhere between 5mA and 10mA. The Zener diode specifications have a Zener resistance (r_z)= 5Ω and recommend a minimum current through the diode of 2mA.

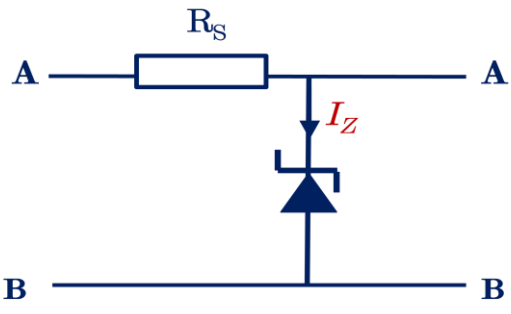


Fig.8.Zener diode circuit

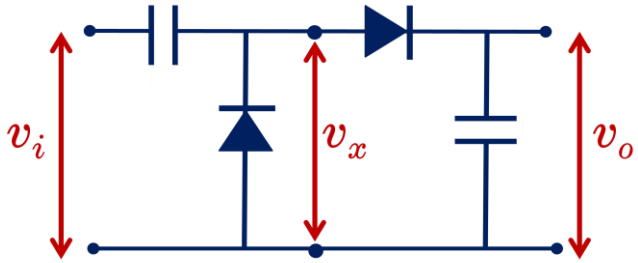
What is the largest value of series resistance that can be used in the regulator circuit? State any assumptions used in arriving at your answer.

Draw the ripple equivalent circuit for fig.7 and use this to obtain the output ripple voltage. **(6)**

c. Draw the basic diode clamp and a diode peak detector circuits, indicating which is which and briefly describe how they operate. To obtain negligible discharge per cycle what should be the relationship between resistance x capacitance (RC) and the signal frequency? **(5)**

d. What is the function of the circuit shown in fig.8?

If the circuit has a sinusoidal input voltage (v_i) of 6V peak-to-peak (+3V to -3V), draw the time dependent voltage waveforms vi, v_x and v_o and indicate their maximum and minimum values. Assume the usual Si diode voltage drop.



(6)

Fig.8.

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