DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2004 (2 hours)

EEE 103 ANALOGUE CIRCUITS 1

Answer **THREE** questions. Solutions will be considered in the order in which they are presented in the answer book and **no marks will be awarded for an attempt at a fourth question.** Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1 **(i)** In figure 1a all the components used are ideal and the load draws a constant current, I_L. Sketch the waveforms of V_S, I_C and V_O that you would expect to observe for these ideal components. {*6*}

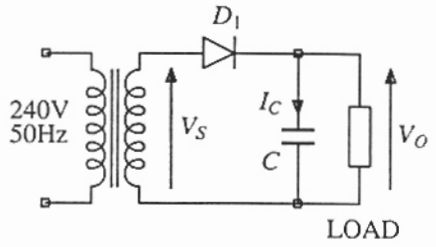


Figure 1a

(ii) Why is a full wave rectifier a more attractive circuit than a half wave one for applications requiring a smooth dc at powers greater than a few watts? {*2*}

D_1 is replaced by a full wave bridge rectifier as shown in figure 1b. The supply is required to provide an average dc output of 30V at a maximum current of 2A and the peak to peak ripple voltage that can be tolerated at maximum load current is 1V peak to peak.

(iii) Suggest a suitable value for the transformer secondary voltage, V_S. {*2*}

(iv) Use an appropriate model to estimate a value of smoothing capacitor, C, that will satisfy the ripple voltage specification given. Be sure to identify any assumptions or approximations implicit in the model you have used. {*4*}

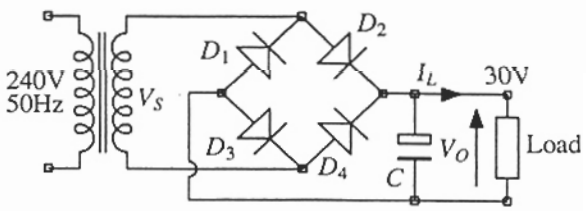


Figure 1b

(v) Estimate the time per 50Hz cycle for which any one of the bridge diodes will conduct when $I_L = 2$A. {*3*}

(vi) Sketch a modified version of figure 1b to show how, by adding a centre tap to the transformer secondary, a positive and negative output can be obtained simultaneously. Label the transformer secondary winding voltage required to get outputs of ± 30V. {*3*}

2 **(a)** The diode in figure 2a has a forward voltage drop of 0.7V. Determine whether the diode will be conducting and work out the reverse bias voltage or the forward conduction current as appropriate. {7}

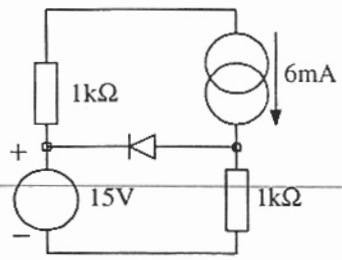
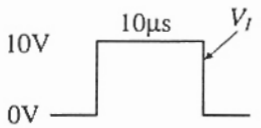


Figure 2a

(b) **(i)** In figure 2b R_1 is initially an open circuit so the circuit effectively consists of R_2 and C only. Sketch V_O in response to the input pulse shown. What is the voltage reached by V_O at the end of the input pulse? Calculate the time for which $V_O > 5$V. *(Remember to think carefully about what will happen to the voltages across the circuit elements at the instant of transient changes of V_I)* {7}

(ii) An R_1 of 1kΩ is included in the circuit. Sketch V_O and I_C over a time period long enough to show all the important aspects of the circuit's response to V_I. Label any exponential shapes with their time constants and label all peak values in the I_C sketch. Assume that D has a forward voltage drop of 0V. {6}



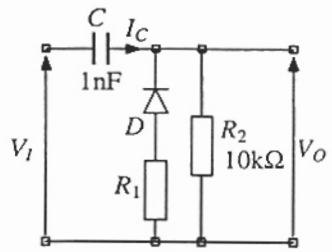


Figure 2b

3 **(i)** What is the purpose of a bias circuit? {2}

The transistor in figures 3a and 3b has a static current gain, h_{FE}, somewhere in the range 100 to 500 and an incremental current gain, β, of 600. The base emitter voltage, V_{BE} is 0.7V.

(ii) For the circuit of figure 3a, work out the maximum and minimum values of I_C and V_C that would be expected due to the spread in h_{FE}. Use your result to explain why this bias arrangement is not very effective. {6}

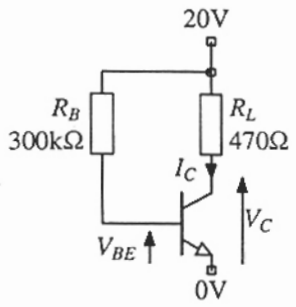


Figure 3a

A more effective bias circuit than that of figure 3a is shown in figure 3b. For the circuit of figure 3b,

(iii) Calculate the dc conditions V_B, I_C and V_C, and the small signal parameters, g_m and r_{be}. Make assumptions that are appropriate for a well designed circuit {5}

(iv) Draw the small signal equivalent circuit assuming that the capacitors can be regarded as short circuits. {4}

(v) Explain how the omission of C_3 would affect the amplifier behaviour. {3}

Assume that a p-n junction has a forward voltage drop of 0.7V and that $kT/e = 0.026$V.

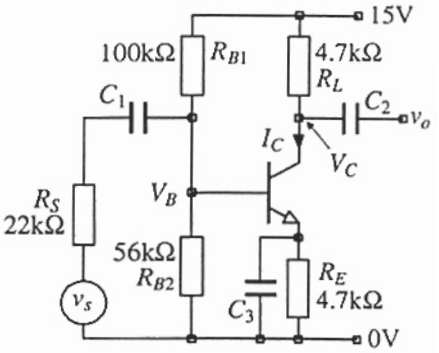


Figure 3b

4 (a) The circuit of figure 4a is a non-inverting amplifier circuit.

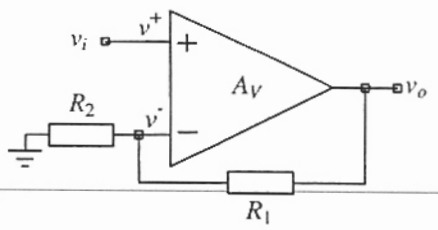


Figure 4a

(i) What does the term "non-inverting" mean? {2}

(ii) Write down the gain, v_o/v_i, of the circuit if the approximation $A_V \rightarrow \infty$ is valid. {1}

(iii) Show that if the approximation $A_V \rightarrow \infty$ is **not** valid, the gain of the circuit is $\frac{v_o}{v_i} = \frac{1}{\left(\frac{1}{A_V} + \frac{R_2}{R_1 + R_2}\right)}$. {5}

(iv) Draw a circuit of an op-amp based inverting amplifier consisting of an op-amp and two resistors. Write down the voltage gain of the circuit in terms of the two resistors used. {4}

(b) The circuit of figure 4b is required to amplify the sinusoidal input so that it appears at the output as a 10V peak to peak sinusoid. It is also required to add a dc offset such that the peak voltage of the positive half cycle of the sinusoid is 10V and the peak voltage of the negative half cycle of the sinusoid is 0V. Find the resistance R_F and the voltage V_1 necessary to achieve the required behaviour. {8}

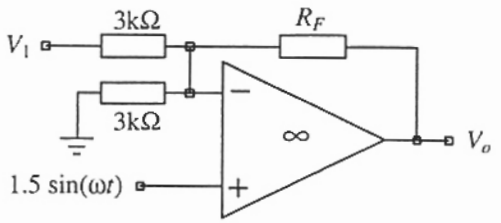


Figure 4b

4RCT/DAS

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