Replies to Questions on Analogue Circuits

These questions relate mostly to EEE225 but somewhat to EEE118 as well as more generally to analogue microelectroincs and electronic systems design. It concentrates mostly on analogue circuits below 30 MHz or so and the topics broadly follow those in the lectures.

Chapter 1. General Questions

1.1 What should I call you/How should I address you?

James or Dr. Green. They are your only good choices. Either is fine.

Please *avoid* the following,

- Games (yes really. With a 'z', i.e. "Gamez" is no better.)
- Dr. Games
- Dr. James
- Prof. Green
- Pro. G. (with or without the final full stop)
- James Green
- James E Green
- Sir
- Tutor
- Teacher
- etc. etc.

1.2 Annotating Circuit Diagrams

> Hi James,
>
> I have been working on the report for my second year design project. I have just had a thought. Should circuit diagrams have annotations on them Or should you just reference the components like V2 is the battery in the text?

It's up to you really. You need to make sure that whatever you choose to do it is clear to someone else besides you (so try having someone else read it and see if they understand)...

Generally I would add DC or AC voltages with respect to ground and branch currents only. But it depends on the field of electronics as well. If I was dealing with an SMPS I'd be thinking in terms of energy or charge transfer.

I would certainly not use an LTSpice drawing in a report. You should re-draw the diagram in Dia or Visio or similar. If you have to use LTSpice for presentation of schematics. I'd make the components and wires black and the background white and turn off the grid - but it's still super ugly!

1.3 Deciding if a university is good for research (choosing an MS or PhD)

Dear Dr. Green,

Does the majority of university funding come from EPSRC?

Can I judge the research direction and strength of a institution by simply see where the money go?

Interesting question. There are a number of ways of measuring the effectiveness of a university department. If you're interested only in research then you can just look at the total "money in" as published by the EPSRC for a given institution, but only a fraction of an engineering department's money comes from EPSRC a lot comes directly from companies and from "innovate UK" (UK government) as well as other research councils such as STFC. Much of this direct income is difficult to confirm unless you have inside information so a true picture is not always easy to gather.

1.4 Exam Technique

I regularly (at least twice a year) get clusters of emails from people who are reasonably intelligent (in my estimation) but are for some reason very bad at exams, or perhaps have been distracted by other things like TSC or alcohol and other substances. They often want advice because they have re-sits to do. I re-sat 4 exams in my first year and 5 in my second, so I know a thing or two about it.

These questions are usually quite melodramatically phrased, "I have failed N exams. I'm doomed/worthless etc. The ground should open up and swallow me etc. etc. Parents will kill me, and so on." Just the sort of thing I like to read on long summer evenings after the results come out, when I could be out with the dog, sitting outside a nice pub with a pint, drinking in a good view over the plains of Warwickshire, watching the sun go down and ruminating over the idea that "...your schooldays are the best days of your life" is one of those truisms that is invariably applicable only to the minority. ;-)

- You are not the only one who has been in this position. My initial score on AMA145 was 24/100 and in AMA156 17/100 (they used to be maths modules taken by EEE students), and they were not the only ones nor were they the lowest scores!
- You need to get consistently good at the skill of taking exams.
- 'Exam skill' is only loosely coupled to "good" or "bad" engineer or "good" or "bad" student. It's possible to be a useless engineer who scores 90+ on written timed tests (exams). This is because taking exams is nothing at all like the real world. Holding knowledge under certain controlled conditions and being able to apply it to a prescribed set of problems all of a similar kind is dis-similar to almost everything that happens in the day to day work of most people, not just engineers. Nevertheless we must test capacity to comprehend and utilize the basics somehow as proof of ability to progress to either research or industry. That is all the undergraduate degree is, the bare bones.

I propose that you work out how many hours you need to spend on the credits you failed. To do this multiply the number of credits by 10 and then subtract the number of hours of lectures. So in a 20 credit module with 36 hours of lectures you would have to spend 164 hours. This is the amount the university demands for a 20 credit course (it's in the handbook).

When I was doing my resits (both first and second year) I got up at about 0830 am washed, dressed and made some quick breakfast. At 0900 I sat down at a big table (big enough for 8 people) with the breakfast, my notes, the problem sheets and the past exam papers. I worked until 1200 and then stopped for 30 minutes in which I made and ate lunch. Then I worked until 1830, when someone had prepared dinner for me. I ate and rested or went for a walk for 1 hour and then worked from about 2030 until 0000. I went to bed immediately. Mental exhaustion means that you sleep easily and a bit of fresh air helps. I did this every day for 6 weeks and passed all of them except AMA243 which I got 36 on second time round, but they let me carry on without passing it.

To actually do the work, first I sat with my lecture notes and made notes on the notes. In the case of courses where the lecturer didn't give out notes (it was traditional for students who attended to write them down, and this ancient and venerable practice can still be found here and there), I found a good book on the book list. I looked at the published course syllabus and matched up the chapters to the syllabus and looked for example questions in the book like the ones in the past exam papers. I used the book to write the course based only on the kinds of questions on the exam and the syllabus headings and to teach this material to myself in the process. The writing and the teaching happened broadly

together because I only wrote down in the new set of notes things I understood and I judged the understanding by being able to explain it to myself and to work through (on rough paper) the examples that were given in the notes and/or book. If I didn't know what the terms in the equations meant I would stop and look back in the notes/book until I found out or understood. By the time I finished I had a new set of notes as well as the original course notes (presuming that is I had showed up to write them out in the lectures otherwise I just had my version of the course notes), where my understanding was good the new notes were brief. Where my understanding was bad initially, my new notes had lots of extra details. I believe that the writing out of all the extra detail and the endless doing of example questions enforces the understanding. Much less material was available on-line then than now. In my own teaching I always give out everything that a candidate needs to pass the course.

Once I finished the new notes for a course I would use the notes to do all of the problem questions presuming I'd not tackled them along the way. I would not look at the answers unless I tried a problem for a long time without success. When I looked at the answer I would look only at the method briefly, 5 seconds, just to see the path to take. Then go back and do the question knowing the correct path of the analysis.

Having finished all the problem sheets I would start on the past exam papers. I would try to have 5 papers minimum for each module. We used to be able to go to "the main library" (pre IC, pre Diamond the Western Bank Library was called the Mail Library) and copy more than 20 years of passed papers if we were willing to pay the photocopying fee, mobile phone cameras had not yet been sufficiently developed so that the number of pixels rendered a passable image of an A4 page. This looking up of old papers was necessary as the department usually gave only 3 on-line. I would do 3 of the 5 with the answers next to me and look at them if I needed to. The first one I usually need to a bit, but after that I didn't look at the answers much at all. The last two papers I would do "blind" and I would only allow myself 2 hours (the length of the exam). Then I would mark them (as best as I could) to ensure I answered all parts of the question in the way the staff member answered it. If I didn't get the method properly I would go back to my notes and figure out why the method of the answer was the one given and not the one I thought it would be. It is infuriating how many lines of method staff members skip in solutions to exams. Of course it's only infuriating if one doesn't understand the method and the people writing the exam solutions *do* understand the method. Sometimes the staff made mistakes in the answers and it cost me time figuring out that I was right and they were wrong, because one starts with the presumption that their solutions are correct. Everyone makes mistakes though.

I didn't have enough hours between the day I worked out how many hours I needed and how many were left available before the first resit exam. That is why I failed AMA243 at the second attempt – I ran out of time to do the work.

If you do this as I have described it, and are *honest* with yourself about your own understanding, you will succeed assuming there is sufficient time available. If you can help it, do not spend time being afraid or worried, this is wasted time. I remember it was a very great intellectual effort and strain; something to be avoided if at all possible.

1.5 How should I decide about a PhD?

> Dear James,
>
> I have been trying to decide about industry or a PhD. I know it's an individual choice but I would like to know what you think.

It is difficult to advise on this topic as much of it is feelings and opinion and they are clouded with the built in bias of the person holding those opinions. I suppose in the general sense if the university is in the QS world top 100 for your chosen subject then it's probably going to be OK but, like a lot of statistics, it tells you nothing about how you will get on with your supervisor, if you will like the place / city / country etc. how you will fair on your particular research problem etc. So much of the specifics of your particular case are uncertain it's impossible to say anything concrete.

General advice:

1. It is not for many people and it should not be chosen lightly. It is not a means to avoid not being a student any more. A good supervisor will not take you on if they believe that is your reason for doing it.
2. It will not pay as well as industry does, while you're doing it. The money comes later.
3. Go look round the place. Including the offices, the laboratories, the union etc.
4. Consider where you will stay, the cost of this etc.
5. Talk at length with the potential supervisor. Do not bother talking about the research too much. Try to find out as much as you can about them. You need to try to judge what kind of person they are. *Much*, especially your mental health, depends on your relationship with your supervisor. If they are engaged with your research, by the time you are finished they will know you better than your parents.
6. Find out the fee and if you will have to pay it. If you have a stipend find out how much and the terms and the length of time.
7. Investigate scholarship options and how to apply for them. Discuss this with the supervisor. It would be well to do this at least 9 – 18 months in advance of your expected start date.
8. Find the current PhD students supervised by your potential supervisor and talk at greater length with them, preferably over lunch, alone. This will be the best source of information, but it will be coloured by their experiences good, or bad.
9. Find out what journals their current students are publishing in. Are they any good?
10. Find out the average number of transactions papers (not letters or conference papers etc.) their students produce during a PhD. If the average is less than two it should make you very worried (unless their research is particularly industrially focused/funded). This number only applies to EEE and is probably going to be the most contentious thing I write here. Publications are important because publication is the validation of the scientific merit and novelty of the research by the scientific community. Novelty and accuracy are what's required to get you the PhD. If prior students have not published a reasonable amount in reputable journals it means that something is not right. That said I have a student in his fourth year, funded by

a company, and we're not publishing anything – it's all confidential. This is the exception though, most good science is published.

Every PhD is totally different to all the others, but there are some commonalities that one may only see after a long period of reflection. These commonalities seem to exist independent of your relationship with your supervisor and there is not a single person I have met working across all fields of medicine, physical sciences, engineering and mathematics that doesn't report these things, however intelligent or mentally "tough" they may appear.

- However well planned it is, the plan will only exist on paper, the reality will never match the plan.
- You will work a $60-70$ hour week fairly regularly. When you're not working, you will dream about it.
- The friendships you form with others in your research group will cross continents and some will never grow stale.
- You will break every piece of equipment in the lab at some point. The more expensive it is the more likely you are to break it earlier on in the PhD. The more important it is to your work the more likely it is to be broken at a critical time in the research. As I write this one of my students has just yesterday told me he's accidentally warped some of the laminations of a machine he's building and he's very near the 4 year mark. Cutting new laminations is a long process and he hasn't enough time, we must fix them somehow.
- You will fix every item of equipment in the lab at some point and this will be part of the training. You will think it's a distraction and is slowing you down but, it will do you good. The people who have to struggle most finish up being the best.
- You will achieve nothing of use in the first 6 to 18 months or so. You will not fully appreciate the problem, despite reading all the literature and you will be too busy breaking and fixing things to do any good experimental work. Your experimental technique will be awful as well. It's like bread, it takes lots of practice and you can't rush it.
- You will need an extension past 3.5 years. It will take somewhere between 3 and 10 years but most likely 4 to 4.5 years.
- When it is not going well you will feel lonely even when you are surrounded by people. You will decide that they do not understand how you feel – even if they are also PhD students ~~suffering~~ experiencing nearly identical problems to you. You will believe that everyone else's PhD is easier than

yours especially if they are in your discipline area.

- It will very likely change your personality permanently. It may affect your relationships with others.
- If you hang on, it *will* all come together in the end, probably quite suddenly in the last 6 months or so.
- It will teach you things far beyond the topic area, things that can only be learned by a similar period of intense intellectual struggle, things about yourself.
- It will most likely be the zenith of your personal intellectual achievement. There may be greater achievements in the future that you will somehow be involved with, probably in some minor capacity, but this one will be all yours. It will be impossible to explain how you feel about it in words. Only another doctorate may understand the feelings you hold for it and, when it is finished, if you believe that you have done it justice, it will be beautiful in your eyes.
- It is the gateway to another world.

If you're not frightened off by that lot then it's probably for you, because most normal people would run to the hills – run for your lives. If you think I'm exaggerating for comic effect then try this, https://goo.gl/caUxhB or, for the other side of the lens, Google "My PhD supervisor hates me" without the quotes. I'm sure you can find something to paint a vivid picture. In fact if I pull Google.co.uk up now and type in "my PhD supervisor" without quotes and wait a second or two, the auto-complete options are:

- hates me
- thinks I'm stupid
- is bullying me
- is moving
- is leaving
- doesn't like me
- ignores me
- is retiring
- died

"Big data" has shown what the population of PhD students in the UK are looking for with regards to their supervisor and it doesn't look good. Of course no one

in their right mind would Google "my PhD supervisor is a lovely person who gives me the impression that they think I'm competent despite the overwhelming evidence to the contrary and trusts me to get the job done even though I blow up all their expensive equipment every time I go near their lab" would they?

This idea that PhDs are form of torture handed down to unsuspecting people in their early 20s perhaps in retribution for crimes they committed in a prior life, and that professors are all fire breathing dragon-like divas who are impossible to work with and change their minds like the wind, is very ingrained in certain parts of society. Some perhaps even many people believe that a supervisor isn't doing their job properly unless they're a complete git to you...https://goo.gl/nFWTVy, which is just non-sense. I've never been mean to my people and they've still thrown tantrums and suffered internal strife just the same as other people who've had supervisors with a range of different approaches. That's not to say the student is at fault, just that the frailty of human nature is exposed by pressure and it's not always easy for the student to cope and not easy for the supervisor (even with the best intentions) to act in the most helpful or useful way.

Sometimes the student really is totally blameless. Once, I borrowed a very expensive (6 figures) Argon laser from a professor at Sheffield. It was too big to move it had water cooling and nitrogen supplied to it and it was the sort of thing where no major spare parts cost less than than $10k. He knew I was using it. One day I got an email from him saying the laser was found broken after I used it and I was "banned from the room until it was fixed" and that I "couldn't use it unless I was supervised by [one of his research associates (a post-doc)]". He wasn't angry but I knew he would be on the inside as the company who made it would come to fix it and they would charge at least $750 just to come to the university never mind to actually fix it. Then there is the problem of other experiments. I was effectively stopping a number of other PhD students and RAs doing their research, how embarrassing. This was very bad for me, I liked to work late at night because the EMC in the department was lower then, also laser time was hard to come by as many people needed to use it. My experiments were measuring noise in semiconductors and the fluctuations I was interested in are fantastically small so late at night was good for me. Even when it was fixed there was no chance that an RA would work with me until 2000 never mind midnight or later. Moreover, I *didn't* break the laser! I was fairly angry that I was accused as my period of breaking everything had long since passed and I thought I was regarded as at least quite competent by most people. I didn't like the idea that I was effectively accused of hiding the fact that I'd broken it as well. He didn't say that but it was implicit since he concluded it was me and I didn't say I'd broken it, I must have known and then hidden the fact... Perhaps this is the point where people go off for a little cry, I might have, had it not been in the middle of the research and after the period of breaking everything, when I could just look at

kit, especially expensive optics, and they would magically break. I decided... to break... into the lab. And fix it. Before they called out the service technician from the company. The laser was working when I switched it off and I cooled it down properly, there was no water or gas leak and no evidence of fire, so it couldn't be a serious problem. Breaking in was easy, no-one ever changed the door codes. After a bit of tinkering and leafing through the error codes in the service manual it transpired that the little bulb that back-lit the "Laser Emission" sign right above the output mirror had blown spontaneously just because light-bulbs don't last forever and I was unlucky that I was the last person to use it before it died. I ordered an unbranded one from RS, waited for it to arrive, broke in again, changed the bulb, tested the laser, and emailed him to explain it. He was very friendly with me thereafter and regarded me as highly competent in many areas of electro-optics, probably more competent than I actually was!

Of course sometimes it is the student's fault. There is still a noise figure meter under a desk in a lab somewhere which I blew the front end up on during my first 6 months. It doesn't matter how but by the time I realised the mistake it was way too late. We've never found a company that could fix it and I've never got round to it myself. The kit was 30 years old by that time, the company that made it stopped supporting it years ago and a Prof. with spare cash brought a shiny new one about 3 months afterwards and the problem went away. But I have never even seen the service manual for that NFM, I could have learned a lot by fixing it and I should have. If I did it now, it would teach me something, probably something interesting, perhaps something cool that I could apply to some other research problems I've got. The fixing really is the training.

Having established that generally speaking the student and the supervisor are not actively culpable for the times when things don't go well, and that they generally don't mean for things to go badly, what would I avoid in a student? Laziness. It's the only thing I can't help with. If the student is not willing to work very very hard no amount of help, encouragement or fire and brimstone from me will make any difference at all. I learned this the hard way too, it was a mistake that lasted three years and I'll never make it again. I'd sooner have no-one than the wrong one. This may give some insight into my list of advice. On first reading it's mostly negative and the good stuff seems fairly cryptic at best and probably just bizarre. It says you'll suffer, initially be paid less that your colleagues in industry and work twice as many hours. If you are going to succeed and get the PhD you will do these things, and ultimately you will view it has having been worth it.

Most people who want to get a PhD know they want to, sometimes they can't even articulate why when asked, they just know. Not everyone is like this but no-one has to be talked into it. If you find someone talking you into it then you

should consider carefully if it's what you really want. The first question I ask when interviewing someone is, "why do you want to do a PhD?" In fact most of the interview is me trying to convince them that they don't want to do it, and if I fail, they must really want it. I will then consider their grades and what funding if any I have available and my view of their intellect and the view of their prior supervisors.

No-one has ever said to me "my supervisor thinks I'm stupid" or "hates me" etc. but if they did I would be incredulous. Obviously I'd feel sad for them and try to help but in general I have no doubt that the supervisor would not say they thought these things. I am fairly sure of this because when I take someone on I don't think that they *might* be successful. I fully believe that they will finish the PhD and I generally have a plan of their whole PhD (in broad brush strokes or bullet points). It is often the case that the plan is changed radically if we discover something interesting or if the problem is found to be much less tractable than I first thought. In general the first half is broadly to the plan and the second half is broadly led by the student based on the outcome of the first half. If I thought someone was stupid or I didn't want to work with them I wouldn't have taken them on in the first place! If I have lost faith in a student's capacity to finish and I fear it is irrecoverable I'd have to sit them down and tell them that I didn't think they would ever get the degree and that they should look for a job or write up for a lower degree (MPhil). That would be my failure, I would have taken someone on believing they could finish and then found I was mistaken. Supervisors hate it when this happens, it makes them feel stupid and that stings because we're supposed to be clever by definition. In this case there are no research outputs (papers, thesis etc.) and the student does not graduate. The time and money (if any) the supervisor invested in the student has also been effectively wasted because their training didn't result in any research outputs. Surviving in academia as a tenured academic requires a lot of drive and self-belief and a good deal of luck too. We don't work as many hours as when we were PhD students, but we do work a lot more than the legal maximum per week. Sometimes I wonder if supervisors that loose their rag at students are just frustrated because they feel the pressure of needing to produce a finished product (a graduated student, the research outputs etc.) in much the same way that PhD students feel pressure and frustration about their experiments not going to plan and their time limit approaching.

Doctoral study is made up of lots of little battles. To get equipment working. To stop people stealing the equipment that you, and they, need to get results. To get some data you need. To convince your supervisor that the data is accurate. To convince journal reviewers that your discussion is scientifically valid. Most people have to battle with themselves to some extent as well. I have never come across an example of someone not finishing (i.e. quitting or taking a lower degree

(MPhil)) when they were intellectually capable because of some tangible research based problem. It's almost always what's going on in their head that holds them back. These things are all part of it and overcoming them will teach you things about yourself that can not be taught by any other means. If you really want it you must/will not let anything stand in your way. If on the other hand you just don't want to leave university well then you'll probably not last 6 months.

I like to think there are actually two universities in spatial superposition with each-other. One which undergraduates experience and another which post grads experience, same corridors, same buildings, but a totally different set of goals and an utterly different learning experience. There is only the slightest crossover between the two, for example in problem classes where the doctoral candidates and the undergraduates interact. Anyone having experienced only the first as an undergraduate and expecting it to continue when they take up postgraduate study would be wise to reconsider their position.

Chapter 2. Historical

2.1 The Collision of Digital and Analogue

Sometimes it can be difficult to reconcile how the various bits of modern electronic engineering go together (analogue, digital, magneto-statics, electro-magnetics etc.). It might be intellectually profitable to go 'back' to when the divisions between analogue and digital were so blurry they didn't really exist. http://youtu.be/Z_qH6CnyxT8 especially 6:52 on-wards. Of course I say go "back" (in quotes) because underneath all that digital stuff is really analogue in disguise.

General info about the EDSAC project can be found on the National Museum of Computing Web-pages at: http://www.tnmoc.org/special-projects/edsac. If you've not been, it's well worth a visit, as is the Porthcurno Telegraph Museum http://www.porthcurno.org.uk (somewhat longer trip though).

2.2 Gravity Waves

Unless, like Matt Damon, you've been spending a lot of time on Mars, the reports of the first direct detection of gravitational waves are probably familiar.

It's often not apparent how many engineers work in "big science", it was always unlikely that an electronic engineer would share the Nobel prize for the first direct detection of gravitational waves. Three theoretical physicists won it and many would argue deservedly so. I'm not contradicting it. The question of who deserves the prize for these big experiments when so many people contribute, though, is a cause of some debate at the time of writing. I do wonder if there is much chance of an experimentalist (someone who actually gets their hands dirty

in a lab) winning it many more times. Most of the big questions are tackled by huge teams and these are generally lead by theoreticians. There are, most likely, as many engineers involved with the latest triumph of big science as there are physicists. In the grand scheme of things almost none of the physicists or engineers have anything more than their name on some journal papers and the feeling of satisfaction they derive from knowing they were part of it. Fortunately, for the great majority that feeling (and a pay slip) is enough.

Since we're on the subject of Nobel prizes, I would like to draw your attention to a familiar circuit which is bound together with a much earlier experimental observation related to relativity. When it was first observed, it was just as powerful as gravity waves are considered presently. Cockroft and Walton shared a Nobel prize in physics in 1951 for the first laboratory demonstration of nuclear fission. Lithium was "transmuted" into Helium, energy and a proton were released. Energy and mass were exchanged as a result of human activity for the first time. They achieved this in the 1930s using an early example of a particle accelerator in which the electrostatic field that accelerated the charged particles towards the target was provided by a Cockroft Walton voltage multiplier circuit (EEE118).

Figure 2.1: Cockroft and Walton's plaque at Trinity College, Dublin.

At the time of the observations their data provided the first experimental validations of $E = mc^2$.

Just in case you're wondering, Einstein won the 1921 Nobel Prize for Physics for "Services to theoretical physics and especially for the discovery of the [law of the] photoelectric effect" (also EEE118 - semiconductors part). Looking back this may seem somewhat surprising, photoelectric effect is a given for us, certainly very important. But, some people might argue that the second half of the twentieth century was dominated more by the effects of special relativity than of the photoelectric effect. It may never be clear why the Nobel council made this choice but we may glean something (as we often can) by attempting to view the world through the eyes of others, the committee in this case. Considering, from their perspective, the recent history of physics specifically the *Rayleigh–Jeans catastrophe* we might draw some conclusions. Still, there is no time now for more discussion, you'll have to go and read some pop-science books.

Greetings from Trinity College, Dublin.

2.3 Can we have a reading week?

A few years ago someone asked for a reading week. So I was encouraged to think about what an engineering student might read if they viewed the world through a social scientist's eyes and had a week free and what we might achieve...

Dear All,

Recently, I've been thinking about why social scientists and humanities majors read stuff. I believe it is because they need to observe the landscape of their discipline through the viewpoints of the key workers and then come to some rational, supported argument that sums up their opinion on the present state of their discipline in a particular area. Their opinion is a reflection of themselves. Actually developing and recognising the characteristics of the opinion rather than just subconsciously holding it can be a very useful exercise in introspection.

Engineering students don't have any equivalent necessity in a taught degree program to reflect on themselves or the reasons they do things. We are used to producing answers which are often right or wrong, usually there is little middle ground or room for argument and counter argument. So we might wonder if engineering students need to have this broad viewpoint about something as fundamental as what it means to be an engineer? We might even consider how similar or different is a quest for knowledge compared to a quest for a degree certificate?

An engineering approach to exams might run as follows: I tell you what I might examine, you learn about 75% of the material and trust 25% of it to your luck based on the principle that whatever I asked last year wont come up this year, and then score about 55% on the exam (on average). You are just an optimisation algorithm trying to get the most marks for the least effort. You tell yourself that it's necessary there are other exams besides this one... No reading, no introspection, no problem. Similarly if I say I will pass all of you no-matter what, will you still work as hard/at all? If I doubled the cost of the degree (again ;-)), would you work twice as hard? Are you trying to become good at electronics or just trying to hold a degree certificate? They are in fact different objectives, which can, more or less, be met simultaneously, if you're careful.

Thinking about the 'big picture' will (probably) help you define your own goals and career path in the short and long term. What is the difference between an engineer who is valuable to their organisation and someone who just holds a certificate in their hand and 'holds down' a job? The differences cannot be learned from a book or tested in an exam hall.

In short, it could be very useful to start thinking about what you're actually trying

to achieve from your time as an undergraduate, for most of you it is almost half gone ;-) And that is a perfect excuse for me to give you some reading, social scientists have a whole reading week, I'm sure you can manage a thousand words or so. I've dug up something short by Jim Williams. I would encourage you to read it and try to "get inside his head" and imagine how he feels about electronics. How much of his world view do you empathise with? How similar/different are your approaches to learning?

To provide some background on Jim, his biography is at the bottom.

If you've read his bio you'll know that Jim was a crusty, old(ish), white, American, man who was writing in the early 1990s about his experiences of learning how to actually do electronics more than 40 years prior. So, you could be forgiven for thinking that you wont have much in common. However, all good engineers share fundamental qualities irrespective of their discipline or the time in which they lived.

To provide a more 21st century perspective on the same theme I would like to impose a couple of YouTube videos on you as well, think of it as a modern version of reading, with pictures. These are presented by a person who has designed and produced commercial mixed signal ASICs despite having no degree or formal qualifications beyond the age of 16. Among a long list of things, she worked for Valve software for several years and once raised $0.4M through Kickstarter in just over 48 hours. At the time of writing Jeri runs her own company, employing around 75 people, working on augmented reality vision systems.

Jeri's Biography: https://youtu.be/cLy0mVkoLio

And then something to think about: https://youtu.be/xhQ7d3BK3KQ

Jim's Biography Jim Williams was at the Massachusetts Institute of Technology from 1968 to 1979, concentrating exclusively on analogue circuit design. His teaching and research interests involved application of analogue circuit techniques to biochemical and bio-medical problems. Concurrently, he consulted U.S. and foreign concerns and governments, specialising in analogue circuits. In 1979, he moved to National Semiconductor Corporation, continuing his work in the analogue area with the Linear Integrated Circuits Group. In 1982 he joined Linear Technology Corporation as staff scientist. Interests included product definition, development, and support. Jim authored over 250 publications relating to analogue circuit design. He received the 1992 Innovator of the Year Award from EDN Magazine for work in high-speed circuits. His spare time interests included sports cars, collecting antique scientific instruments, art, and restoring and using old Tektronix oscilloscopes. He lived in Palo Alto, California with his son Michael, a dog named Bonillas, and 28 Tektronix oscilloscopes, he passed away in 2011.

If you're into the socials: http://twitter.com/jeriellsworth http://www.facebook.com/jeri.ellsworth, http://www.youtube.com/user/jeriellsworth

The Art and Science of Analog Circuit Design

Edited by

Jim Williams

Butterworth–Heinemann

Boston Oxford Melbourne Singapore Toronto Munich New Delhi Tokyo

MIT building 20 at 3:00 A.M.
Tek. 547, pizza, breadboard.
That's Education.

1. The Importance of Fixing

Fall 1968 found me at MIT preparing courses, negotiating thesis topics with students, and getting my laboratory together. This was fairly unremarkable behavior for this locale, but for a 20 year old college dropout the circumstances were charged; the one chance at any sort of career. For reasons I'll never understand, my education, from kindergarten to college, had been a nightmare, perhaps the greatest impedance mismatch in history. I got hot. The Detroit Board of Education didn't. Leaving Wayne State University after a dismal year and a half seemed to close the casket on my circuit design dreams.

All this history conspired to give me an outlook blended of terror and excitement. But mostly terror. Here I was, back in school, but on the other side of the lectern. Worse yet, my research project, while of my own choosing, seemed open ended and unattainable. I was so scared I couldn't breathe out. The capper was my social situation. I was younger than some of my students, and my colleagues were at least 10 years past me. To call things awkward is the gentlest of verbiage.

The architect of this odd brew of affairs was Jerrold R. Zacharias, eminent physicist, Manhattan Project and Radiation Lab alumnus, and father of atomic time. It was Jerrold who waved a magic wand and got me an MIT appointment, and Jerrold who handed me carte blanche a lab and operating money. It was also Jerrold who made it quite clear that he expected results. Jerrold was not the sort to tolerate looking foolish, and to fail him promised a far worse fate than dropping out of school.

Against this background I received my laboratory budget request back from review. The utter, untrammeled freedom he permitted me was maintained. There were no quibbles. Everything I requested, even very costly items, was approved, without comment or question. The sole deviation from this I found annoying. He threw out my allocation for instrument repair and calibration. His hand written comment: "You fix everything."

It didn't make sense. Here I was, under pressure for results, scared to pieces, and I was supposed to waste time screwing around fixing lab equipment? I went to see Jerrold. I asked. I negotiated. I pleaded, I ranted, and I lost. The last thing I heard chasing me out of his office was, "You fix everything."

I couldn't know it, but this was my introduction to the next ten years. An unruly mix of airy freedom and tough intellectual discipline that

would seemingly be unremittingly pounded into me. No apprenticeship was ever more necessary, better delivered, or, years later, as appreciated.

I cooled off, and the issue seemed irrelevant, because nothing broke for a while. The first thing to finally die was a high sensitivity, differential 'scope plug-in, a Tektronix 1A7. Life would never be the same.

The problem wasn't particularly difficult to find once I took the time to understand how the thing worked. The manual's level of detail and writing tone were notable; communication was *the* priority. This seemed a significant variance from academic publications, and I was impressed. The instrument more than justified the manual's efforts. It was gorgeous. The integration of mechanicals, layout, and electronics was like nothing I had ever seen. Hours after the thing was fixed I continued to probe and puzzle through its subtleties. A common mode bootstrap scheme was particularly interesting; it had direct applicability to my lab work. Similarly, I resolved to wholesale steal the techniques used for reducing input current and noise.

Over the next month I found myself continually drifting away from my research project, taking apart test equipment to see how it worked. This was interesting in itself, but what I really wanted was to test my

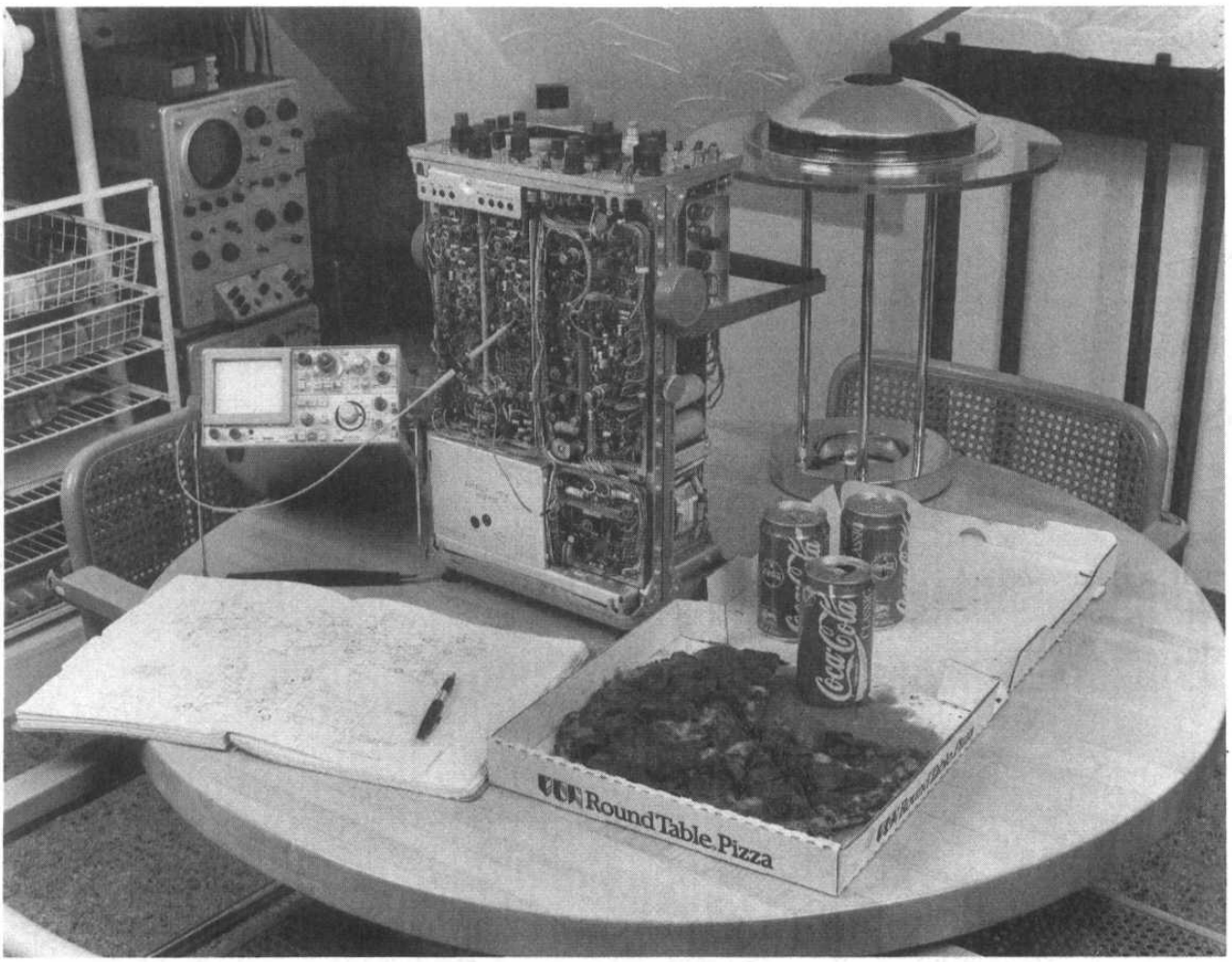

Figure 1–1. Oh boy, it's broken! Life doesn't get any better than this.

understanding by having to fix it. Unfortunately, Tektronix, Hewlett-Packard, Fluke, and the rest of that ilk had done their work well; the stuff didn't break. I offered free repair services to other labs who would bring me instruments to fix. Not too many takers. People had repair budgets . . . and were unwilling to risk their equipment to my unproven care. Finally, in desperation, I paid people (in standard MIT currency—Coke and pizza) to deliberately disable my test equipment so I could fix it. Now, their only possible risk was indigestion. This offer worked well.

A few of my students became similarly hooked and we engaged in all forms of contesting. After a while the "breakers" developed an armada of incredibly arcane diseases to visit on the instruments. The "fixers" countered with ever more sophisticated analysis capabilities. Various games took points off for every test connection made to an instrument's innards, the emphasis being on how close you could get utilizing panel controls and connectors. Fixing without a schematic was highly regarded, and a consummately macho test of analytical skill and circuit sense. Still other versions rewarded pure speed of repair, irrespective of method.[1] It really was great fun. It was also highly efficient, serious education.

The inside of a broken, but well-designed piece of test equipment is an extraordinarily effective classroom. The age or purpose of the instrument is a minor concern. Its instructive value derives from several perspectives.

It is always worthwhile to look at how the designer(s) dealt with problems, utilizing available technology, and within the constraints of cost, size, power, and other realities. Whether the instrument is three months or thirty years old has no bearing on the quality of the thinking that went into it. Good design is independent of technology and basically timeless. The clever, elegant, and often interdisciplinary approaches found in many instruments are eye-opening, and frequently directly applicable to your own design work. More importantly, they force self-examination, hopefully preventing rote approaches to problem solving, with their attendant mediocre results. The specific circuit tricks you see are certainly adaptable and useful, but not nearly as valuable as studying the thought process that produced them.

The fact that the instrument is broken provides a unique opportunity. A broken instrument (or anything else) is a capsulized mystery, a puzzle with a definite and very singular "right" answer. The one true reason why that instrument doesn't work as it was intended to is really there. You are forced to measure your performance against an absolute, non-negotiable standard; the thing either works or it doesn't when you're finished.

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1. A more recent development is "phone fixing." This team exercise, derived by Len Sherman (the most adept fixer I know) and the author, places a telephone-equipped person at the bench with the broken instrument. The partner, somewhere else, has the schematic and a telephone. The two work together to make the fix. A surprise is that the time-to-fix seems to be less than if both parties are physically together. This may be due to dilution of ego factors. Both partners simply must speak and listen with exquisite care to get the thing fixed.

The reason all this is so valuable is that it brutally tests your thinking process. Fast judgments, glitzy explanations, and specious, hand-waving arguments cannot be costumed as "creative" activity or true understanding of the problem. After each ego-inspired lunge or jumped conclusion, you confront the uncompromising reality that the damn thing still doesn't work. The utter closedness of the intellectual system prevents you from fooling yourself. When it's finally over, and the box works, and you know why, then the real work begins. You get to try and fix you. The bad conclusions, poor technique, failed explanations, and crummy arguments all demand review. It's an embarrassing process, but quite valuable. You learn to dance with problems, instead of trying to mug them.

It's scary to wonder how much of this sort of sloppy thinking slips into your own design work. In that arena, the system is not closed. There is no arbitrarily right answer, only choices. Things can work, but not as well as they might if your thinking had been better. In the worst case, things work, but for different reasons than you think. That's a disaster, and more common than might be supposed. For me, the most dangerous point in a design comes when it "works." This ostensibly "proves" that my thinking is correct, which is certainly not necessarily true. The luxury the broken instrument's closed intellectual system provides is no longer available. In design work, results are open to interpretation and explanation and that's a very dangerous time. When a design "works" is a very delicate stage; you are psychologically ready for the kill and less inclined to continue testing your results and thinking. That's a precarious place to be, and you have to be so careful not to get into trouble. The very humanness that drives you to solve the problem can betray you near the finish line.

What all this means is that fixing things is excellent exercise for doing design work. A sort of bicycle with training wheels that prevent you from getting into too much trouble. In design work you have to mix a willingness to try anything with what you hope is critical thinking. This seemingly immiscible combination can lead you to a lot of nowheres. The broken instrument's narrow, insistent test of your thinking isn't there, and you can get in a lot deeper before you realize you blew it. The embarrassing lessons you're forced to learn when fixing instruments hopefully prevent this. This is the major reason I've been addicted to fixing since 1968. I'm fairly sure it was also Jerrold's reason for bouncing my instrument repair allocation.

There are, of course, less lofty adjunct benefits to fixing. You can often buy broken equipment at absurdly low cost. I once paid ten bucks for a dead Tektronix 454A 150MHz portable oscilloscope. It had clearly been systematically sabotaged by some weekend-bound calibration technician and tagged "Beyond Repair." This machine required thirty hours to uncover the various nasty tricks played in its bowels to ensure that it was scrapped.

This kind of devotion highlights another, secondary benefit of fixing. There is a certain satisfaction, a kind of service to a moral imperative,

that comes from restoring a high-quality instrument. This is unquestionably a gooey, hand-over-the-heart judgment, and I confess a long-term love affair with instrumentation. It just seems sacrilege to let a good piece of equipment die. Finally, fixing is simply a lot of fun. I may be the only person at an electronics flea market who will pay more for the busted stuff!

2.4 Beat the Buzz

Dear All,

None of you really seemed to have any idea about the beat the buzz game that I suggested was a "fun" use for a Darlington pair or triple. Specifically a situation where a very small base current needs to control a much large current.

A super simple example (battery and buzzer, no transistors) https://www.youtube.com/watch?v=KG6fg1QO1gw

Something from my childhood https://www.amazon.co.uk/Childrens-Beat-Buzzer-Co-ordination-Grafix-x/dp/B00HYW1Z3S

Yes, toy packaging really did look like that, it was a simpler time...

One of the key problems with the game in the YouTube video is that the buzzer takes some time to be activated and if you're really fast or have a very poor (light) contact it will not buzz. When it does buzz we'd like it to stay buzzing so there is no pretending that you "didn't hear it". The sensitivity can be increased almost without limit by cascading transistors in the Darlington structure which act as a sensitive switch. The "staying on" is perfect for a standard two transistor latch circuit. Both can be found either in Google images or in the design ideas pages of Horowitz and Hill. Alternatively a double pole double throw relay can be used to make a latch but it will consume more power than a two transistor latch.

I think you should club together and build one, with a score board and lights and all sorts. Obviously you can lift parts from the EEE store to do this...

Chapter 3. Component Technology

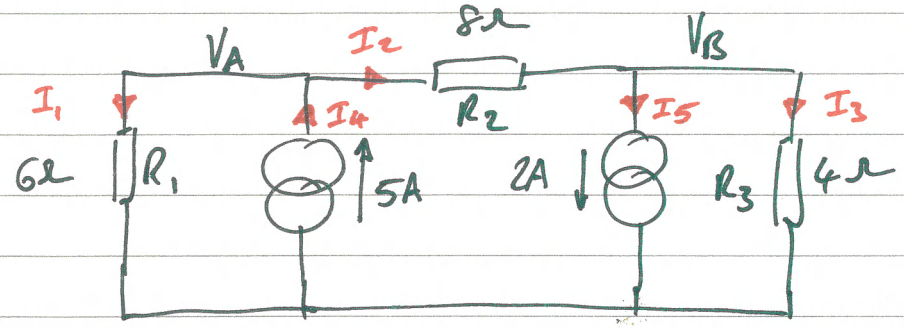
Chapter 4. Circuit Theory Questions

4.1 Loop and Node Analysis

I am stuck on Loop and Node analysis, please help.

Have a look at this PDF which shows hand written solutions with explanation for a reasonably simple example.

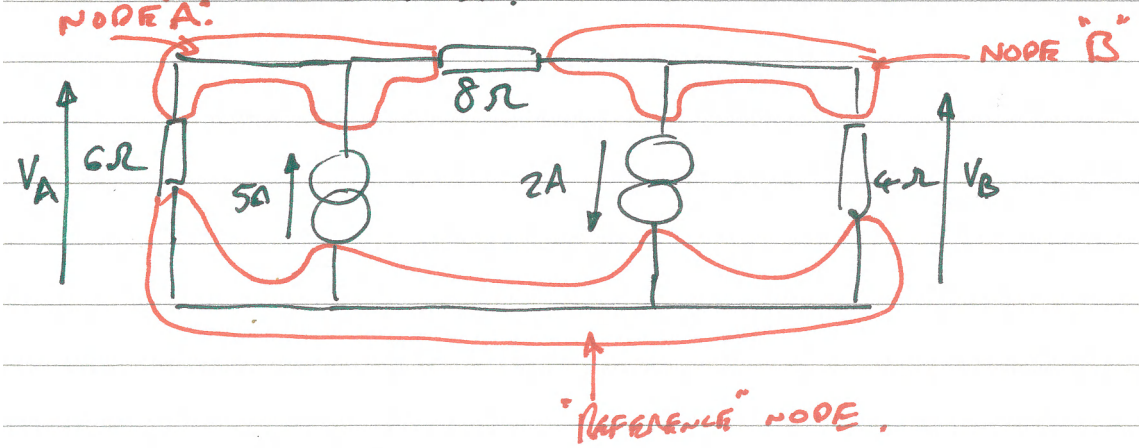
Node Analysis: 1/3



The objective is to use Kirchhoff's Current Law (KCL) at each node to write a self consistent set of equations for the circuit which can be solved for any variable (e.g. voltage, current, power etc.)

Kirchhoff's Current Law says that all currents flowing into and out of a node (a point where components are connected together) must sum to zero.

We label the nodes with voltages with respect to a reference node...



Begin by adding up the currents flowing into and out of "A".

$$5 = I_1 + I_2 \quad (1)$$ (5 is the current of the source I_4)

NOW DO THE SAME FOR "B"

$$I_2 = I_5 + I_3 \quad (2)$$

NOTE THAT ALL CURRENTS THAT "ENTER" i.e. FLOW INTO A NODE ARE ON THE OPPOSITE SIDE OF THE EQUATION TO THOSE CURRENTS WHICH FLOW OUT OF A NODE.

WE CAN INSERT VOLTAGES IN PLACE OF THE CURRENTS BY USING OHM'S LAW.

(1) BECOMES:

$$5 - \frac{V_A}{6} + \frac{V_A - V_B}{8} \quad (3)$$

(2) BECOMES:

$$\frac{V_A - V_B}{8} = 2 + \frac{V_B}{4} \quad (4)$$

THERE ARE A NUMBER OF WAYS TO GO FORWARD INCLUDING SUBSTITUTION, ELIMINATION AND FORMING A MATRIX OF CO-EFFICIENTS. I WILL SUBSTITUTE.

SOLVE (3) FOR V_B:

$$V_B = -40 + \frac{7}{3} \cdot V_A \quad (5)$$

SUBSTITUTE (5) INTO (4) TO REMOVE V_B.

$$-\frac{1}{6}V_A + 5 = -8 + \frac{7}{12}V_A \quad (6)$$

SOLVE (6) FOR V_A

$$V_A = 52/3 = \underline{17.3\dot{3}\ V} \quad (7)$$

THE CURRENT IN R_1:

$$I_1 = \frac{V_A}{R_1} = \frac{17.3\dot{3}}{6} = \underline{2.8\dot{8}\ A} \quad (8)$$

THE VOLTAGE ACCROSS THE 8Ω RESISTOR(R_2).

- FIND V_B : SUBSTITUTE (7) INTO (5)

$$V_B = -40 + \frac{7}{3} \cdot 17.3\dot{3}$$

$$= 4/9\ V$$

ACCROSS THE 8Ω RESISTOR R_2 WE HAVE $V_A - V_B$...

$$V_A - V_B = 17\,1/3 - 4/9 = \underline{16\,8/9\ V}$$

Chapter 5. Diode Questions

Chapter 6. Transistor Questions

6.1 Can we have more EEE225 Questions?

Some of you have asked for more transistor style questions.

For the transistor part of the course, as long as you can:

1. work out the small signal gain, input resistance and output resistance of a differential pair with one input grounded and the other driven.
2. work out the small signal gain, input and output resistance of a Darlington pair connected as common emitter without degeneration.
3. work out the resistance looking into the output of most common current sources and current mirrors.

You will be fine.

But, for those who are curious there is always more to discover. I have neglected to discuss with you an entire class of operational amplifiers called current feedback op-amps. They don't appear on the exam and they're not in the syllabus and there is no need to concern yourself with their existence at all. I don't think they get discussed in the undergraduate degree program or in the MSc program. This is one that you have to teach yourself. For those who go into the engineering profession, teaching yourself is a skill that must be developed. And, if you want to do some more analysis of circuits with several transistors in them, it is a perfect place to go looking as it is relevant to modern analogue IC design.

Question Read and ensure you are confident with the information in: http://www.analog.com/media/en/training-seminars/tutorials/MT-034.pdf

1. Discuss the input resistance of the non-inverting and inverting inputs compared with a voltage feedback op-amp.
2. Compare the compensation schema with that of voltage feedback op-amps. Does the CFA have a gain bandwidth product? Why? (this is hard as it requires a good grasp of some difficult concepts and concepts sometimes take a while to really "sink in").

3. Looking at figure 3 on page 3, what are Q3 and Q4 doing? Why don't they use resistors for this purpose?
4. Would you describe Q1 and Q2 common emitter or common base? If you think about it from the point of view of the non-inverting input and then again from the inverting input does it change your answer?
5. Looking at figure 3 on page 3. Calculate the small signal input resistance looking into both inputs separately.
6. Ignoring the compensation (and any other frequency dependent effects) calculate algebraically (with letters not numbers) the open loop gain (i.e. output voltage / input quantity) of the CFA when the non-inverting input is held at ground and the inverting input is driven by a small signal. This gain will have units of Ohms.
7. Calculate the output resistance.

If you want "help" with this question try "Opamps for Everyone" by Mancinni, http://www.ti.com/ww/cn/uprogram/share/operation_080625.pdf

If anyone makes a serious attempt at the question, I will provide a solution.

I doubt this question can be answered properly in less than 1h30 minutes, by someone who knows where the question is heading. So expect it to take at least a few days perhaps a week or more the first time.

Ultimately I very considerably extended the first problem sheet to provide more than enough questions even for the most voracious appetite. This question didn't make it into the problem sheet however as it is a little outside of the scope of the course.

6.2 Direction of currents in small signal models

From the slide shown in figure 6.1 it says $i_e = i_o + i_b$. However according to the small equivalent, I think it should be $i_e + i_b = i_o$. So why $i_e = i_o + i_b$ is always true?

Also why does the emitter current come into the node which leads to the $i_e + i_b + g_m\, v_{be} = 0$? What I think is that $i_e = i_b + i_c = i_b + g_m\, v_{be}$. Why my thinking is wrong?

Yes, the direction of i_o on the diagram is inconsistent with the equation in the text. A minus sign is missing. I have added it to my book of errors.

The emitter current direction depends on how you choose to define it. There is nothing wrong in what you have said but you do have an inconsistency between

your equations (a minus sign is missing). The emitter node is at the top of R_S in the diagram. Both the base and collector signal currents flow into and out of the emitter of the transistor, but I have drawn the emitter current flowing into the transistor and the base current also flowing into the transistor. This cannot be physically true, when the emitter current is flowing into the transistor, the base current will be flowing out. It does not matter however. As long as I write out my node or loop equations properly, the algebra will provide a minus sign in the appropriate place to denote that either the base or emitter current will be in the opposite direction to the way I defined it.

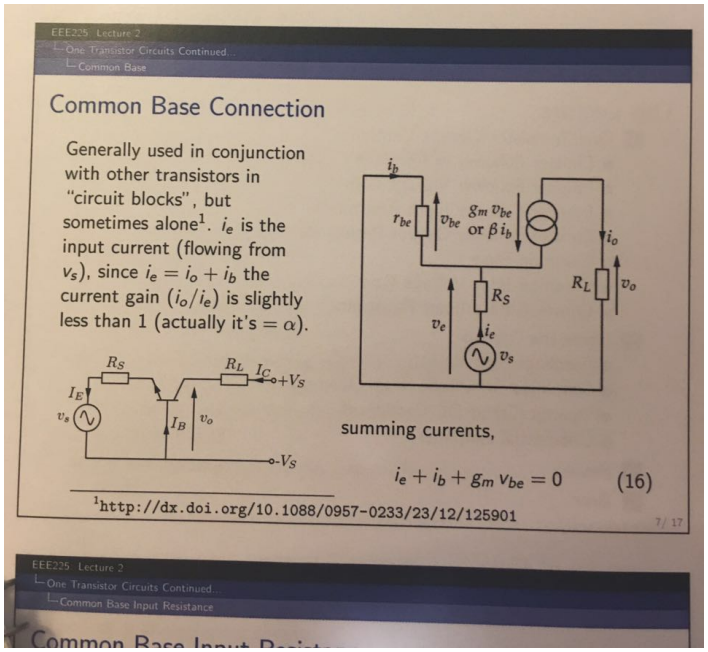


Figure 6.1: Common Base small signal model.

6.3 Reduction of Differential Amplifier Small Signal Model

Figure 6.2 shows the small equivalent circuit of the differential amplifier. My question is how the red pen circled part equal a resistor, $r_{e2} = \frac{1}{g_{m2}}$.

Also, for T2, if a transistor's base is connected to the ground, can it always be said to be a common base transistor?

This question is answered in the video solutions to Q6 of problem sheet 1 which can be found on YouTube https://youtu.be/rs9mVtP7pDs. The solution is also derived in a handout attached to the back of one of the sets of lecture notes.

Yes. "Common" is another word for ground which is also sometimes called "earth". The ground on the base only needs to exist for the AC conditions the

DC potential can be different from ground in order to bias the transistor thereby setting up the appropriate quiescent currents. An example of this is C_7 in **??**.

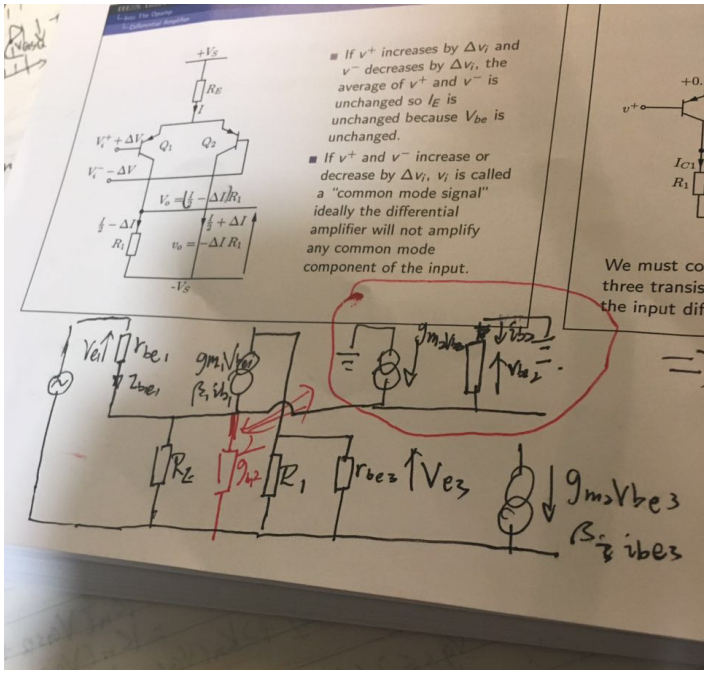


Figure 6.2: Differential pair small signal model.

6.4 Reduction of Differential Amplifier Small Signal Model II

For figure 6.2, why the voltage across V_E is V_{e1}? Is it because that the only voltage supplied in this case is on the T1?

Also, when calculating the gain in this case, do we assume that T1 and T2 are identical which means that $r_{e1} = r_{e2}$.

I can't see V_E on your diagram, so I can't answer the question. V_{e1} is just my name for the voltage between the emitter of transistor number 1 and the ground. Hence V (voltage) e (emitter) 1 (transistor number one).

Do you mean $r_{be1} = r_{be2}$ or $r_{e1} = r_{e2}$. I ask because r_{e1} has not been discussed in any of the lectures when considering the differential amplifier. Both equations are true, although I'm not sure how either will help...

6.5 Differential Pair DC Conditions

In figure 6.3, what means the quiescent current in T1 and T2 are nearly identical? Aren't they both equal to $I_E/2$? Why they are not identical before adding the current mirror?

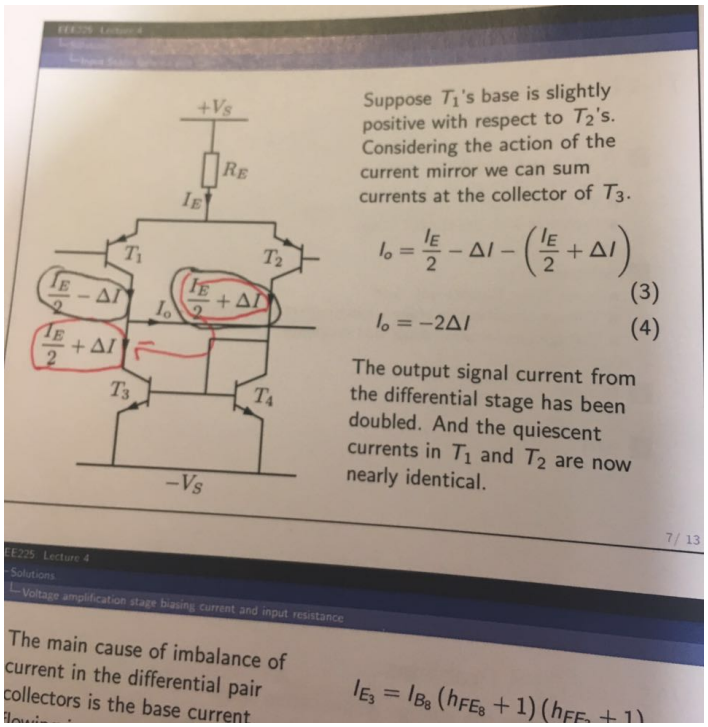


Figure 6.3: Differential pair DC conditions.

In an ideal situation they are equal and both equal to $I_E/2$. This is only true if the saturation current and the temperature of both transistors are identical. This is not true even in an integrated circuit where the transistors are closely matched. Nevertheless they are not identical.

What is the imbalance of the current in differential pair?

It is the different in current flowing out of each the collector of the differential pair. Surely the name is self-explanatory?! This imbalance exists due to the differences in the saturation current and temperature mentioned above.

Is it the emitter current difference of T1 and T2?

Collector. But there is a difference in the emitter current too and this is the sum of the collector current and base current.

Also, why is it influenced by the base current of VAS?

The VAS transistor, usually configured as a non-degenerated common emitter amplifier, must have some base current to be in the forward active region and it needs to be in the forward active region to provide amplification. The base current must be supplied by one collector of the differential pair, but not the other hence it is likely to add some imbalance between the collector currents in the differential pair.

6.6 Impedance Transformation in Transistor Stages

In figure 6.4, why should there be a current source? And also, why does T9 make the input resistance of OPS larger than if T9 and I_{T9} were not used. Why does it make the output resistance smaller than if T9 and I_{T9} were not used?

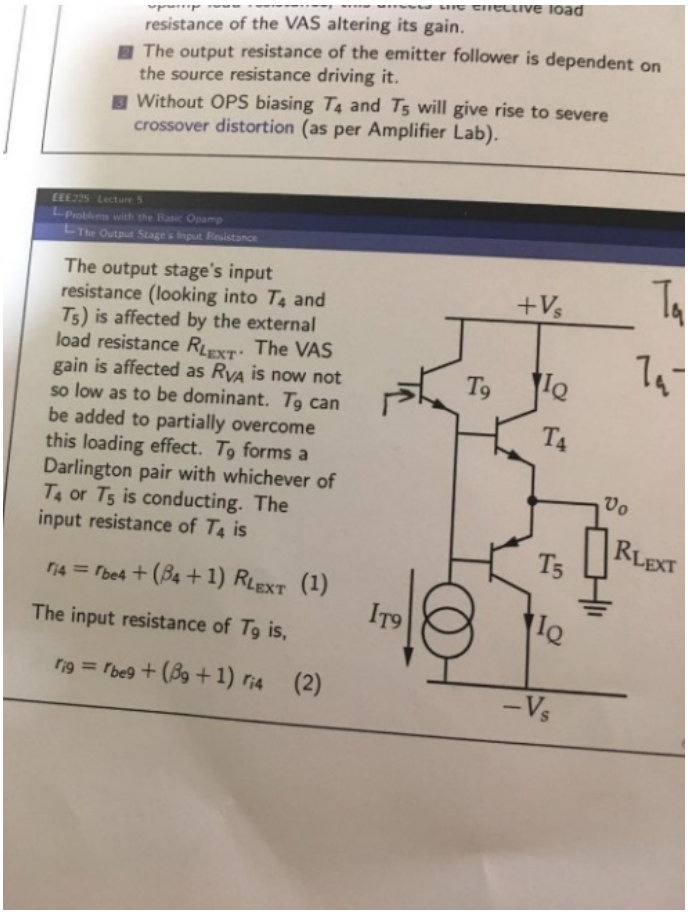


Figure 6.4: Push-Pull Output stage and Class A driver.

The current source is not necessary but there has to be some load for the emitter follower formed by T9. The current source is probably an improvement over just using a resistor load – it depends on how the circuit is designed, a badly designed current source could be worse than an optimally chosen resistor, but in general the current source will be better in almost all respects. A well designed current source allows T5 to switch on faster and T4 to switch off faster while maintaining lower noise and lower power dissipation in T9 and in the current source. It also permits lower distortion in the emitter follower stage for an equivalent level of performance compared to a resistor load. You will need to do some serious thinking to convince yourself of these statements.

T9 performs (as all transistors do) an impedance transformation on signals entering and leaving its base/emitter/collector. In one half cycle of the output waveform T9 and T4 form a Darlington and in the other half cycle T9 and T5 form a Darlington like structure. If you can derive the input resistance and output resistance of a Darlington pair you should, with some thought, be able to deduce the underlying nature and usefulness of the transformation. The input resistance is derived in a handout in the course book (between lectures 3 and 4, I think). These derivations are also questions on problem sheet 1, question 4, parts 5 and 6.

The output resistance of this stage does not reduce as a result of using T9 and I_{T9} – all else being equal. I hope that I have not said this in the lecture notes anywhere. The magnitude of the impedance transformation is increased by the use of T9 and I_{T9}. This means that the output stage as a whole can drive a given load resistance while itself being driven by a source with a much higher source resistance than would be possible if T9 and I_{T9} were not included. We can observe the effect of including T9 and I_{T9} by four example circuits shown in figure 6.5.

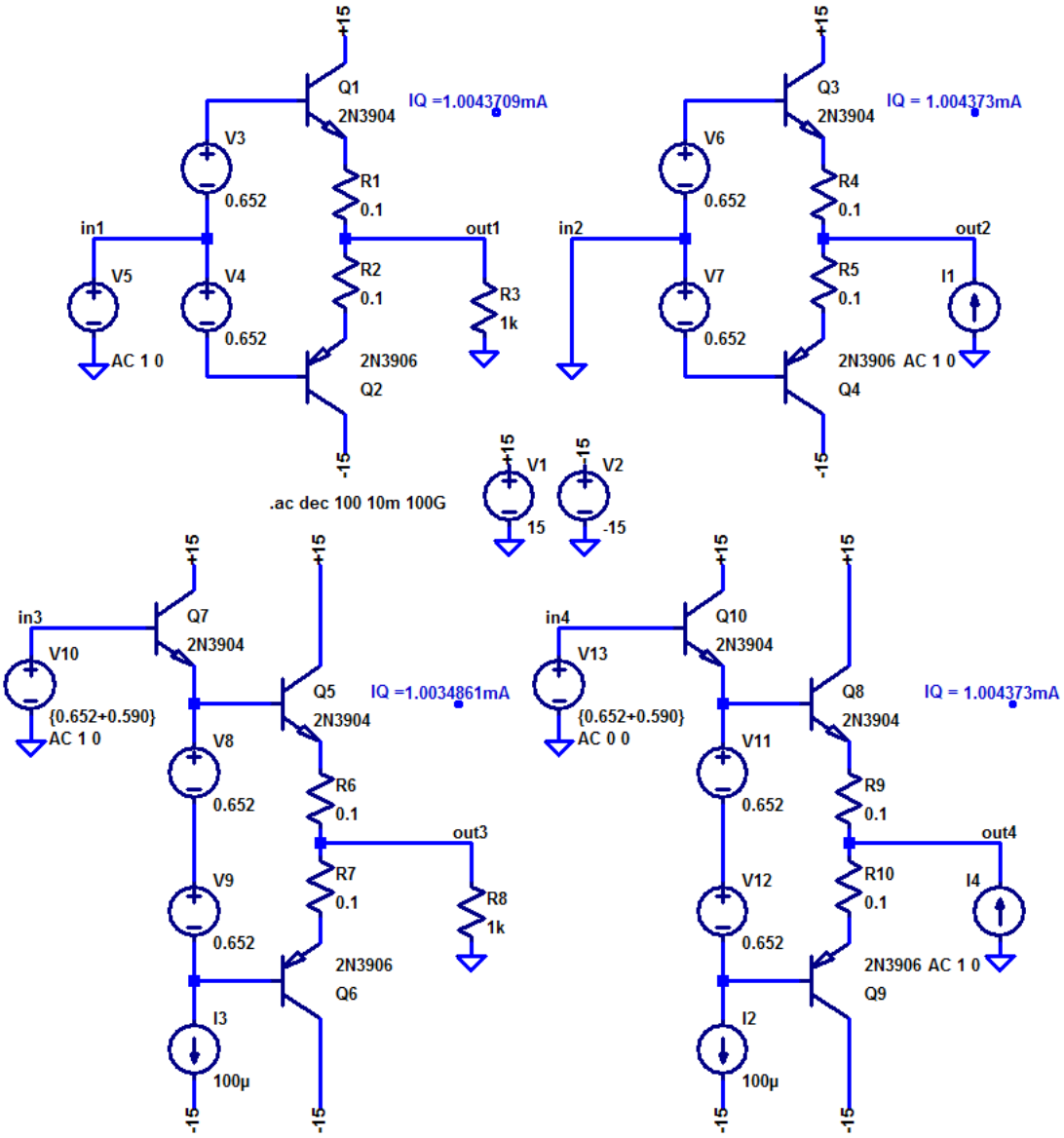


Figure 6.5: Top Left: Standard push pull stage biased to approximately 1 mA quiescent current and using 0.1 Ω emitter degeneration resistors, set up to find the input resistance while the load is 1 kΩ. Top Right: Standard push pull stage biased to approximately 1 mA quiescent current and using 0.1 Ω emitter degeneration resistors, set up to find the output resistance while the source resistance is 0 Ω. Bottom Left: Standard push pull stage biased with 1 mA quiescent current and using 0.1 Ω emitter degeneration resistors driven by a class A emitter follower stage loaded by an ideal current source, set up to find the input resistance. Bottom Right: Standard push pull stage biased with 1 mA quiescent current and using 0.1 Ω emitter degeneration resistors driven by a class A emitter follower stage loaded by an ideal current source, set up to find the output resistance.

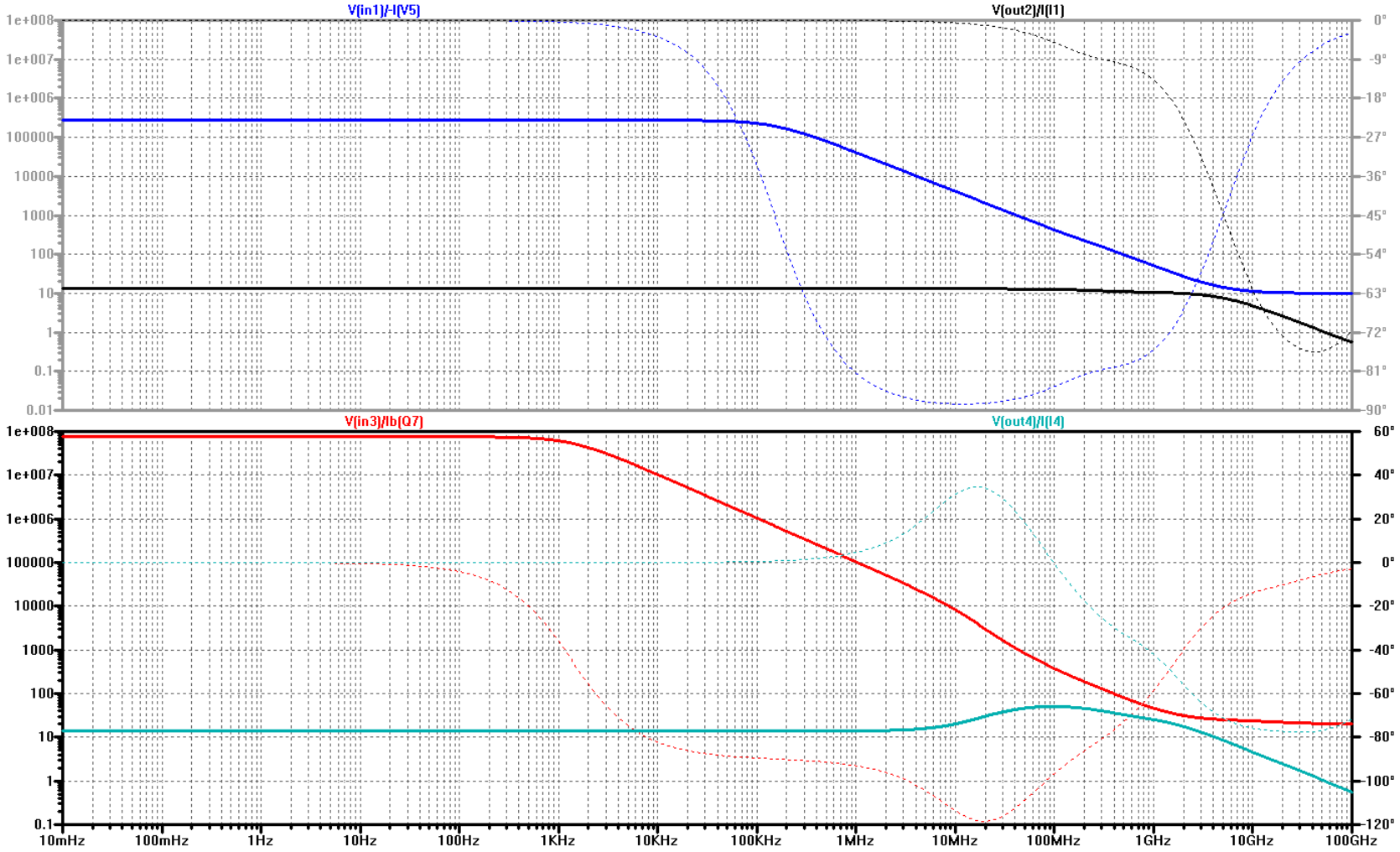


Figure 6.6: Top: Input (blue) and output (black) resistance of a standard push pull stage biased with 1 mA quiescent current and using 0.1 Ω emitter degeneration resistors. Bottom: Input (red) and output (cyan) resistance of a standard push pull stage biased with 1 mA quiescent current and using 0.1 Ω emitter degeneration resistors driven by a class A emitter follower stage loaded by an ideal current source. Note the input resistance in the bottom sub-figure is approximately 2.5 orders of magnitude greater.

Comparing input resistances, blue the upper sub-figure of figure 6.6 and red in the lower sub-figure, the input resistance is increased by the use of T9 and I_{T9} by approximately 2.5 orders of magnitude. The output resistance is very similar in the mid-band at slightly more than 10 Ω. So T9 increases the input resistance and in this case high input resistance is desirable.

The forgoing discussion does not fully illuminate the whole picture, however. We could, if we did some algebra rather than using simulated examples show that in the T9, I_{T9} case the 1 kΩ load resistor is made to look like approximately 1×10^8 Ω from the perspective of a signal looking into the base of T9. If we included a source resistance with V5 or V10 in figure 6.5 we could also see the effect that the source resistance has on the output resistance of the stage.

To considering the effect the source resistance has on the output resistance we can select a range of source resistances and simulate to find the resulting output resistance numerically. This is shown in figure 6.7 and the result is shown in figure 6.8. In the mid band (below approximately 10 kHz) the output resistance increases dramatically as the source impedance increases.

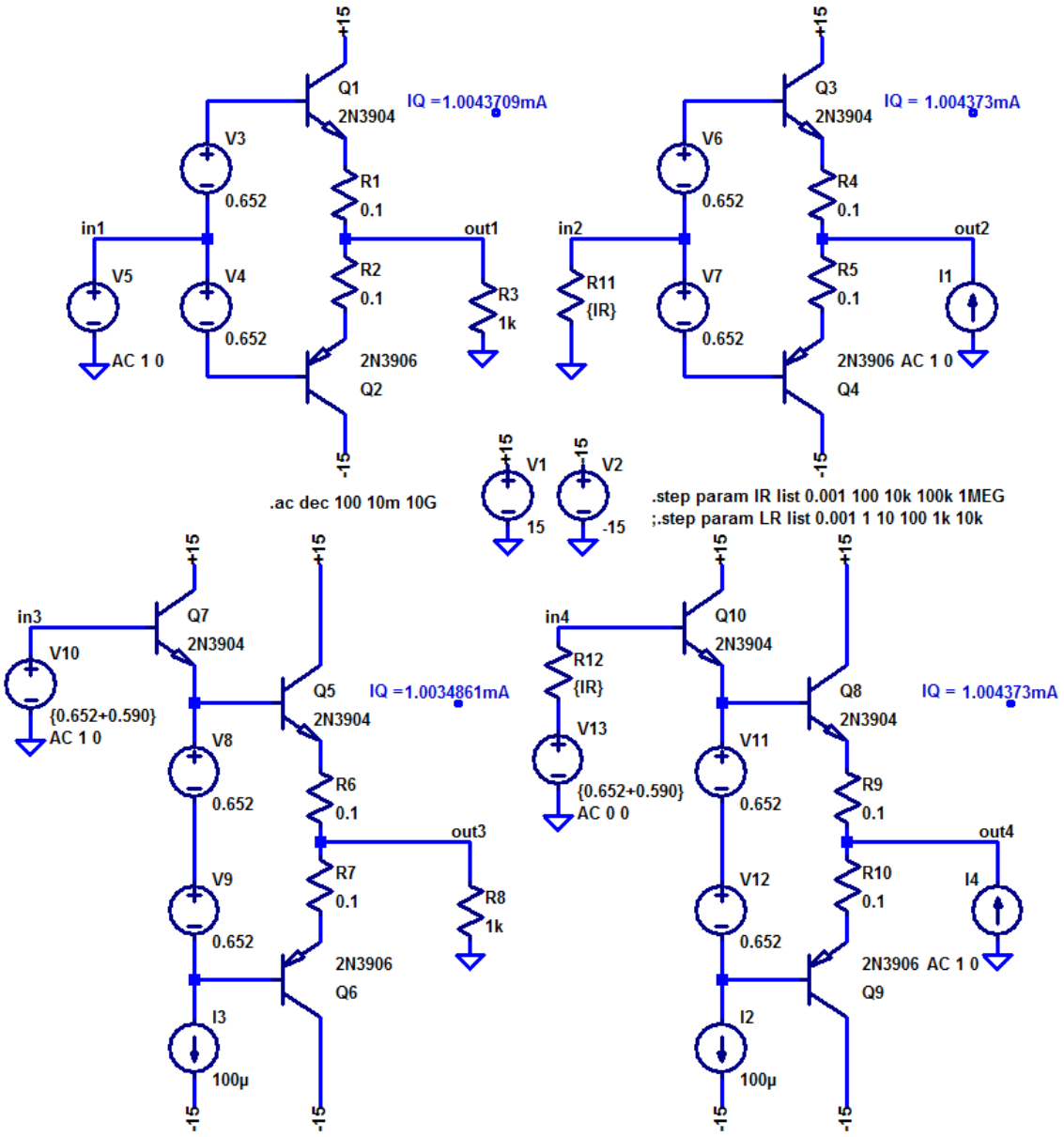


Figure 6.7: Simulations on the two push pull stages designed to expose the effects of source resistance on output impedance and load resistance on and input impedance. Note that R_{11} and R_{12} are selected from the .step command.

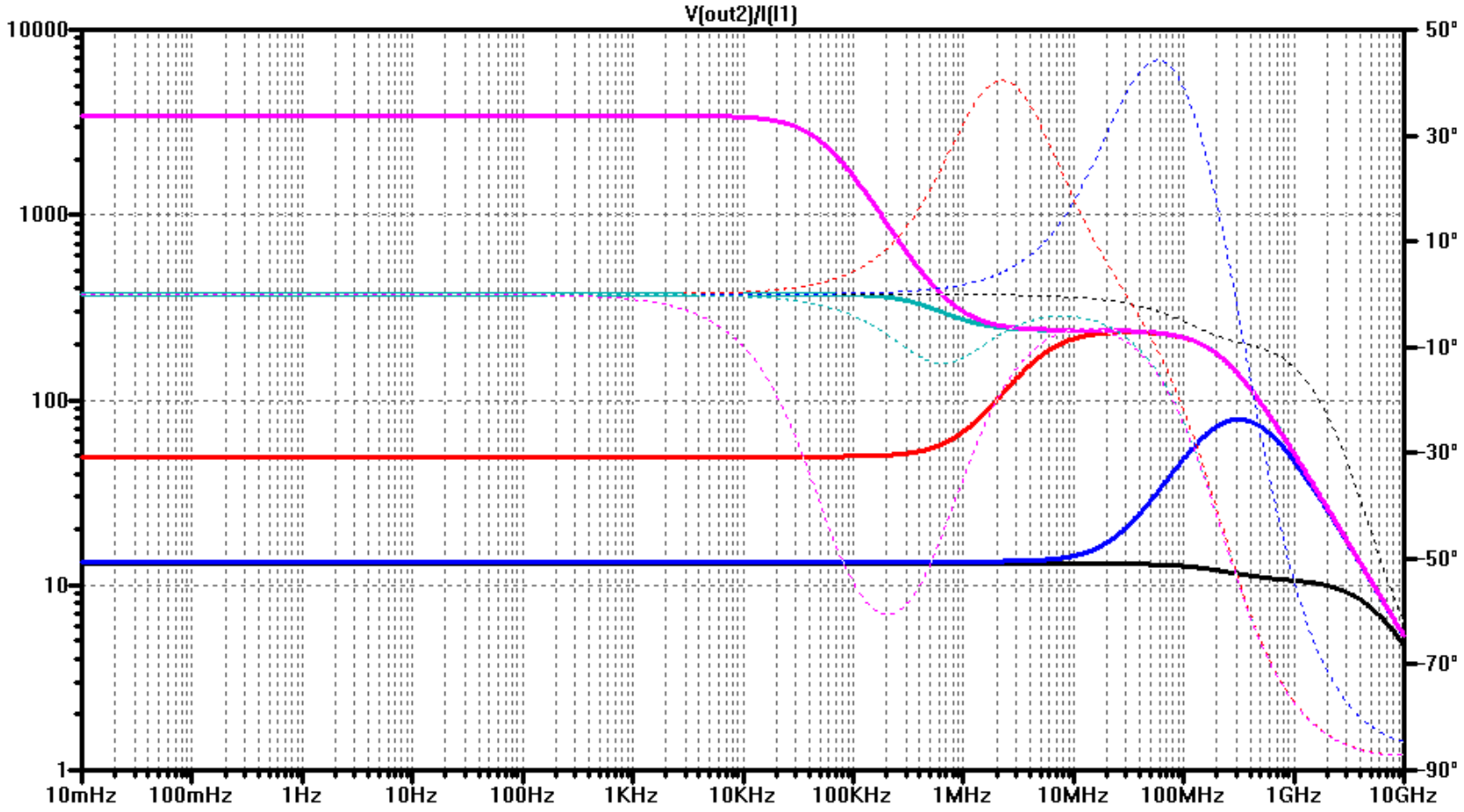


Figure 6.8: Output impedance resulting from a set of source resistances. Black = 1 m , Blue = 100, Red = 10 k, Cyan = 100 k, Magenta = 1 MΩ.

Similarly the effect on input impedance of changing load resistance is expressed by numerical example in figure 6.9 with results shown in figure 6.10. The input impedance increases as the load resistance increases. Of course we are not in control of the load resistance in op-amp design situations. It depends on the user of the IC, not the designer. The objective of the analysis is to show that the source and load resistances and input and output impedances are interrelated. The relationships can be derived by small signal models and linear algebra. This idea of impedance transformation (both in magnitude and phase) is fundamental to the operation of the transistor when considering signals. The first problem sheet, especially question 4 is concerned with this kind of work. We can describe amplifiers and oscillators as operating as impedance transformers.

The fleet of mind will note that the graph in figure 6.8, and some of the other graphs has units of Ohms and there is a magnitude and phase shift component to the solution. It is a small leap, but a leap none the less, to realise that a resistance with phase shift is simply partly resistive and partly either capacitive or inductive, depending on the sign of the phase. This may become clearer if one considers the Argand diagram. Resistances lay on the real positive axis, inductive and resistive parts lay above the horizontal axis and pure inductances are 90° out of phase with resistive components on the positive imaginary axis. Similarly capacitive resistive components lay below the horizontal with purely capacitive elements laying on the negative imaginary axis. I have spoken about source and load resistances because I have used real resistors (no imaginary parts) but it does not follow that the impedance looking into the input and output of the amplifier stage will be purely resistive, hence I have said impedance. In real design situations, especially when one amplifier stage drives another amplifier stage the source and load resistances are in fact impedances as well. These ideas are beyond the scope of EEE225, but it cannot hurt to know they exist.

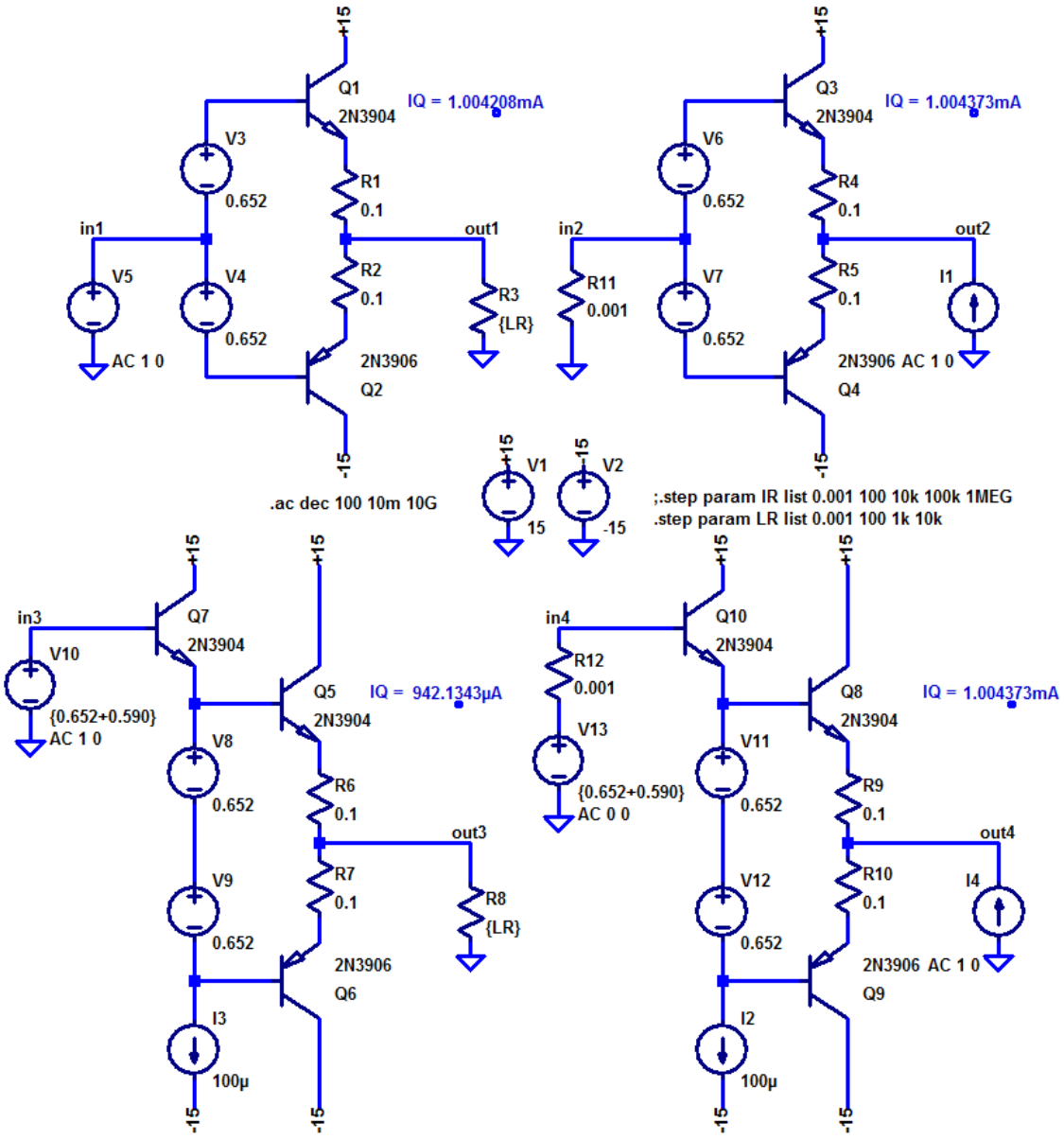


Figure 6.9: Numerical simulation for the effect of load resistance on input impedance of a push pull stage.

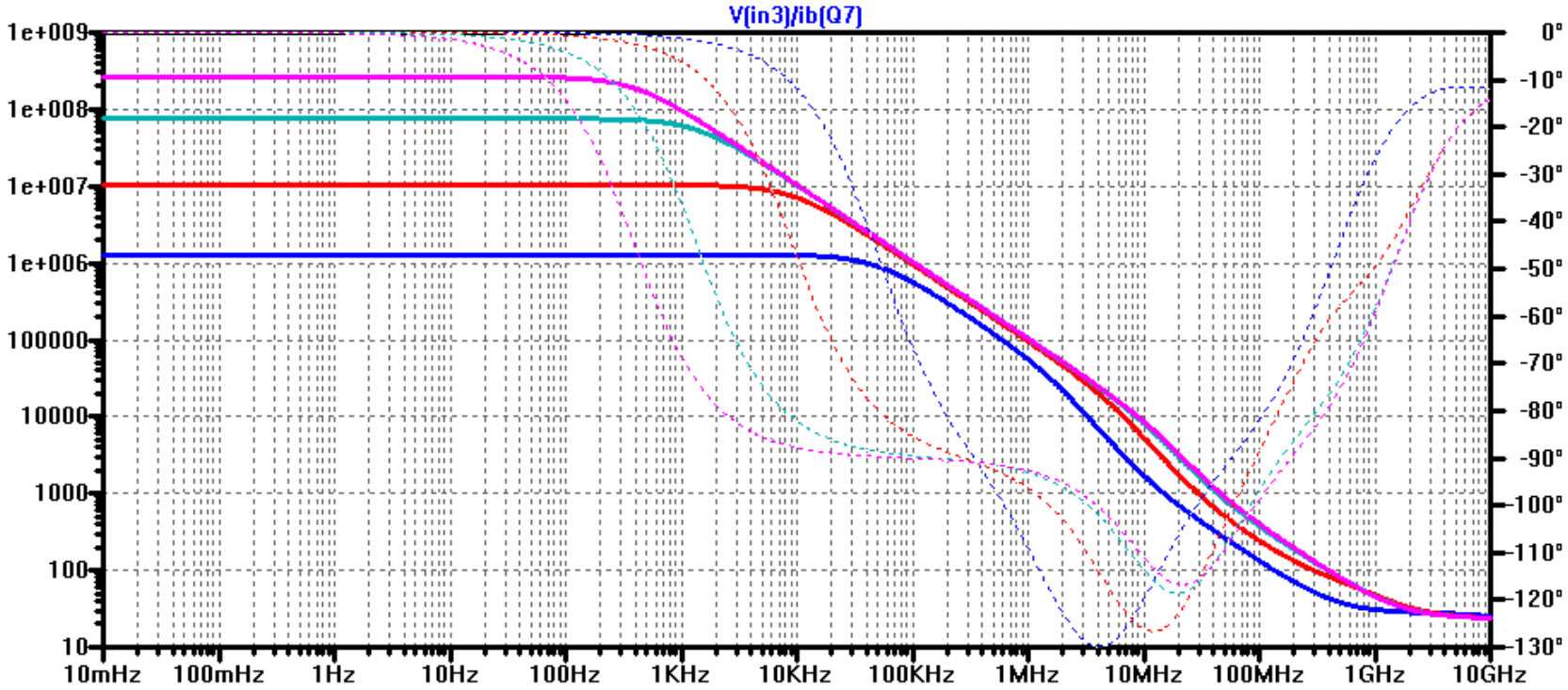
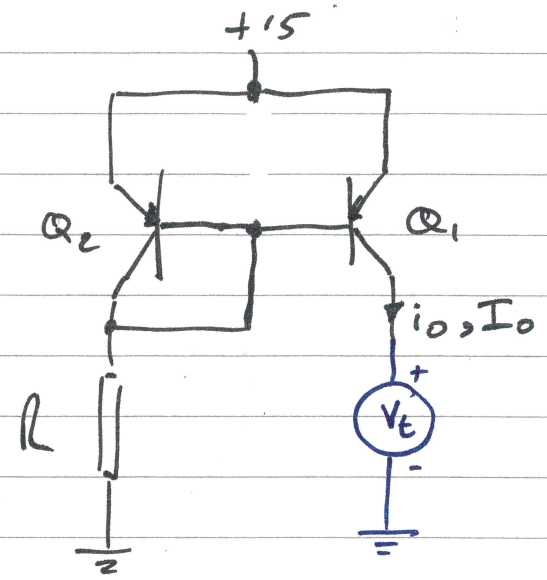


Figure 6.10: Input impedance resulting from a set of load resistances. Blue = 1 m, Red = 100, Cyan = 1 k, Magenta = 10 kΩ.

6.7 Current Mirror Output Resistance I

Someone has asked a question from the back of "Millman and Grabel" – a veritable gold mine of questions covering the first two thirds of the course.

The solution to this question turns out to be quite simple, in the end. If you want something a bit harder consider the same question but degenerate the emitters of both Q_1 and Q_2, then see how the output resistance of the mirror is affected. In the more complicated case try to get your answer in the form $r_{out} = r_{ce_1} \cdot$ ([stuff and things to do with β and resistors]) as this will make clear the effects of the degeneration (negative feedback) compared to the non-degenerated version.



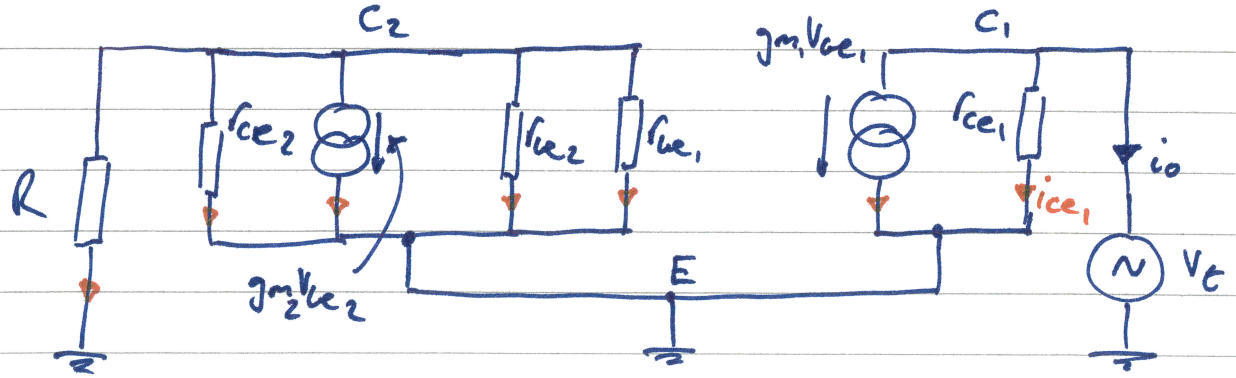
$\beta_o = 50$, $\beta_F = 50$, $V_A = 50$, $I_o = 100\mu$

- FIND THE OUTPUT RESISTANCE ...

- DRIVE A TEST SIGNAL V_t INTO THE OUTPUT. SEE WHAT i_o AND V_t RESULT.
- USE OHM'S LAW $R_o = V_t / i_o$ ...

- THIS QUESTION IS FROM PP 950 OF "MICROELECTRONICS" BY JACOB MILLMAN & ARVIN GRABEL, 2nd ED. CHAPTER 14 14-1 PART 6.
- THERE ARE LOTS OF APPROACHES. LET'S IMAGINE YOU MAKE NO ASSUMPTIONS...
  - NOTE I KNOW r_{ce} WILL BE IMPORTANT! IF YOU DON'T, YOU'LL BE ABLE TO SHOW THAT $r_o = \infty$ ...

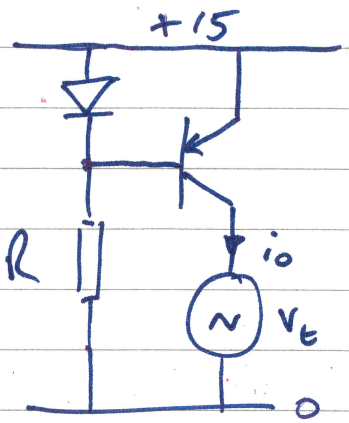
- A SMALL SIGNAL MODEL...



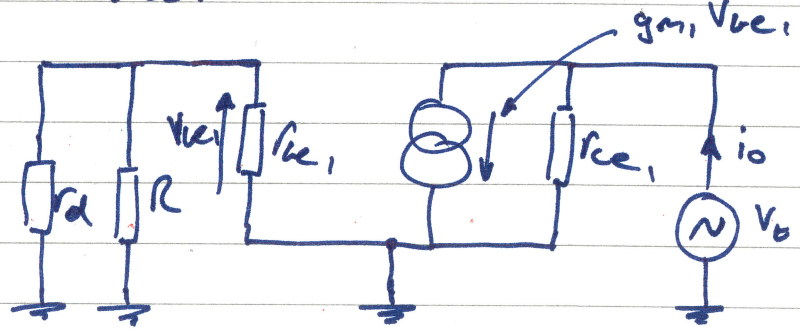
- WHAT A HORRID THING!

- LOOK AT Q_2 IN THE QUESTION. IS IT A TRANSISTOR OR A DIODE? C AND B ARE CONNECTED...
  - IT IS A TRANSISTOR CONNECTED AS A DIODE.

SO:



WE CAN USE THIS SIMPLIFICATION TO DRAW A SIMPLER SMALL SIGNAL MODEL.



BUT... LETS IMAGINE I DIDNT SEE THAT SIMPLIFICATION USE NODE ANALASYS ON THE FULL MODEL.

AT C_1 :
$$i_o = g_{m_1}(V_{c_2} - 0) + \frac{V_{c_1} - 0}{r_{ce_1}} \quad (1)$$

AT C_2 :
$$\frac{V_{c_2} - 0}{R} + \frac{V_{c_2} - 0}{r_{ce_2}} + g_{m_2}(V_{c_2} - 0) + \frac{V_{c_2} - 0}{r_{be_2}}$$

$$+ \frac{V_{c_2} - 0}{r_{be_1}} = 0 \quad (2)$$

WE NEED ONE MORE EQUATION.

$$V_t = \underbrace{\frac{V_{c_1} - 0}{r_{ce_1}}}_{i_{ce_1}} \cdot r_{ce_1} \quad (3)$$

$g_{m_1} V_{be_1}$ DOES NOT COME INTO THIS EQUATION. IT DOES NOT CARE WHAT VOLTAGE WE PUT ACCROSS IT, IT WILL

ONLY ADMIT A CURRENT OF $g_{m_1} V_{be_1}$, NO MORE, NO LESS.

- LOOKING AT (3) WE CAN SEE THAT $V_t = V_{c_1}$. (4)
- SUBSTITUTING (4) → (1):

$$i_o = g_{m_1} V_{c_2} + \frac{V_t}{r_{ce_1}} \quad (5)$$

- GET (2) IN TERMS OF V_{c_2} IN HOPE OF SUBSTITUTING INTO (5)...

$$V_{c_2} = 0 \; ! \quad (6)$$

- (6) → (5)

$$i_o = \frac{V_t}{r_{ce_1}} \quad \text{AND} \quad R_o = V_t / i_o \quad \therefore \; \underline{\underline{R_o = r_{ce_1}}}$$

I DID THAT TO PROOVE IT. I HOPE, WITH PRACTICE YOU CAN SEE BY LOOKING. THE HARD PART IS TO REALISE THAT r_{ce} IS IMPORTANT. IF IT IS LEFT OUT, THE QUESTION CAN BE VERY CONFUSING!!

SO WHAT IS THE VALUE OF r_{ce}?

- TRY PAGE 394 – 396 IN MILLMAN, 2nd Ed.
- YOU'LL NEED TO HAVE ANSWERED PART A OF THIS QUESTION IN WHICH YOU FIND THAT THE MIRROR IS SOURCING 100 μA TO ITS LOAD AND Q_1 & Q_2 HAVE AN EARLY VOLTAGE OF 50 V.

6.8 How does a Phase Splitter work?

An explanation from an analogue point of view is below, phase splitters find used in digital systems as well. Of course there is no analogue and digital really it's all the same. It's just a question of how one chooses to think about it. What follows is quite a common method I use for checking something when I don't want to do too much algebra by hand. The diagram is hand drawn and the equations written using any/all of KVL, KCL, Ohm's law, and the principle of superposition as appropriate. The rest of the algebra is done in Maple (but Mathcad, Mathmatica etc. are also capable programs). There are some benefits and dangers with symbolic computational systems:

1. They're not very intelligent. They use rules to combine and simplify expressions and they don't make any assumptions (e.g. f is real and positive) unless you explain it to them. They are not very good at factorising and getting a standard form, like the first or second order LTI system standard forms where numerator and denominator are a polynomial in s with unity in the s^0 term. It's like pulling teeth.

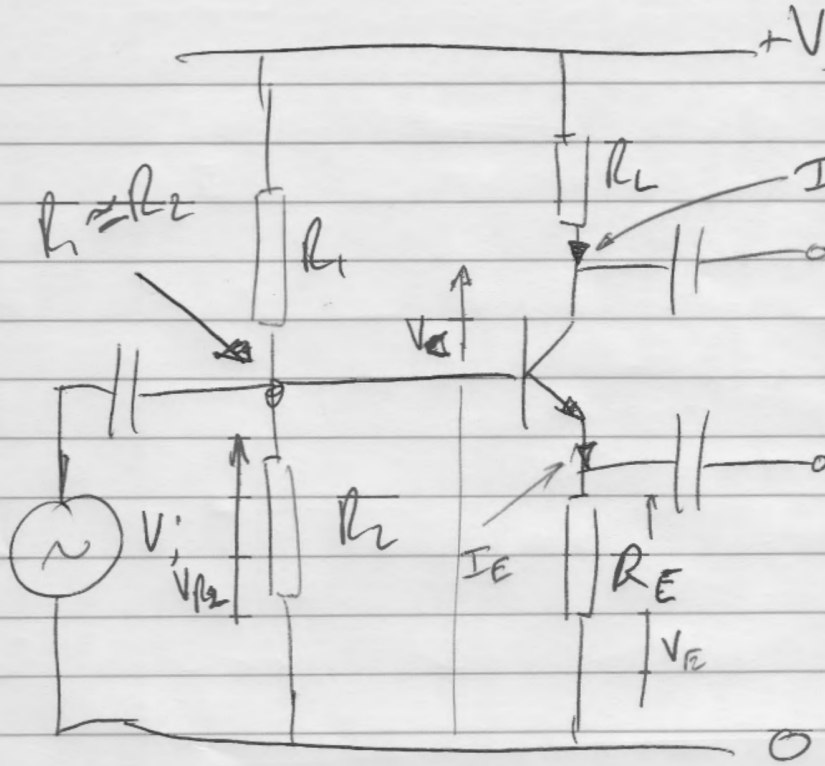
2. Just like numerical computational systems (Matlab, SPICE, Finite Element programs (Ansys, COMSOL etc.)) if one doesn't think carefully about what one is asking the computer to calculate it will duly spit out nonsense. The user must be wary of taking whatever comes out at face value without any critical thought.

3. No mistakes. If one analyses the circuit correctly to obtain the correct equations, having drawn the correct model etc. the answer that comes out of the computer will have no algebraic errors (the computer obeys the laws of mathematics). Often I make mistakes (some might argue that if I did more by hand, I'd make less mistakes!).

4. They're fast. Much faster than by hand. Often, if I have no need to report the method, for example in research where a particular derivation is required but I presume anyone who might need it can derive it themselves, I will probably use Maple to do my algebra. If I have need of the method, for example for problem sheet solutions, I will do it by hand so that I have a more elegant method and a proper factorisation. Students will be doing the problems by hand in the exam so the solutions provided should also be done by hand.

In this case I couldn't be bothered to do it by hand as the phase splitter is not in EEE225... the result is that this stands firstly as a solution to a common emitter amplifier with 100% feedback (which is effectively what this kind of phase splitter is) and secondly it stands as an example of a method I sometimes use but which most candidates will not be aware of.

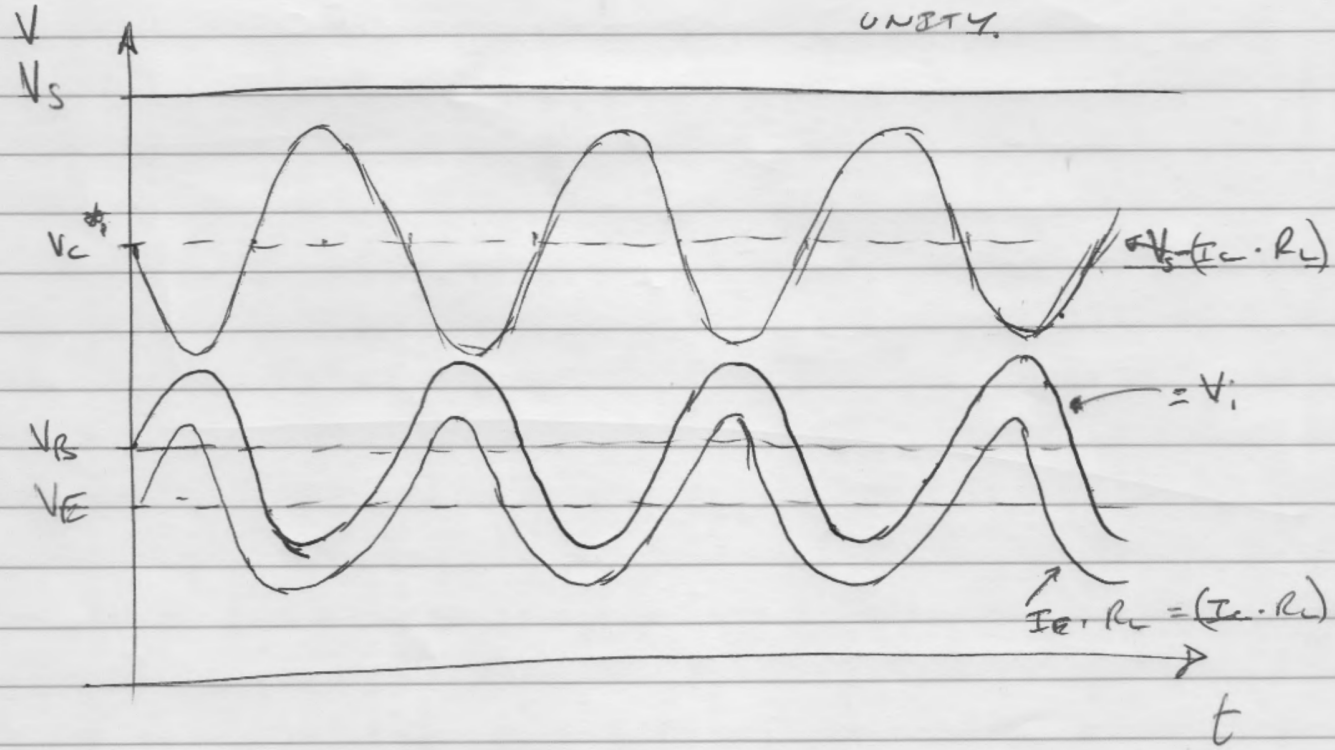
Phase splitters were commonly used in valve audio amplifiers to drive the two "n-channel" valves. Valves are only electron devices, there is no valve in which holes are emitted from the anode and travel from the anode to the cathode. This is of course because holes are a fiction developed to make explanation of phenomena in crystals easier and valves are devices not formed with crystals. Having only "n-channel devices, and requiring a push pull output stage, we can make a phase splitter to invert the signal to one of the output devices thereby getting one to "push" current while the other "pulls" current through the load. This can be seen in the "Williamson" amplifier shown in figures 6.11 and 6.12, a famous 4 stage amplifier whose number of stages risks stability problems (due to the accumulation of phase shift in the open loop). The effective use of negative feedback was quite limited because of this. The push pull output stage is V5 and V6. V3 and V4 are a push pull voltage amplifier/driver stage, V2 is the phase splitter in which R7 is the collector load and R5 is the emitter load. R6 and C2 form a very crude (but very widely used power supply voltage drop from the 450 V used in the OPS and VA/driver to the lower supply voltage needed for the push pull, similar arguments for R2 and the V1 stage which is a valve version of a "Type 1" common cathode (common emitter) amplifier with degeneration. Global negative feedback is taken from the secondary of the output transformer to the cathode of the input stage. The output transformer is necessary because the LF valves (generally called "receiver valves" to separate them from "transmitter valves" and "industrial valves") tended to run at several hundred volts and perhaps 0.5 – 400 mA. A loudspeaker from this period would have been perhaps 8 – 16 Ω possibly 32 or 64Ω. Since it's the number of turns and the current that determines the MMF, some transformation is needed from mA and kV to A and V. Lower power amplifiers were needed than in modern times because output power was costly to obtain, therefore speakers were made more efficient (but higher distortion) in order to get a loud sound from a modest power amplifier. In modern times output power is inexpensive 5 kW is perhaps not easily obtained but it certainly can be obtained. Therefore speakers are made to have lower distortion but also lower sensitivity (dB / W @ 1 m). This is done mostly by limiting the x-max (distance the cone travels back and forward, thereby maintaining uniform magnetic flux density cutting the whole of the voice-coil winding and in-so-doing avoiding one of the main distortion mechanisms. The compliance of the surround and spider are also more liable to obey Hook's law if the displacement is small which is another distortion mechanism. Books on audio and valves are listed in section 11.2.



$I_C = I_E$

$R_L = R_E$

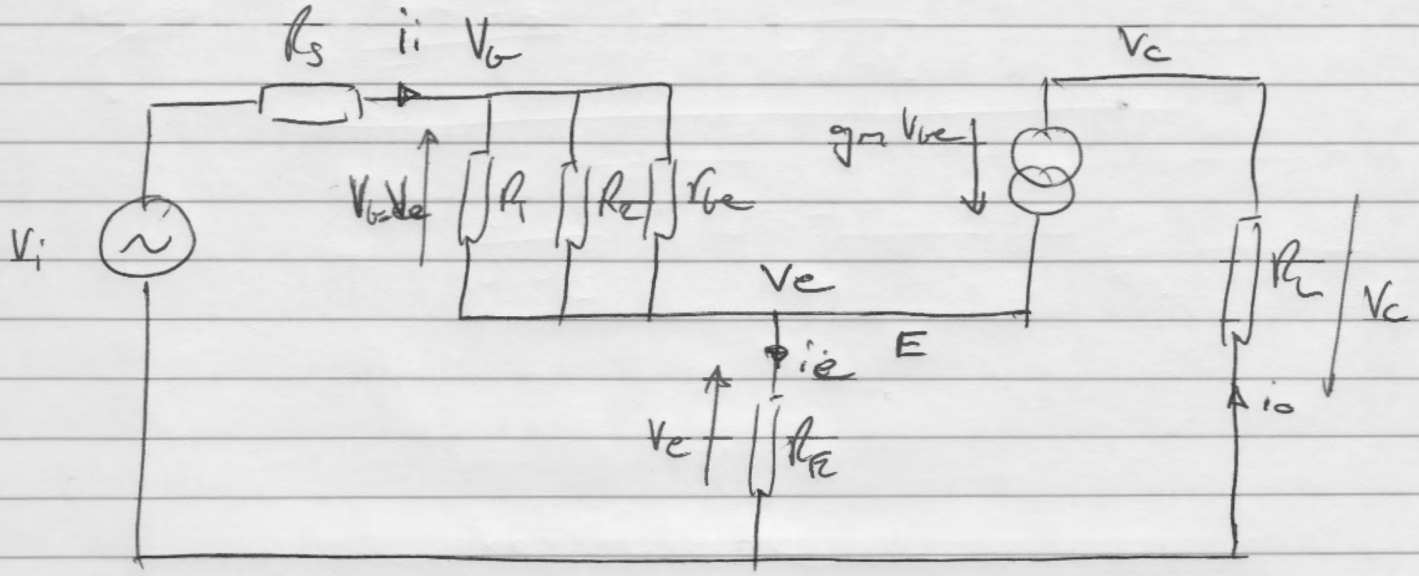
THE NEGATIVE FEEDBACK IN THIS CIRCUIT IS HIGHLY EFFECTIVE IT IS ARRANGED TO GIVE A GAIN VERY CLOSE TO UNITY.



*1 DON'T FORGET AS V_{BE} ↑, I_C ↑ AND V_C ↓ BECAUSE $V_C = V_S - (I_C \cdot R_L)$ . . .

IF $R_L \cong R_E$ GAIN ~ 1. ∴ $V_C \simeq V_E$ BUT IN ANTI-PHASE HENCE PHASE SPLITTER.

PHASE SPLITTER WITH SMALL SIGNALS



$$R_1 // R_2 // r_{be} = Z_b$$

@ E

$$i_e = i_i + g_m(V_b - V_e)$$

$$\frac{V_c}{R_c} = \frac{V_b - V_e}{Z_b} + g_m(V_b - V_e)$$

@ B $\quad i_i = i_1$

$$\frac{V_i - V_b}{R_s} = \frac{V_b - V_e}{Z_b}$$

@ C $\quad i_o = g_m(V_b - V_e)$

$$\frac{0 - V_c}{R_L} = g_m(V_b - V_e)$$

restart :

Some calculations to illuminate the phase splitter

Some node equations (sum currents at the emitter):

$$EQ1 := \frac{ve}{RE} = gm\cdot(vb - ve) + \frac{vb - ve}{zb}$$

$$\frac{ve}{RE} = gm\,(vb - ve) + \frac{vb - ve}{zb} \quad \textbf{(1)}$$

Sum currents at the base:

$$EQ2 := \frac{vi - vb}{Rs} = \frac{vb - ve}{zb}$$

$$\frac{vi - vb}{Rs} = \frac{vb - ve}{zb} \quad \textbf{(2)}$$

Sum currents (and multiply by RL...) at the collector

$$EQ3 := vc = -gm\cdot(vb - ve)\cdot RL$$

$$vc = -gm\,(vb - ve)\,RL \quad \textbf{(3)}$$

Ultimatley we want the magnitude of the output signal from the emitter = the magnitude of the output signal from the collector but in anti-phase so lets see what we have to do to RL and RE to make this happen. We hypothesise RL and RE will be the main factors because we know how a common emitter amplifier *with* degeneration works (it was covered in EEE118 lectures 13 - 15) and at the start of EEE225 (very briefly).

$$EQ4 := isolate(EQ2, vb)$$

$$vb = \frac{zb\,vi + Rs\,ve}{zb + Rs} \quad \textbf{(4)}$$

$$EQ5 := subs(EQ4, EQ1)$$

$$\frac{ve}{RE} = gm\left(\frac{zb\,vi + Rs\,ve}{zb + Rs} - ve\right) + \frac{\frac{zb\,vi + Rs\,ve}{zb + Rs} - ve}{zb} \quad \textbf{(5)}$$

$$EQ6 := isolate(EQ5, ve)$$

$$ve = \frac{gm\,zb\,RE\,vi + RE\,vi}{zb + Rs + gm\,zb\,RE + RE} \quad \textbf{(6)}$$

$$EQ7 := \frac{lhs(EQ6)}{vi} = \frac{rhs(EQ6)}{vi}$$

$$\frac{ve}{vi} = \frac{gm\,zb\,RE\,vi + RE\,vi}{(zb + Rs + gm\,zb\,RE + RE)\,vi} \quad \textbf{(7)}$$

$$EQ8 := lhs(EQ7) = simplify(rhs(EQ7))$$

$$\frac{ve}{vi} = \frac{RE\,(gm\,zb + 1)}{zb + Rs + gm\,zb\,RE + RE} \quad \textbf{(8)}$$

So we have the size of the output at the emitter with respect to the input. What about the output at the collector?

$$EQ9 := isolate(EQ1, ve)$$

$$ve = \frac{gm\ zb\ RE\ vb + RE\ vb}{zb + gm\ zb\ RE + RE} \tag{9}$$

$EQ10 := isolate(EQ2, vb);$

$$vb = \frac{zb\ vi + Rs\ ve}{zb + Rs} \tag{10}$$

$EQ11 := subs(EQ10, EQ9)$

$$ve = \frac{\frac{gm\ zb\ RE\ (zb\ vi + Rs\ ve)}{zb + Rs} + \frac{RE\ (zb\ vi + Rs\ ve)}{zb + Rs}}{zb + gm\ zb\ RE + RE} \tag{11}$$

$EQ12 := isolate(EQ11, ve)$

$$ve = \frac{gm\ zb\ RE\ vi + RE\ vi}{zb + Rs + gm\ zb\ RE + RE} \tag{12}$$

$EQ13 := subs(EQ10, EQ3)$

$$vc = -gm \left(\frac{zb\ vi + Rs\ ve}{zb + Rs} - ve \right) RL \tag{13}$$

$EQ14 := subs(EQ12, EQ13)$

$$vc = -gm \left(\frac{zb\ vi + \frac{Rs\ (gm\ zb\ RE\ vi + RE\ vi)}{zb + Rs + gm\ zb\ RE + RE}}{zb + Rs} - \frac{gm\ zb\ RE\ vi + RE\ vi}{zb + Rs + gm\ zb\ RE + RE} \right) RL \tag{14}$$

$EQ15 := simplify(EQ14)$

$$vc = -\frac{RL\ gm\ zb\ vi}{zb + Rs + gm\ zb\ RE + RE} \tag{15}$$

$$EQ16 := \frac{EQ15}{vi}$$

$$\frac{vc}{vi} = -\frac{RL\ gm\ zb}{zb + Rs + gm\ zb\ RE + RE} \tag{16}$$

So now we have the output at the collector as a function of the input signal. What do we have to do to make the gain from input to emitter the same as the gain from the input to the collector (i.e. to make a unity gain buffer with two outputs in antiphase with eachother). In EQ17 the -1 deals with the inversion of vc with respect to ve.

$EQ17 := rhs(EQ16) = -1 \cdot rhs(EQ8)$

$$-\frac{RL\ gm\ zb}{zb + Rs + gm\ zb\ RE + RE} = -\frac{RE\ (gm\ zb + 1)}{zb + Rs + gm\ zb\ RE + RE} \tag{17}$$

$EQ18 := isolate(EQ17, RL)$

$$RL = \frac{RE\ (gm\ zb + 1)}{gm\ zb} \tag{18}$$

Assume gm. zb >>1 in this case we can get rid of the 1 in the numerator because it's very small compared to gm.zb, so:

$$EQ19 := RL = \frac{RE\ (gm\ zb)}{gm\ zb}$$

$$RL = RE \tag{19}$$

To get ve and vc signal swing of equal amplitude, RL = RE (assuming gm.zb >> 1, which is usually true)

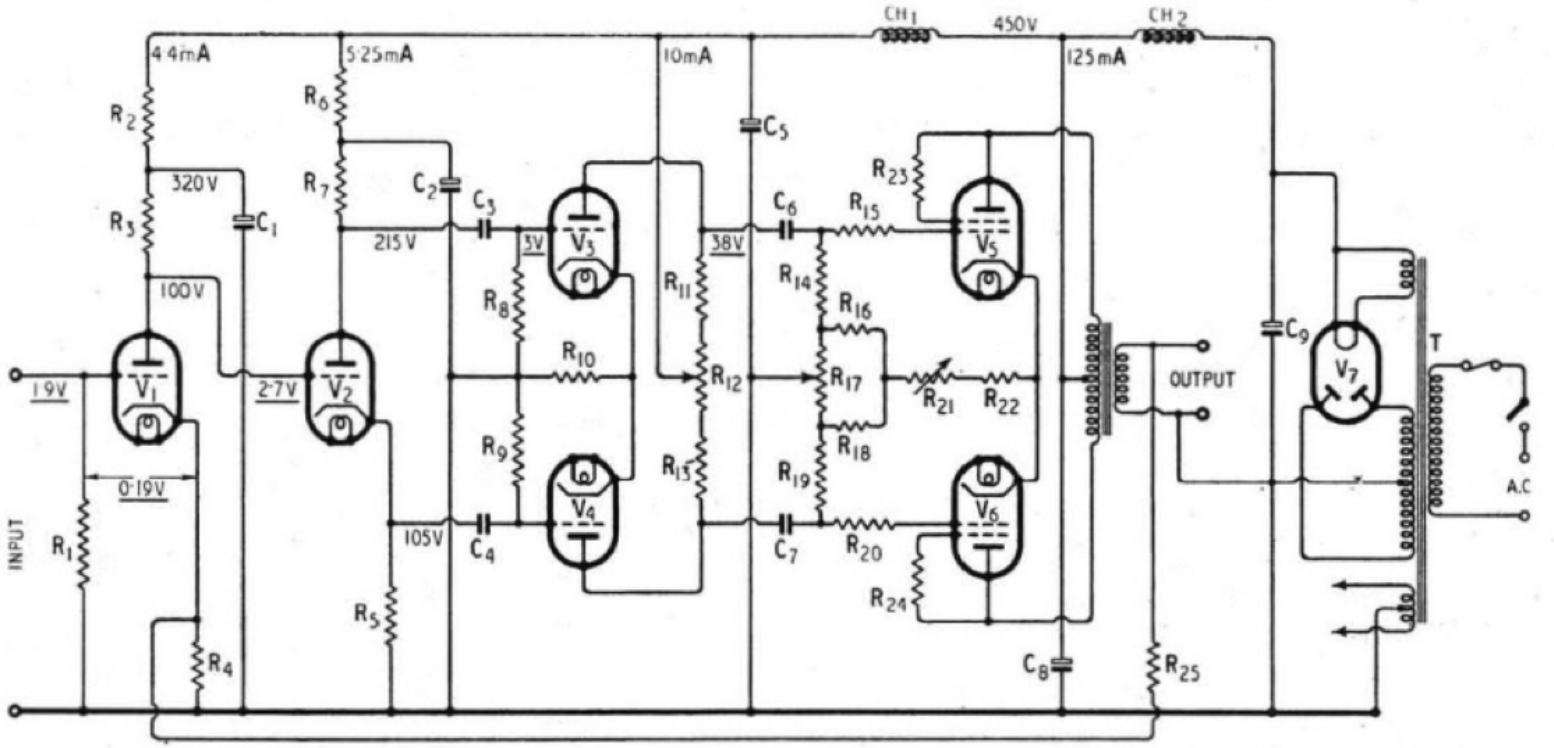


Fig. 5. Circuit diagram of complete amplifier. Voltages underlined are peak signal voltages at 15 watts output.

CIRCUIT VALUES.

R_1	1 MΩ ½ watt ± 20 per cent	R_{15}, R_{20}	1,000Ω ½ watt ± 20 per cent	C_8	8 μF 550 V, Wkg.
R_2	33,000Ω 1 watt ± 20 ,,	R_{16}, R_{18}	100Ω 1 watt ± 20 ,,	C_9	8 μF 600 V, Wkg.
R_3	47,000 Ω 1 watt ± 20 ,,	R_{17}, R_{21}	100Ω 2 watt wire-wound variable.	CH_1	30 H at 20 mA (Min.)
R_4	470 Ω ½ watt ± 10 ,,	R_{22}	150Ω 3 watt ± 20 ,,	CH_2	10 H at 150 mA (Min.)
R_5, R_6, R_7	22,000 Ω 1 watt ± 10 ,,	R_{23}, R_{24}	100 Ω ½ watt ± 20 ,,	T	Power transformer. Secondary 425-0-425 V, 150 mA (Min.) 5 V. 3A, 6.3 V. 4A, C.T.
R_8, R_9	0.47 MΩ ½ watt ± 20 ,,	R_{25}	1,200 √speech coil impedance, ½ watt.		
R_{10}	390 Ω ½ watt ± 10 ,,	C_1, C_2, C_5	8 μF 450 V, Wkg.	V_1 to V_4	L63
R_{11}, R_{13}	39,000 Ω 2 watt ± 10 ,,	C_3, C_4	0.05 μF 350 V, Wkg.	V_5, V_6	KT66.
R_{12}	25,000 Ω 1 watt wire-wound variable.	C_6, C_7	0.25 μF 350 V, Wkg.	V_7	U52.
R_{14}, R_{19}	0.1 MΩ ½ watt ± 20 ,,				

Figure 6.11: The popular “Williamson” audio amplifier schematic, 1947.

Figure 6.12: Photograph of one implementation of the popular "Williamson" audio amplifier. The valves are closest to the photographer on the left. Transformers and inductors at the back and on the right. Capacitors are the grey boxes, and are of the "paper in oil" type. In the case the value bases are point to point wired. Other components (resistors and smaller ceramic capacitors) are wired on "tag strip". Circuit boards were not commonly used in 1947, having been invented in the interwar period by Paul Eisler. They were not widely used in consumer products until considerably after WWII.

6.9 The relationship between small signals and the DC power supply

Dear James,

I am sorry for bothering you again. I suddenly got an idea but not sure if it is right, is the signal's point of view just when the transistor has been converted into small signal equivalent circuit? And in this case, the Vcc can be ignored as ground, although it has been grounded, the effect of the Vcc still exist, for example in problem sheet one operational amplifier anatomy, Q6 part 1 Ie, $I1$, $I2$ and $I3$ had been calculated rely on Vcc which is 15 V, the result had been used in the rest of the question but Vcc can be ignored as the rest of question is talking about small signal equivalent circuit? Signal source is the only thing we need to focus on? Should I always treat Vcc as grounded in small signal equivalent circuit?

Yes. Your description is exactly right. :-)

6.10 Relationship between beta h_{FE} and h_{fe}

Dear James,

I am sorry I got question again and again, please do not kill me... I am working on 2013–2014 past paper Q3 a (iii) and came cross "both T1 and T2 have an h_{FE} of 100 and both have an hfe(=β) of 200". I am confused. Based on my understanding of h_{FE} and h_{fe}, the capital FE is for large signal and lower case fe is for small signal. Is that means, when I am calculating r_{be}, as it is from small signal equivalent circuit, I should use h_{fe}; and I am calculating I_C or I_B, as it can be calculated without small signal equivalent circuit, I need to use h_{FE} rather than h_{fe}?

The short answer: yes, you're right again.

The long answer: This question is as deceptive as this long answer is long and winding. One would expect that the DC current gain $h_{FE} = (I_C/I_B)$ would be equal to the small signal current gain h_{fe} or β at low frequencies, say less than 10 kHz or so and generally speaking that is true. $h_{fe} = \beta = h_{FE}$ at "low frequencies". It turns out – but we don't discuss it in EEE225 – that β ($\equiv h_{fe}$) drops as frequency increases. This is a frequency dependence effect of the transistor, which is similar to frequency dependence in operational amplifiers but it is sometimes 1st, 2nd or 3rd order depending on how realistic the model needs to be for the circuit you're thinking about and what frequency range you're

working in. This change of β with frequency is why we need a definition of β (h_{fe}) and h_{FE}. If β didn't change with frequency it would always = h_{FE} and we'd only have one term for both of them.

If even a 3rd order transistor model is not enough to give an accurate model (usually $f = 30$ MHz $\rightarrow$ 1 GHz) we imagine that the base emitter junction can be modelled by a transmission line of $R//C$ separated by R series elements. If that's not enough we usually resort to another kind of n–port linear network idea e.g. S–parameters, which will probably only come up in some 4th year lectures on high speed circuits (http://en.wikipedia.org/wiki/Two-port_network). An n–port networks approach is always used above 1 GHz.

Millman* describes feedback using n-ports. It's very general which means it is readily applied to very many situations and is therefore a powerful analysis tool. But like a lot of powerful tools it requires rather a lot of thought to get used to the ideas that drive it, these ideas are quite abstract at times, so I don't teach it in EEE225. But having finished EEE225 you should be fine to explore it on your own without suffering too much.

A good review of how the transistor small signal modelling has developed (from a historical perspective) and the effects of cheaply available computational power is given by R. L. Pritchard who was a prolific researcher in the modelling of transistors shortly after their invention up until about 2000, http://tinyurl.com/o545pql. This paper has some excellent references, but many are heavy going so need a fair bit of effort to follow.

Anyway back to the sample paper question... It assumes a fictional device in which h_{FE} does not equal β at low frequencies. This is done to ensure that the student answering the question knows the difference between β and h_{FE}. If they are the same number, how will I know if you're thinking about using h_{FE} and β for your large and small signal calculations respectively? The solution to my problem is to present a question with an unrealistic device in which $I_B = I_C/100$ but $r_{be} = 200/g_m$ ($h_{FE} = 100$ but $\beta = 200$). In this way I know what's going on in your head (scary ehh!), even if you don't write down any equations. Of course you will be writing out all your working... wont you?

If you're interested in the frequency dependence of transistors try Millman* or Analysis and Design of Analog Integrated Circuits by Grey, Hurst, Lewis and Meyer or Sheffield's EEE331 course notes (now superseded by EEE338 or EEE335 I think.). If you're feeling brave you could jump in the "deep-end" by trying: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6268302. If you do look at that IEEE paper, I call h_{FE}, β_0 which in my view makes everything a lot clearer – the zero means "0 Hz". Others may disagree of course.

*Yes, I'm very keen on Jacob Millman... He won the IEEE Education Medal in 1970. McGraw Hill sponsored a teaching grant in his name until 2004, 22 years after his death. I consider him a key figure in post 1950 electronic circuits education along with F. E. Terman, P. R. Grey, S. Seeley, R. J. Smith, R. C. Dorf, P. Horowitz and W. Hill. Other lists for pre 1950 and for things like electronic devices, control systems, microwave engineering etc. exist but they're also just my opinion. I encourage you to read about those yourselves and form your own opinions about who made a significant contribution and who was a one-hit-wonder.

Much can be learned, by those willing to look, think and try some examples, from the past and from the struggles of others. This is true even if the problems those prior workers found almost insurmountable seem trivial in modern times.

6.11 Current Mirror Balance

Dear James,

I attached a photo of the thing I felt wrong (figure 6.13). In the second paragraph, after "in other words", I think $I_{C6} = I_I$ should be $I_{C6} = I_{C7}$. Am I right?

Best Regards,

You are half right. This circuit will make $I_{C6} = I_{C7}$ assuming the transistors are identical, but under ideal circumstances no base current would flow, then $I_{C7} = I_I$ which is what we're thinking about in the bit you've been reading. If you look further down the page below (22) the text goes on to say that in this circuit $I_{C6} = I_{C7}$ not I_I.

6.12 Differential Pair I

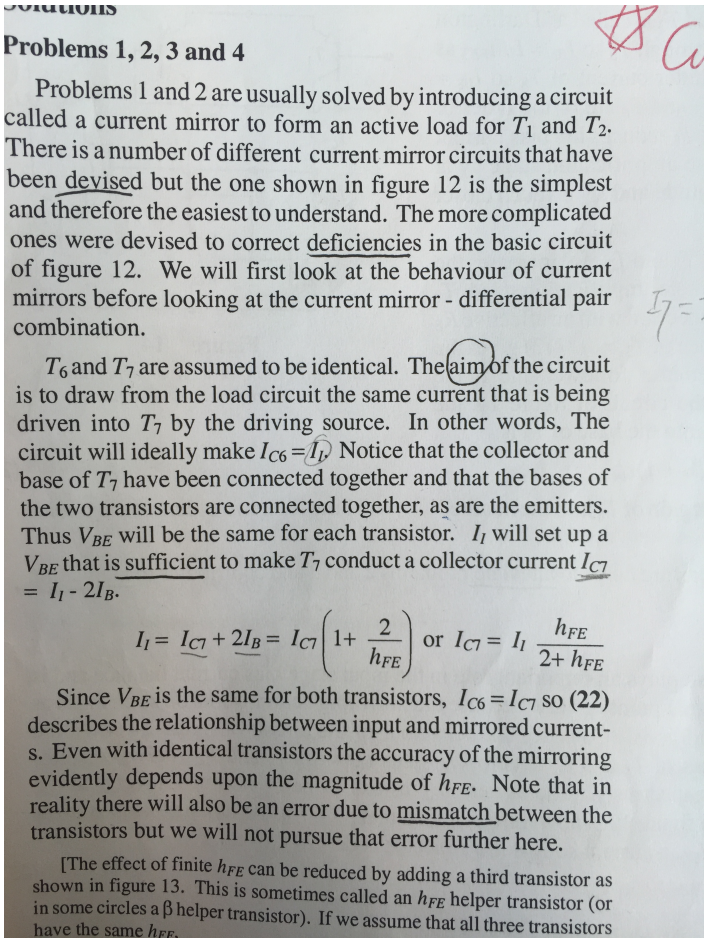
Hi James,

For the answer of Q3 in 2012–2013 past paper, part (a)(ii) the differential pair is constructed with two pnp transistors, and current mirror is constructed by two npn transistors, I think the answer is wrong since It said the differential pair is constructed by two npn transistors. Pls tell me is I'm wrong.

Kind regards,

What you have said is correct, but the solution is not wrong either.

The solution says "this could be drawn equally well with a npn differential amplifier and a pnp current mirror" or similar. i.e. it would be ok to invert the circuit



Problems 1, 2, 3 and 4

Problems 1 and 2 are usually solved by introducing a circuit called a current mirror to form an active load for T_1 and T_2. There is a number of different current mirror circuits that have been devised but the one shown in figure 12 is the simplest and therefore the easiest to understand. The more complicated ones were devised to correct deficiencies in the basic circuit of figure 12. We will first look at the behaviour of current mirrors before looking at the current mirror - differential pair combination.

T_6 and T_7 are assumed to be identical. The aim of the circuit is to draw from the load circuit the same current that is being driven into T_7 by the driving source. In other words, The circuit will ideally make $I_{C6} = I_I$. Notice that the collector and base of T_7 have been connected together and that the bases of the two transistors are connected together, as are the emitters. Thus V_{BE} will be the same for each transistor. I_I will set up a V_{BE} that is sufficient to make T_7 conduct a collector current $I_{C7} = I_I - 2I_B$.

$$I_I = I_{C7} + 2I_B = I_{C7}\left(1 + \frac{2}{h_{FE}}\right) \text{ or } I_{C7} = I_I \frac{h_{FE}}{2 + h_{FE}}$$

Since V_{BE} is the same for both transistors, $I_{C6} = I_{C7}$ so **(22)** describes the relationship between input and mirrored currents. Even with identical transistors the accuracy of the mirroring evidently depends upon the magnitude of h_{FE}. Note that in reality there will also be an error due to mismatch between the transistors but we will not pursue that error further here.

[The effect of finite h_{FE} can be reduced by adding a third transistor as shown in figure 13. This is sometimes called an h_{FE} helper transistor (or in some circles a β helper transistor). If we assume that all three transistors have the same h_{FE}.

Figure 6.13: Notes page on Current Mirrors.

– that is to say a candidate can draw an npn differential with a pnp mirror and get the marks or the candidate can draw a pnp differential loaded by an npn mirror and also get the marks.

6.13 Effect of Current mirror on differential pair

In past paper 2012–2013 section B Q3 a. (iii), about the advantages to be gained by using a current mirror as an active load for a differential pair. The answer states four advantages of it: one of them is "increases stage gain because of high impedance at the output node". Rely on my understanding of current mirror, the functions of it is that using the negative signal and also for balancing the I_{C1} and I_{C2}, as I_{C6} is larger than $0.7/R$ (I guess), so it reduces the I_{B3}, then T8 has been added before T3 for generating a larger base current for T3. These are the functions and advantages I can imagine, so I don't understand why it can increase the stage gain (Is it just as simple as adding one resistor can increase the resistance? Adding two more transistor can increase the impedance, if my guess is right, I think the calculation of the proof can be very complicated by using small signal equivalent circuit.), I think it is the T8's advantage that increase the input impedance of op-amp in the amplification stage.

You're really asking how does the current mirror increase the stage gain, I think.

The gain of any stage is some function of the transconductance of one or more active devices and the load(s) that that device(s) see. In the case of Problem Sheet 1 question 6, for example, the g_m is of the first transistor and the resistor in question is R_1. R_1 also sets the stage quiescent current because it has the 0.7 V of T3 across it. Since g_m is proportional to I_C and I_C is set by the size of R_1 and increasing the I_C requires a commensurate reduction in R_1 which will reduce the gain of the stage! Overall there is negligible change in gain if one attempts to do this. It seems therefore that we can not win... However a current mirror can be used to balance the currents in the two collectors of a differential pair and to present an output impedance to the differential pair transistors of r_{ce} which will be in the 10 – 100 kΩ range or similar. In this way we we can take away the dependence of I_C on R_1 and the dependence of gain on R_1. I_C becomes dependent on the tail current only (more or less) and R_1 is dependent on the Early voltage of the mirror transistors.

You rightly say that the current mirror also provides twice the g_m. This is because the unused half of the signal in the differential pair is moved over to the other leg and flipped in sign so that it acts to increase the apparent current driven into or pulled out of the base of T3 (it is also possible to think about this as there being a bigger change in v_{be} across the base emitter of T3). Either way gain doubles with little effort on the part of the designer.

To get the output impedance of the current mirror, go back to section 6.7. I sent out a hand drawn derivation about a week or two ago which showed that for a non-degenerated mirror, the output resistance was equal to r_{ce}.

6.14 Differential Pair II

> Dear James,
>
> For this question. I would like to ask. If question only ask for differential pair. Is that mean it connect with a current source without the transistor at the right hand side. However, if the question ask about for small signal diagram should I replace current source with a load resistor and with another transistor at right hand side. I am confusing about this, but they all called differential pair?

When we talk about differential pair we only mean two transistors whose emitters are connected to a single current pathway (which may be a resistor or a current source). When we talk about a differential pair with a current mirror we mean at least four transistors. There are two which form the differential pair and a further two which are the mirror. It may be that a fifth and or sixth transistor are also used to make an active current source in the tail of the pair.

When we perform small signal analysis on the differential pair we usually hold one input at ground and adjust the other input either above or below the first. In this way there is a difference in the input voltages and that is sufficient to produce an output. If we do hold one of the inputs at ground then it turns out that the transistor whose input we have grounded looks like a common base amplifier from the point of view of the other transistors emitter. This is very useful as we can perform a side analysis to show that the input resistance looking into a common base amplifier is approximately $1/g_m$ and that in the differential pair this resistor is connected from the emitter of the input transistor to the ground. This side analysis allows us to get rid of one of the transistor hybrid-π models and therefore greatly simplify the analysis problem. I think this simplification is one of the things you talk about in your question. It would be a good idea to have a look at me doing Question 6 part ii from problem sheet 1 in a video as all of what I have said here is covered in detail https://youtu.be/rs9mVtP7pDs

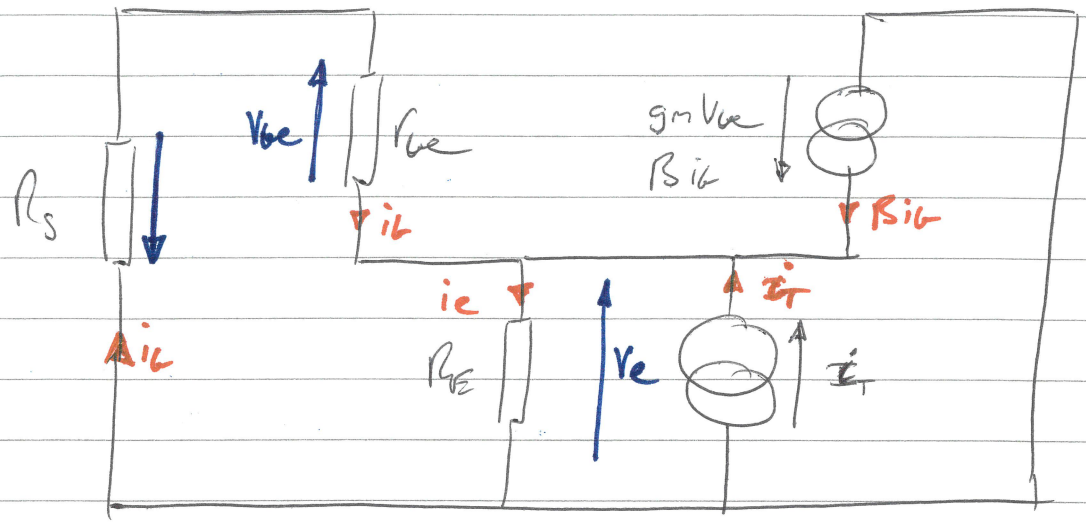
6.15 Emitter follower output resistance

I have prepared the derivation from Slide 6 of EEE225 Lecture 2 by hand so that you can see every line of working and some description of how the equation is reduced at the end by getting rid of the parts that are not dominant. This can

tell us what's important and what can be ignored and is very useful when the number of transistors in the circuit starts to increase.

EMITTER FOLLOWER OUTPUT RESISTANCE

11/11/15.



SUM I @ EMMITTER NODE:

$$i_b + \beta i_b + \dot{I}_T = i_e \qquad (1)$$

$$i_b(1+\beta) + i_T = i_e \qquad (2)$$

$$i_b(1+\beta) + I_T = \frac{V_e}{R_E} \qquad (12)$$

SUM I AROUND R_S, r_{be} & R_E...

$$i_b R_S + i_b r_{be} + i_e R_E = 0$$

$$i_b(R_S + r_{be}) = -i_e R_E \qquad (\text{AND } V_e = i_e R_E.$$

$$V_e = -i_b(R_S + r_{be}) \qquad (13)$$

(13) → (12).

$$\therefore \quad i_b = \frac{-V_e}{R_S + r_{be}}$$

$$\frac{-V_e}{R_S + r_{be}}(1+\beta) + I_T = \frac{V_e}{R_E}$$

$$\frac{-V_e}{R_s + r_{be}} + \frac{-V_e \beta}{R_s + r_{be}} + I_T \frac{-V_e}{R_E} = 0$$

$$V_e \left(\frac{-1}{R_s + r_{be}} - \frac{\beta}{R_s + r_{be}} - \frac{1}{R_E} \right) + I_T = 0$$

$$\not{-} V_e \left(\frac{1 + \beta}{R_s + r_{be}} + \frac{1}{R_E} \right) = \not{-} I_T$$ (INVERT BOTH SIDES)

$$R_o = \frac{V_e}{I_T} \ldots$$

$$\frac{V_e}{I_T} \left(\frac{1 + \beta}{R_s + r_{be}} + \frac{1}{R_E} \right) = \frac{I_T}{I_T}$$

$$\frac{V_e}{I_T} = \frac{1}{\frac{1 + \beta}{R_s + r_{be}} + \frac{1}{R_E}}$$

$\frac{1}{R_E}$ IS VERY SMALL AND WE CAN IGNORE IT.

$$\therefore \frac{V_e}{i_T} = \frac{1}{\frac{1 + \beta}{R_s + r_{be}}} = \frac{R_s + r_{be}}{1 + \beta}$$

LETS ASSUME $\beta >> 1 \quad \therefore (1 + \beta) \simeq \beta$

SO WE HAVE $\frac{R_s + r_{be}}{\beta}$ OR $\frac{R_s}{\beta} + \frac{r_{be}}{\beta}$

REMEMBER ME!

NOW $g_m = \frac{\beta}{r_{be}}$ SO $\frac{r_{be}}{\beta} = \frac{1}{g_m}$.

So the final form is:

$$r_o = \frac{V_e}{i_T} = \frac{R_s}{\beta} + \frac{1}{g_m}$$

This shows us that looking into the output we see the source resistance reduced by β added to a term related to I_c (the quiescent collector current.)

often we say $r_o \simeq \frac{1}{g_m}$ because it is often the bigger of the two if I_c is modest and R_s is $\sim k\Omega$...

6.16 Checking small signal models and simulation of transistor circuits

Hi James,

I'm currently making my way through the questions in the additional problem sheet (ED: this is now part of problem sheet 1) you provided – it is very useful!

Overall, I feel the DC conditions section of the questions fine; I've been calculating the parameters and then using simulations to verify whether what I have done is correct or not.

The issue I'm having is knowing whether the small signal model I develop is correct or not - I've found it is possible to verify the parameter values (i.e. voltages, gain, etc) using simulation but it is based on that initial model. My question is, is there any way to verify the small signal model that is developed is accurate or not?

Any response would be appreciated. Thank you.

Kind regards,

You can do numerical simulations in SPICE which is fine. Either by setting up a transistor with the correct DC conditions and then performing a .tran or .ac analysis or by setting up a small signal model in SPICE and calculating the g_m by hand for the I_C which you calculate by hand. I attach an example of this for a common emitter amplifier in the style of Q1 on the sheet you're working on (See Commonemitteramplifiersmallsignal.asc). This example is made up for LTSpice (http://www.linear.com/designtools/software/). Speaking of LTSpice there is a very good user group at https://groups.yahoo.com/neo/groups/LTspice/info with lots of help and examples. You have to join the group to get access.

The other possible method is to do your drawing of the small signal circuit and then have a program like Maple, Mathmatica or Mathcad do the maths for you. You can do the whole business algebraically and then put numbers in at the end and plot some graphs. It has several drawbacks though. Firstly, there is still no guarantee that the small signal model is correct. Secondly, the computer does not know about standard forms of transfer functions and the answers it produces are often difficult to interpret unless you do some more manipulation thereafter. Moreover there is no chance to use these programs in the exam, so I generally advise students not to bother with them. I often use Maple and Matlab in my research though.

The only method I have for developing the small signal model is a terminal by terminal replacement of the transistor with the π model and then conversion of all the high value capacitors to short circuits and low value capacitors (such as the collector to base capacitance in a transistor) to open circuits. All the DC voltage sources are shorted and all the DC current sources are open. The only other thing is practice, over and over and over.

I will try to provide more solutions for the new problem sheet (ED: This is now done). I have several more questions to add to it as well, but it takes an unbelievable amount of time to write them out. If you're feeling ok with question 1 I strongly suggest you concentrate your efforts on Q10 next. There is a moderately difficult integral that is required in part 6 and the solution to it is required to do part 7 and 8 as well. The integral is not examinable in 225, it used to be in 204 though, and I can't see the harm in expanding your reach a bit you'll need it for 223. If you're pushed for time though you can leave it out. It turns up in my second semester design project as well so will benefit students working on that.

If you want some more advanced stuff on the frequency dependence of the op-amp at the transistor level I can send you some notes I wrote years ago. They are not lecture quality but they do the job. Otherwise there's always Grey Hurst Lewis and Meyer.

6.17 Output stage (degeneration) resistors

Dear James,

For the output stage of an op amp, I notice that in the handout to lecture 5, slide 8, an improved output stage is depicted (attached). I understand the purpose for the transistor and resistor configuration at the input of the OPS, however I am struggling to understand the purpose of R_{E4} and R_{E5} (circled). Is this to increase the input resistance of T9?

Many thanks,

P.S Apologies for the closeness of this to the exam, I realised that it's bank holiday weekend after I'd written this but everything just feels like one long day at the moment!

It is not close to the exam! I fully expect to receive emails at 2 am on Tuesday morning, whether I'll answer them or not is dependent on how good the bottle of Rioja on my shelf is. If it's good there's not much chance of an answer...

The resistors R_{E4} and R_{E5} do increase the external load resistance as seen from the output of T9, but only marginally as they are very low value resistors com-

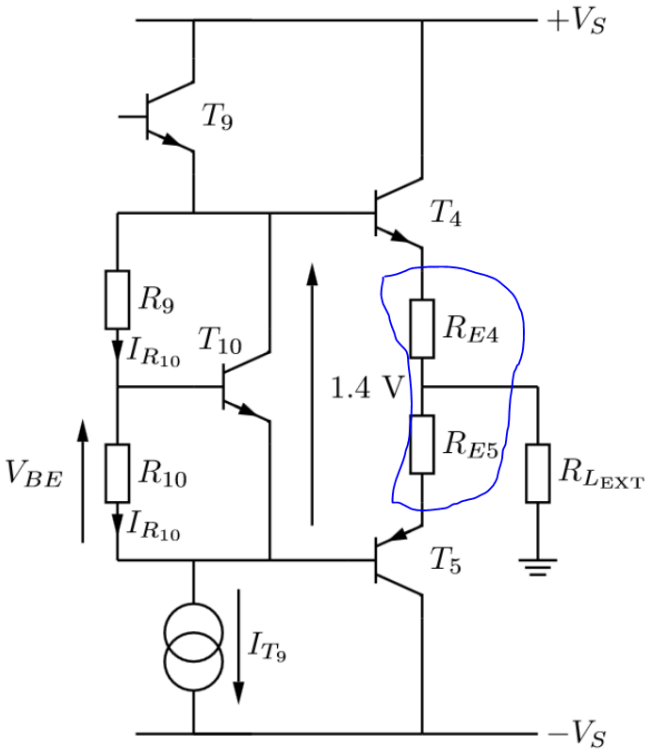


Figure 6.14: Push Pull Output Stage.

pared to the expected size of the load resistor and the global feedback acts to minimise the output resistance thereby reducing their apparent value. R_{E4} and R_{E5} could be 50 Ω in an integrated circuit op-amp and a load resistance for a standard op-amp will be probably a few kΩ (special apps such as line drivers or ADC drivers etc. will be different). These resistors serve at least two useful purposes:

1. They allow the designer to set the quiescent current in the output stage. This is the constant current which flows from the upper supply to the lower supply and ensures that both transistors are just about in their forward active region and hence crossover distortion is minimised i.e. Class B operation. By choosing the voltage we'd like to measure across R_{E4} and R_{E5} we can select the quiescent current by Ohm's Law. We usually do this in discrete circuits by making R10 a variable resistor. In real integrated circuits a couple of transistors are used in a number of cunning arrangements.

2. They provide thermal stability. Since the voltage across T10's collector emitter is fixed at approximately 1.4 V we should consider what will happen to the collector current in T4 and T5 if their temperature increases. Their

temperature might increase due to joule heating if they carry a significant current, since we can calculate the current and power for a given load we do know they will get hot. When T increases the I_C that will flow given a certain V_{BE} goes up a little bit. This makes the transistor dissipate more power, which makes it hotter. Since the transistor is now slightly hotter, it requires a lower V_{BE} than before to maintain a certain I_C. But V_{BE} is fixed so I_C will increase, resulting in yet more power dissipation. The overall result is that the transistor is destroyed. This could take up to 20 minutes or so from switch on in a guitar amplifier but the actual thermal runaway event is all over quickly (a couple of seconds at most) and it doesn't sound very nice through a speaker when it happens. The transistor usually dies short circuit between C and E and so leaves your speaker connected to a big DC voltage which does it no good at all.

To stop this from happening we can include R_{E4} and R_{E5}. If as before the power dissipation in the transistor causes the temperature to increase and thence I_C to increase this new higher I_C will flow through the resistors and by Ohm's law the voltage across the resistor will increase slightly. We can use Kirchhoff's voltage law (KVL) around the T4, T5, R_{E4}, R_{E5}, T10 loop. $I_C \cdot R_{E4} + I_C \cdot R_{E5} + V_{BE4} + V_{BE5} = V_{CE10}$. If $I \cdot R_{E4}$ and $I \cdot R_{E5}$ are increasing and V_{CE10} is fixed then V_{BE4} and V_{BE5} must decrease somewhat. This acts to turn off the transistor slightly and reduce I_C, reducing the power dissipation and thereby reducing the temperature. It is therefore an electrical feedback system designed to ensure the thermal stability of the output stage.

We might then ask how effective R_{E4} and R_{E5} are likely to be given that they are usually in the range 0.05 – 0.5 Ω in a discrete power amp. Actually they are sufficiently effective, because I_C is proportional to $\exp(V_{BE})$ we might presume (correctly) that a small change in V_{BE} will yield a big change in I_C hence the small values of R_{E4} and R_{E5} are sufficient to adjust V_{BE4} and V_{BE5} enough to maintain thermal stability. We would like to keep R_{E4} and R_{E5} small because both the small quiescent current and the full load current flows through them and so they will dissipate a fair amount of power $I^2 \cdot R_{E4}$ and $I^2 \cdot R_{E5}$ in the form of heat, which is usually not the desired output from an amplifier.

In integrated circuit op-amps the temperature of T4, T5 and T10 are all roughly the same (isothermal conditions are in force) because they are all on the same die (chip). Heat dissipated in the power stage warms T10 quickly as the heat has little distance to travel and the thermal mass of the chip is small, it's also thermally insulated from the air by the injection moulded package. Since they will be on the same die, made in the same foundry system it is possible to make the I_C vs V_{BE} as a function of temperature characteristic for T10, T4 and T5 almost identical, hence a second *thermal* feedback loop exists. Now the current

I_{T9} is fixed so as T10 gets heated up by T4 and T5's power dissipation T10's I_C cannot increase so it's V_{BE} must drop. Since the V_{BE} of T10 has dropped $I_{R_{10}}$ will drop (Ohm's law). $I_{R_{10}}$ flows through R9 as well so the voltage across R9 will also drop. The voltage across R9 and R10 together must equal the voltage across T10's collector emitter (KVL). Hence as T10 gets hotter its V_{CE} drops, this is quite satisfyingly elegant as the V_{CE} of T10 also biases T4 and T5... All in all, both stuff and things get hotter and cooler together but the overall quiescent conditions look after themselves nicely. Minimising the temperature dependence of biasing in the output stage is highly desirable from a distortion perspective as the optimum quiescent current is often decided by distortion considerations and the crossover distortion in class B output stages is particularly sensitive to the quiescent current setting. Crossover distortion is also generally the dominant distortion mechanism in class B amplifier circuits and minimising it therefore has the biggest impact on distortion performance. Certain op-amps such as the OPA134 (one of my all-time favourites) have cunning circuits in place of R9, R10 and T10 to minimise the crossover distortion. "Google Patents" makes it relatively easy to see what the analogue integrated circuit companies are up to in this regard.

If we're not thinking about an integrated circuit op-amp (i.e. a discrete power amplifier as in EEE223) and we want to make use of the thermal feedback between T10 and T4/T5 we need to make sure that T4 and T5 are mounted on a heat-sink if we don't do this there is a reasonable chance thermal runaway will occur and they will be destroyed, certainly if Emitter resistors are not used as well. A TO220 power transistor package will have a thermal mass of about 62°C/W without a heat-sink so even 1 W will leave us with a junction temperature somewhere above 80°C. Unless we make some effort to get the heat out we can't make full use of the transistor's current carrying capacity or range of permissible V_{CE} (the "safe operating area"). We must ensure that 1) there is a big enough heat sink and 2) that we put T4,T5 AND T10 on the heat-sink so that heat can flow from T4 and T5 into the heat sink and then the heat sink can warm up T10. Of course the thermal time-constant of this thermal feedback loop is quite long 20 minutes or so is common.

There is a third type of amplifier to consider which is not considered in EEE225. It is the integrated circuit power amp (e.g.http://www.ti.com/lit/ds/symlink/lm1875.pdf, http://sound.westhost.com/project19.htm). It is a chip (quite a large one, but not as big as a PC CPU) which can be found in PC speakers, digital radios, and small practice guitar amps (10 W output or so). In this amplifier the chip is just large enough that it takes a few 100s of milliseconds for heat to flow from one part to another. What is more the thermal mass is not very high so even modest currents can cause local heating in the output stage. In such conditions the thermal connection between T10 and T4/5 is not

maintained over short timescales (1 second or so) this has lead to an assessment metric for this kind of amplifier called "thermal distortion" and if you get tired of revising all the various parts of EEE225 you might like to read about it, for example,http://www.douglas-self.com/ampins/thermald/thermald.htm.

6.18 Output stage (degeneration) resistors II

For the diagram in figure 6.15 why we suddenly add two resistor R_{E4} and R_{E5} to the circuit.

RE4 and RE5 provide

- A means of setting the quiescent current in the output stage. The voltage between Q4 and Q5's base, which is notionally but not exactly 1.4 V is equal to the $V_{B_{(Q4)}} + V_{B_{(Q5)}} + I_Q(R_{E4} + R_{E5})$. Hence if I_Q is the only variable we can use the bias voltage between the bases of the push pull transistors to set the quiescent current.
- A means of providing some local feedback around the push pull stage to prevent thermal runaway. Suppose Q4 gets hotter. The V_{BE} needed to maintain a particular I_C drops. If it does and V_{BE} does not change then I_C must increase. If I_C increases then the power dissipation in the transistor $(= I_C \cdot V_{CE} + I_B \cdot V_{BE})$ must also increase which will lead to the transistor getting hotter. This extra increase in temperature further reduces the V_{BE} required to maintain a particular value of I_C and fairly swiftly the transistor gets so hot it is destroyed. This is an example of positive feedback. If we add a resistor in the emitter of both transistors we can make the value of biasing voltage available to the transistor dependent on the value of I_C. Suppose R_{E4} is a small but finite value, suppose that the circuit is switched on from cold and I_C having settled at an initial value starts to warm the transistor. The transistor's I_C goes up because the V_{BE} is fixed by the biasing voltage and the junction temperature is rising. As I_C increases the voltage drop across R_{E4} increases. The voltage drop across R_{E4} and the V_{BE} of Q4 must sum to (approximately) half of the total biasing voltage. Since R_{E4} is getting a bigger share of the biasing voltage Q4's V_{BE} must be dropping, assuming the biasing voltage is constant. This reduction in V_{BE} acts to slightly switch off the transistor, reducing I_C and reducing the temperature of the transistor. The reduction in temperature increases the V_{BE} required for a given I_C and a balance is found between I_C, the temperature of the transistor and the voltage drop across R_{E4}. Note that $I_C = I_Q$ in this case.

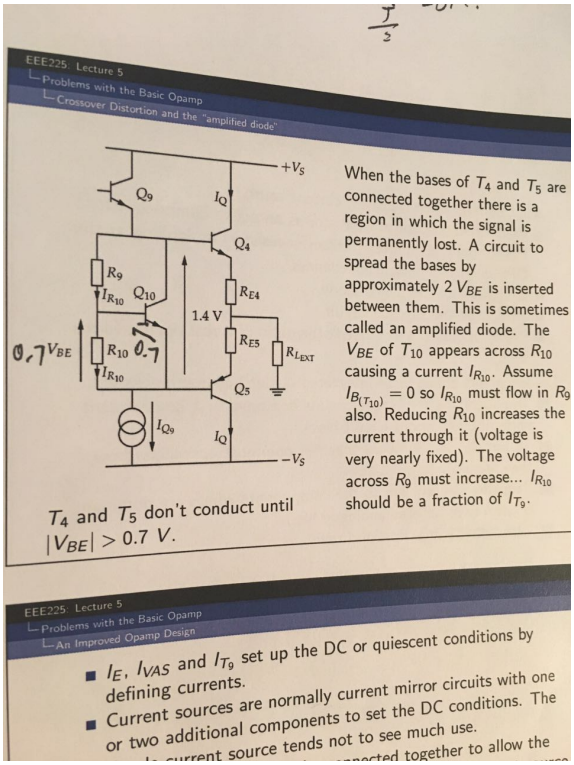


Figure 6.15: Emitter degeneration resistors in the Output Stage.

6.19 Angle of Conduction of Push Pull OPS

Good news everyone,

Some of you have revealed that you're not keen on the angles of conduction in a push pull stage. Others have been asking about a problem sheet question on EEE223. So I've rolled the two together in LTSpice.

It's not easy to answer the EEE223 problem sheet question that has caused a little difficulty using SPICE because spice takes account of parameters of the semiconductor devices that we don't consider when we use a pen and paper (like V_{BE} is not always 0.7 V among others). To make things a bit easier for my own purposes, I've wrapped the question in a negative feedback loop with a nice high open loop gain op-amp. You can still interrogate the DC conditions, try adjusting the power supply rail voltages etc. Any EEE223 question you may have to answer is not going to be solved using a simulator, some things (like design work) have to be done with a pen and paper...

Anyway, loading up the files Angle.asc, Angle.plt clicking the little running person in LTSpice will show plots of output current and the power stage transistor collector currents as a function of the value of the push pull emitter resistors. Since

these resistors set the quiescent current in the push pull stage we can change their value to move between different angles of conduction. Several values are plotted by default.

Figure 6.16 highlights the angle of conduction for each pair of current waveforms.

If you want to see the quiescent current for each case in SPICE try setting the input voltage amplitude to zero and click run.

If you don't have LTSpice it can be downloaded free from Professor Google's website.

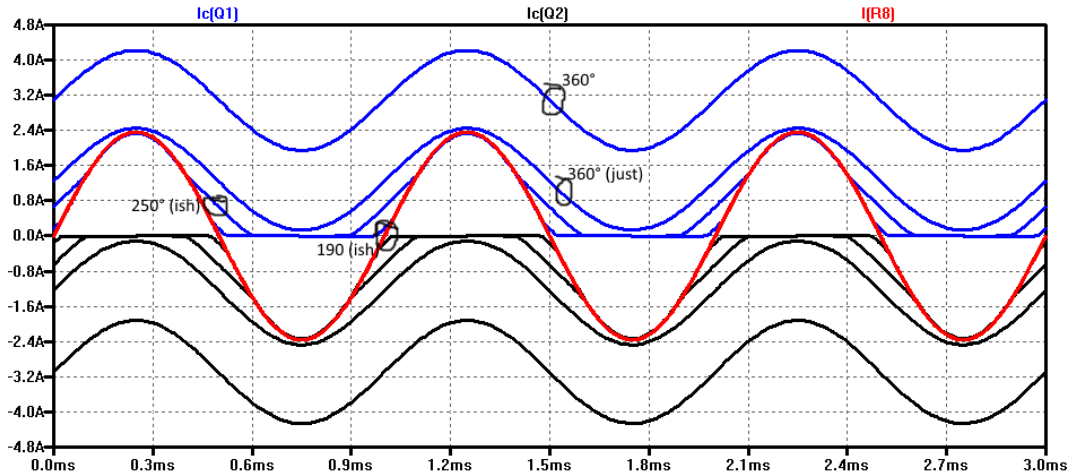


Figure 6.16: Angles of conduction in a push pull output stage.

6.20 Amplifier Classes Single Ended Current Source Load Class A vs Push Pull Class A

Dear Dr. Green,

I'm writing this e-mail to ask you to clarify a misconception I recently encountered.

Some sources (such as Russian Wikipedia page and some forums) state, that in the Class A amplifier quiescent current must be at least equal to peak current in the load, however other sources (including some other second year lectures and some other forums) state that the quiescent current only has to be at least half of the peak load current. When looking at some current graphs per each output transistor, it appears that the latter statement is true. Could you please confirm or disprove that?

Also, I attach an interesting anode voltage regulator schematic, otherwise this e-

mail would be too boring. It uses TL431, buffered with common base amplifier, all loaded with current source, in order to allow it to work on higher voltages required for the gate of regulator MOSFET.

I look forward to hearing from you.

Yours Faithfully,

Nice looking regulator. Seems like you're quite fond of the amplified band gap reference.

The question you pose about the limit of class A in terms of the quiescent current requires some discussion of the circuit shape involved. Figure 6.18 shows an LTSpice screen-shot which has two amplifiers one is a single ended emitter follower loaded with a current sink (right), the other is a push pull of two emitter followers one NPN one PNP. Both amplifier stages are designed with a quiescent current of 1 mA and a quiescent output voltage of approximately zero. They are not realistic designs. They are simplified (with the magic of the simulator) to illuminate the answer to the question. Both circuits are loaded by a 1 kΩ resistor. The figure shown in the screen shot shows the push pull circuit in the upper graph and the single ended circuit in the lower graph. Both amplifiers are driven to the point where they are on the boundary of class A operation. If the input sine wave sources are made a little larger in amplitude the amplifiers will leave class A operation and the output transistors will each conduct for less than 360° of the cycle. Looking at the size of the load resistor current in the top and bottom graphs it is (hopefully) clear that I have been able to drive the push pull twice as hard as the single ended design without leaving class A. The peak output current in the push pull case is 2 mA but only 1 mA in the single ended case. In the push pull and single ended cases the quiescent current is 1 mA... The difference in stated minimum quiescent current from the sources you cite is therefore due to each source considering a different topology of amplifier. The single ended push pull also has a maximum theoretical efficiency of half that of the Class A push pull.

If you're using LTSpice (and I can't think why you wouldn't be) save the the circuit *.asc and plot description *.plt to the same folder. Open the *.asc and just hit run. It will plot what I have shown in the picture. It should then be possible to plot anything else you want to see and also to change the amplitude of the input waveform.

ClassAPushPullvsSingleEnded.asc, ClassAPushPullvsSingleEnded.plt

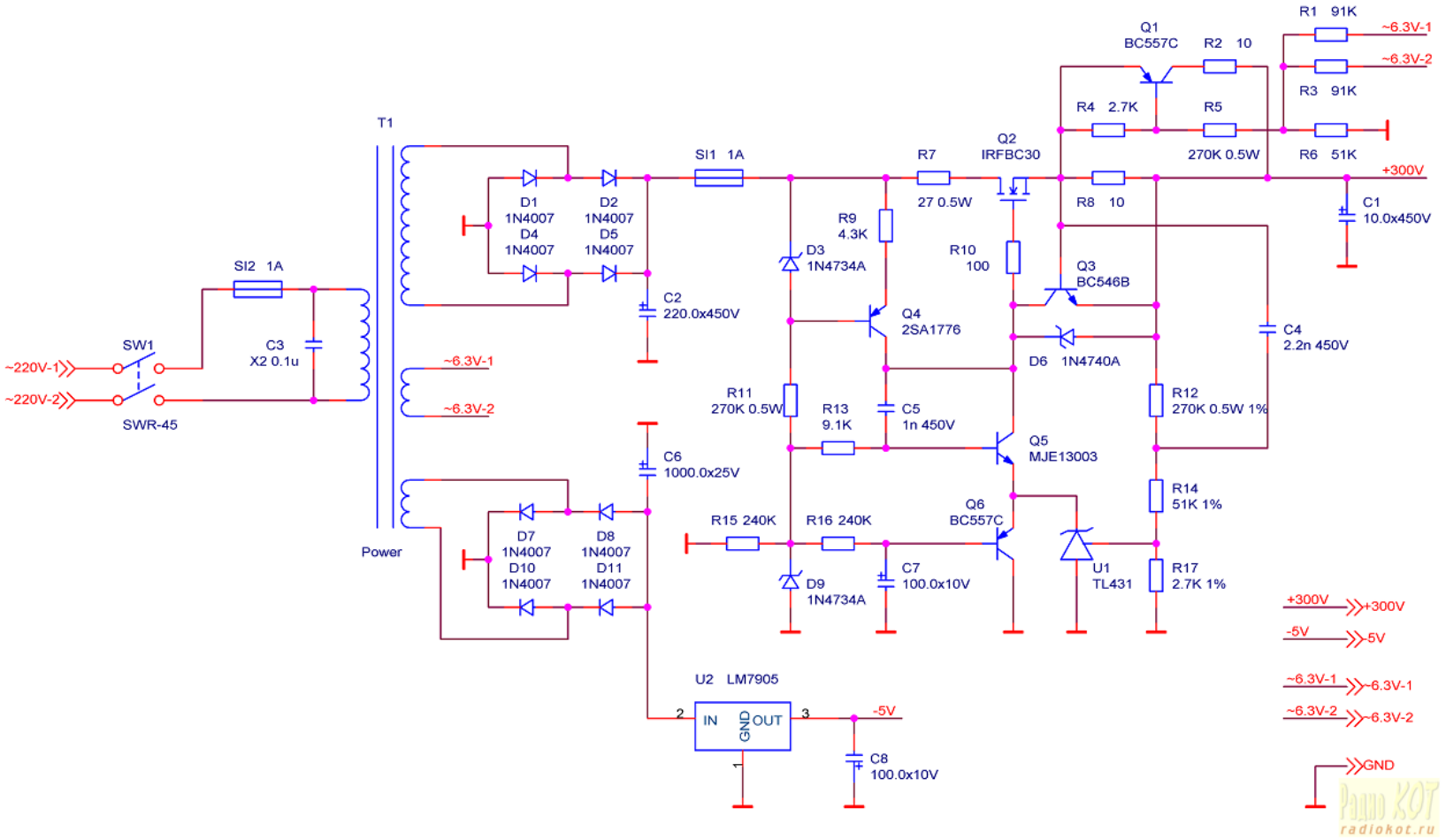


Figure 6.17: Valve HT power supply schematic.

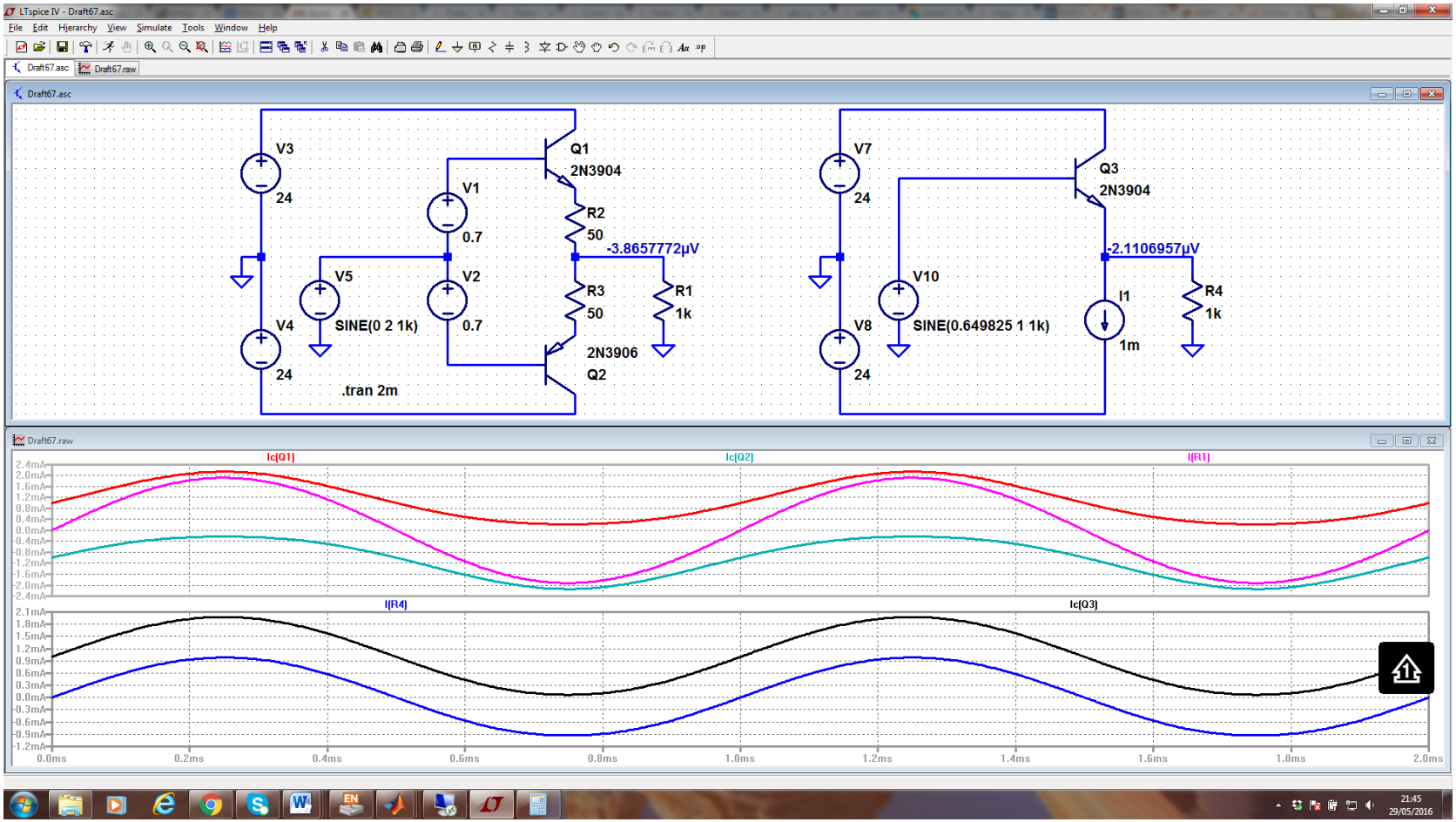


Figure 6.18: Class A Push Pull Emitter Followers *versus* Class A Single Ended Emitter Follower both at nearly the maximum linear signal excursion.

Dear Dr. Green,

Thank you for such thorough explanation. It's all clear to me now. For some reason I've been automatically assuming generic push-pull output stage when talking about amplifier classes, not considering that single-ended stages can have classes as well. Simulation files run as expected, too.

P.S. In the circuit I've sent you, take a look at Q1, which serves a pretty interesting purpose: During normal operation it shunts current sense resistor R8 with R2. However, when the regulator enters current limiting mode, and it's output voltage falls below certain level, Q1 will turn off, reducing the preset current limit by un-shunting R8, and thus preventing Q2 from dissipating too much power.

Yours Sincerely,

6.21 Why is the Small Signal Model the same for NPN and PNP?

The lecture notes said that both npn and pnp version have the same small signal equivalent which is shown in figure 6.19 (left). However, I think the small signal equivalent circuit of them should be different because the current direction of NPN and PNP is different. Would you please tell me why they have the same small signal equivalent circuit?

The small signal model deals with (small) signals. In small signal analysis, where the electronic devices' characteristics are linearised, the currents, which we often suppose are sine waves, spend half a cycle going in one direction and then half a cycle going in the other direction. In other words the two small signal diagrams (right) are identical.

The linearisation of the circuit is implicit in the small signal model because there are no non-linear components in it. The resistor and the current source are both represented by linear functions $i_b = v_{be}/r_{be}$ for the resistor and $i_c = \beta\, i_b$. Notice that all of the symbols in these equations are lower case which means signals i.e. AC quantities that are of an amplitude so small they do not move too far along the characteristic curves of the device such that, over the amplitude of the signal, the device can be approximated by the linear equations in the model all the while maintaining an acceptable level of error. This approximation brings enormous simplifications to circuit problems and means we don't have to deal with exponentials every time we want to analyse circuits with bipolar transistors and diodes, square law equations when we deal with FETs or Child's law when we deal with triodes.

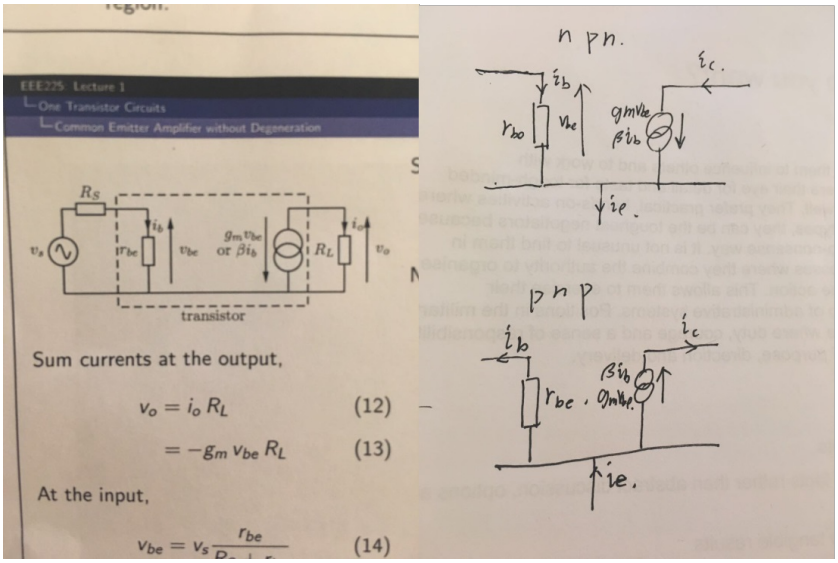


Figure 6.19: Relationship between circuit layout and small signal model of a single transistor.

ED: while we're on the subject of Child's law, something I didn't mention when I wrote this reply but could be very useful in making links between the semiconductors and circuits, especially if you like valves is the relationship between Child's law which you've probably never heard of and deals with electrons transported in a vacuum with the assumption of no scattering *versus* the Mott-Gurney law, which is very familiar to all those who have studied EEE118 but almost certainly not by that name. Mott-Gurney starts by postulating a strong scattering of carriers, perhaps due to a crystal lattice, a carrier mobility, μ, and an average saturated drift velocity, v, in an electric field. The rest is not derived in EEE118 as far as I recall but under certain conditions (no scattering) Mott-Gurney becomes the same as Child's law. The implication being that the underlying mechanism of free carrier generation is general and not a thing that only happens in semiconductors. Of course if you've studied metal semiconductor junctions in EEE225 this may not be news to you. I would think a bit of background reading about valves and crystals and electron clouds would do no harm at all in knitting together a lot of the semiconductor and circuits concepts it might even give some phenomenological insight about why shot noise exists.

6.22 Convention of current flow in small signal diagrams

In the small signal equivalent circuit, the output current is always opposite the collector current according to the graph. Could you tell me why this is always true?

It is a definition that I choose because I prefer it that way and, on the whole, no-one questions it. It could be re-written the other way if you like. My reasoning is as follows, we have current flowing into the transistor's input and a voltage at the input with respect to ground that is consistent with the direction of current flow (i.e. Ohm's law is obeyed at the input) and a current flowing out of the transistor's output and a voltage across the load resistor which is consistent with the direction of that current (Ohm's law obeyed again). Thinking about the transistor as a system the information (the signal) flows from the source into the input gets amplified and then flows out of the output and into the load, that is how the currents and voltages are drawn. If we decide that the signal flows from the source into the input and from the load into the output of the transistor, that's ok too. But we'll need to be careful to recognise that the signal flowing into the output is inverted (180° phase shift) with respect to the input. When we do algebra on the (linear) equations that describe the circuit we will find a minus sign pops up in just the right place to make it all ok. That is, assuming we've written our equations out correctly!

6.23 A Question about Cascodes

For the cascode stage, what is the voltage swing? And what is the "bandwidth" of the CE stage?

The voltage swing is the maximum voltage that the collector of the upper transistor, T2, in slide 11 of lecture 5 can rise to, minus the minimum voltage it can fall to, while maintaining T2, and therefore T1, in the forward active region. This is the maximum available 'un-distorted' signal swing. In reality there is a good deal of distortion when the signal is within this range, but what we really mean is that the stage is not 'clipping', where the collector voltage of T2 tries to fall below the base voltage of T2 or rise above the supply voltage.

The bandwidth of the stage is the high frequency at which the gain of the stage falls to -3 dB below the "mid-band" value minus the low frequency at which the gain of the stage falls to -3 dB below its mid-band value. Often the lower -3dB point is not significant in cascode circuits as the bandwidth extension we hope to achieve is at high frequencies. In figure 6.20 the high frequency -3 dB point is approximately 12 MHz and the lower -3 dB point is at 6 Hz. So the bandwidth is approximately 12 MHz.

Consider the two amplifiers in figure 6.21, the left one is a standard "Type 1" common emitter amplifier, from EEE118, with DC degeneration on the emitter which is bypassed at all frequencies of interest by C_3, such that the stage appears un-degenerated from a signal point of view. The high frequency response of this circuit is shown in black in the graph of figure 6.22. The circuit on the right of

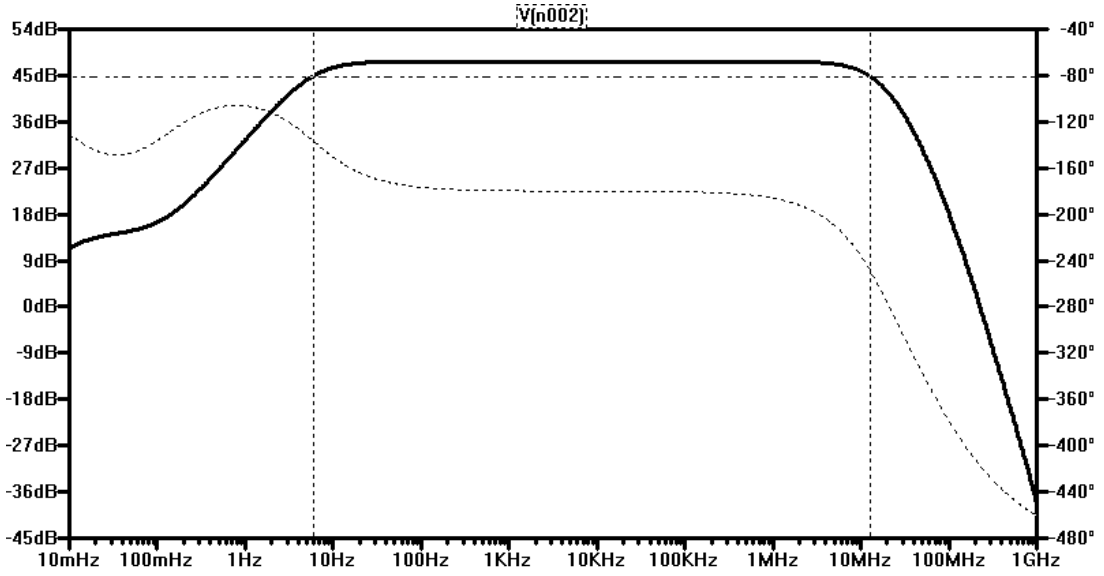


Figure 6.20: Measurement of simulated -3 dB bandwidth of an amplifier stage in SPICE.

figure 6.21 is a cascode created with the same[1] transistors. The quiescent current in Q1 and Q3 and in Q2 are all close to 1 mA the V_{CB} of Q1 and Q2 are different about 8 V vs about 4 V but this doesn't change the depletion capacitance of the reverse biased base to collector junction very much we can assume the stages are more or less identical from a signal's point of view. The key difference is that Q1 has very little voltage swing on its collector (in this case about the same as the input signal magnitude in fact). The swing on the collector of Q2 is the full output voltage. This voltage falls across the collector to base depletion capacitance and causes a current $I = C\,\mathrm{d}V/\mathrm{d}t$ to flow in C_{CB}. This current partially cancels the base current flowing into Q2. The result of this cancellation is that Q2 amplifies a base current which is smaller than we would expect, consequently the gain appears to be somewhat lower than we expect. Since the current in C_{CB} gets bigger as its impedance drops ($X_C \to 0$ as $f \to \infty$) we should expect this drop off in gain to occur at higher frequencies.

The cascode avoids significant current flowing in the C_{CB} of Q1 by not having much signal swing on the collector of Q1. The $\mathrm{d}V/\mathrm{d}t$ is small and the current is small, the small current doesn't cancel out the input current so much and the gain appears not to reduce until much higher frequencies. The lack of signal swing on the collector of Q1 occurs because the resistance looking into the emitter of

[1]Identical in fact, because SPICE doesn't know about the differences between transistors of the same type unless you set up the differences you require, for example by using a Monte-Carlo arrangement on their parameters, or otherwise making them different.

Q3 is quite small. The current generator in the collector side of the small signal model of Q1 is driving a low value load resistor, namely the input resistance of Q3, which is roughly $1/g_{m3}$. Since $V = I \cdot R$ and R is small, for a given I, V will be proportionally smaller.

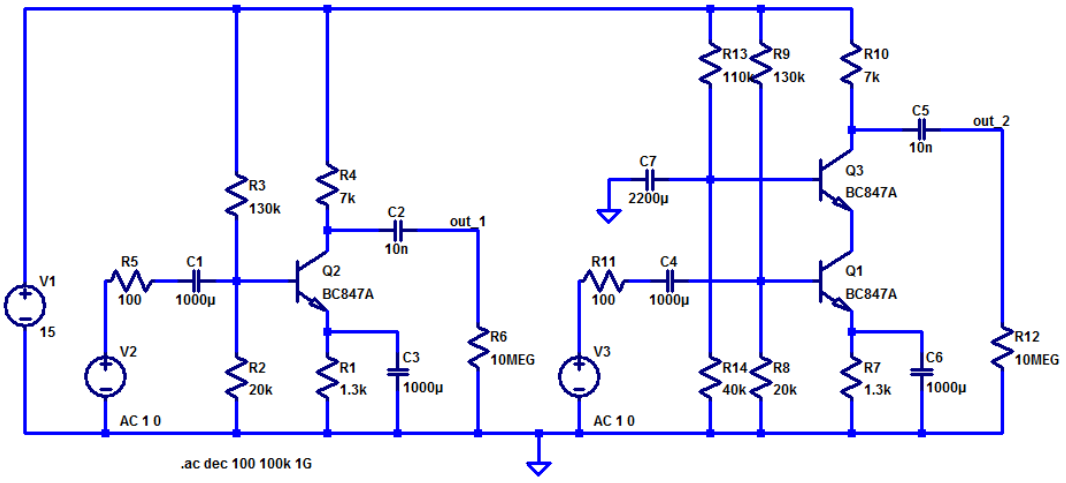


Figure 6.21: left: Type 1 common emitter with DC degeneration. Right: Similarly biased cascode version of the Type 1 (left).

6.24 Signal swing and headroom

Dear Dr Green,

I have been looking at the notes for the basic Op-amp circuit (figure 1 on page 1 of Op-amp Anatomy). One of the problems mentioned with the voltage amplifier stage (CE amplifier) is that the gain is limited by the constraints of the DC conditions. What do you mean by this?

I thought that the gain of the voltage amplifier is limited by the r_{ce3}, r_{i4} and r_{i5}.

Is the Maximum gain of the voltage amplifier $= (r_{ce3}//r_{i4}//r_{i5}) \cdot g_m$?

Sincerely,

The voltage gain of the VA is given by $g_{m3} \cdot (r_{ce3}//r_{i4}//r_{i5}//R_{VA})$ where R_{VA} is generally the smallest by quite some margin such that the approximation gain $= g_m \cdot R_{VA}$ holds.

Suppose we have a +15 V power rail and want a quiescent current of 1 mA. Let's also suppose that there is a 1.4 V biasing circuit between R_{VA} and the collector of T3 such that the output stage is properly biased. If the output voltage is zero,

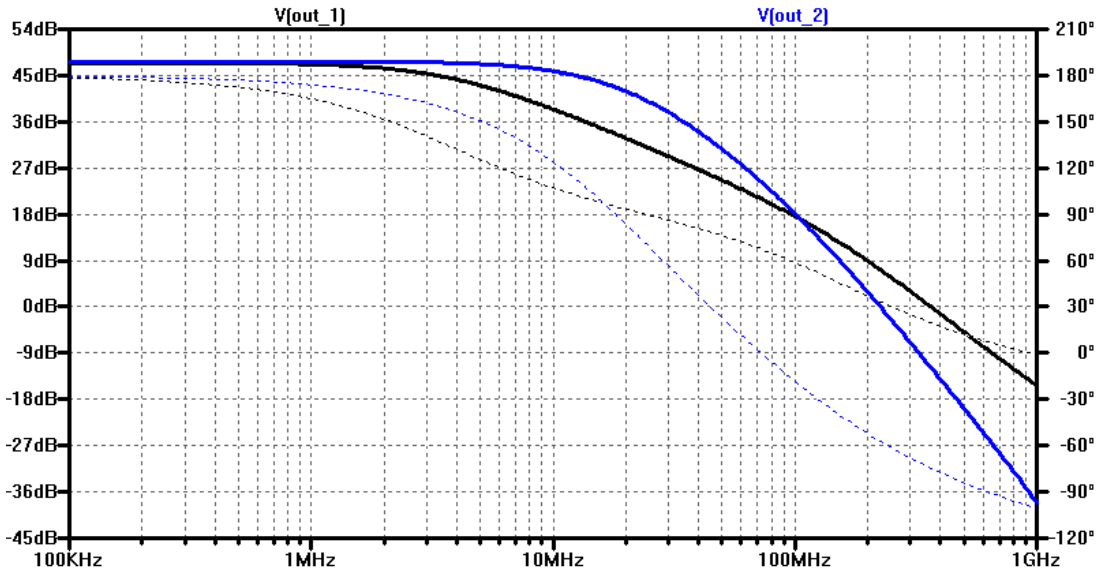


Figure 6.22: Bandwidth extension due to reduction in C_{CB} current by cascoding T1 and T2 in figure 6.21 (right).

then the voltage at the lower end of R_{VA} should be +0.7 V (half of the 1.4 V we need to bias the output stage). Then we have $I_{C3} = 1$ mA $= (15 - 0.7)/R_{VA}$. R_{VA} is therefore 14.3 kΩ. Now suppose we want to make R_{VA} bigger, to increase the gain of the VA stage for example, but we don't want to lower g_{m3}, which is $(e \cdot I_{C3})/(k \cdot T)$. Well, we can't. If we increase R_{VA} then the quiescent, DC current, I_{C3} must fall and this will lower g_{m3}. Even though R_{VA} will have gone up g_{m3} will have gone down and we may find the gain is less than before. Hence there is a limit to the value of R_{VA} which is given by the DC conditions we desire (i.e. our choice of I_{C3}).

6.25 Transconductance of a non-degenerated common emitter (e.g. op-amp VAS)

If I want to solve the transconductance of the VAS of an amplifier, as the VAS is a common emitter transistor, is the transconductance of VAS just be g_m?

Also is the transconductance $1/g_m$ of the VAS?

Yes, Just the g_m of the vas transistor.

And the gain is $g_m \cdot R_{VA}$ if r_{be} is much greater than the small signal resistance looking back into the differential pair.

6.26 Transresistance of a non-degenerated common emitter (e.g. op-amp VAS)

Thanks for your help James

Also for the second question, sorry for the typing mistake.

What I want to know is whether the transresistance is equal to $1/g_m$?

Regards

The resistance looking into the emitter is often $1/g_m$ if the base is not degenerated by a resistor (common base amplifier where base is not fully decoupled to ground). So if it's a common base amplifier with good design then the resistance looking into the emitter would be approximately $1/g_m$. Transresistance must be measured in volts per amp ($R = V/I$), so I can see where you're coming from with the $1/g_m$ idea, but a simplified derivation may point you in the right direction.

Suppose we have a transistor amplifier set up as common emitter; as in EEE118 but we don't worry about biasing resistors etc. just to keep it simple. We can assume it was biased by very large resistors that we need not take account of. That's not very realistic but it will demonstrate the method. Now suppose the signal is in the form of a current, perhaps from a photo-diode or a piezo-electric strain transducer. We will assume the source resistance in parallel with the current source is really big and we can ignore it. We are left with just a current source, a transistor and a load resistor between the collector and the positive DC power supply. We can therefore draw a small signal model by replacing the transistor with the hybrid-π model and start some algebra. See the by hand derivation in figure 6.23. We can also see clearly from this photo why I word-process all my lecture notes and do not generally use an OHP.

A paper on transresistance amplifier is at http://bioelectronics.tudelft.nl/~wout/documents/tcas20103.pdf I'm not planning for you to read it in any detail, as the fellow writing does tend to obscure fairly direct arguments in a lot of equations. Many people think, possibly sub-consciously, that big equations make them look clever but, in fact, it just makes me want to not read their work at all, unless they have some insightful words to go with the equations. The author of the paper has a nice diagram however, figure 5, which should be reasonably familiar to you. Have a look at it and identify the various circuit blocks. Answer below...

Answer: You will probably fairly quickly work out that it is a Type 2 common emitter from EEE118 but made with a cascode of two BJTs (rather than a single BJT as in EEE118) and this cascode is loaded with a one transistor current source

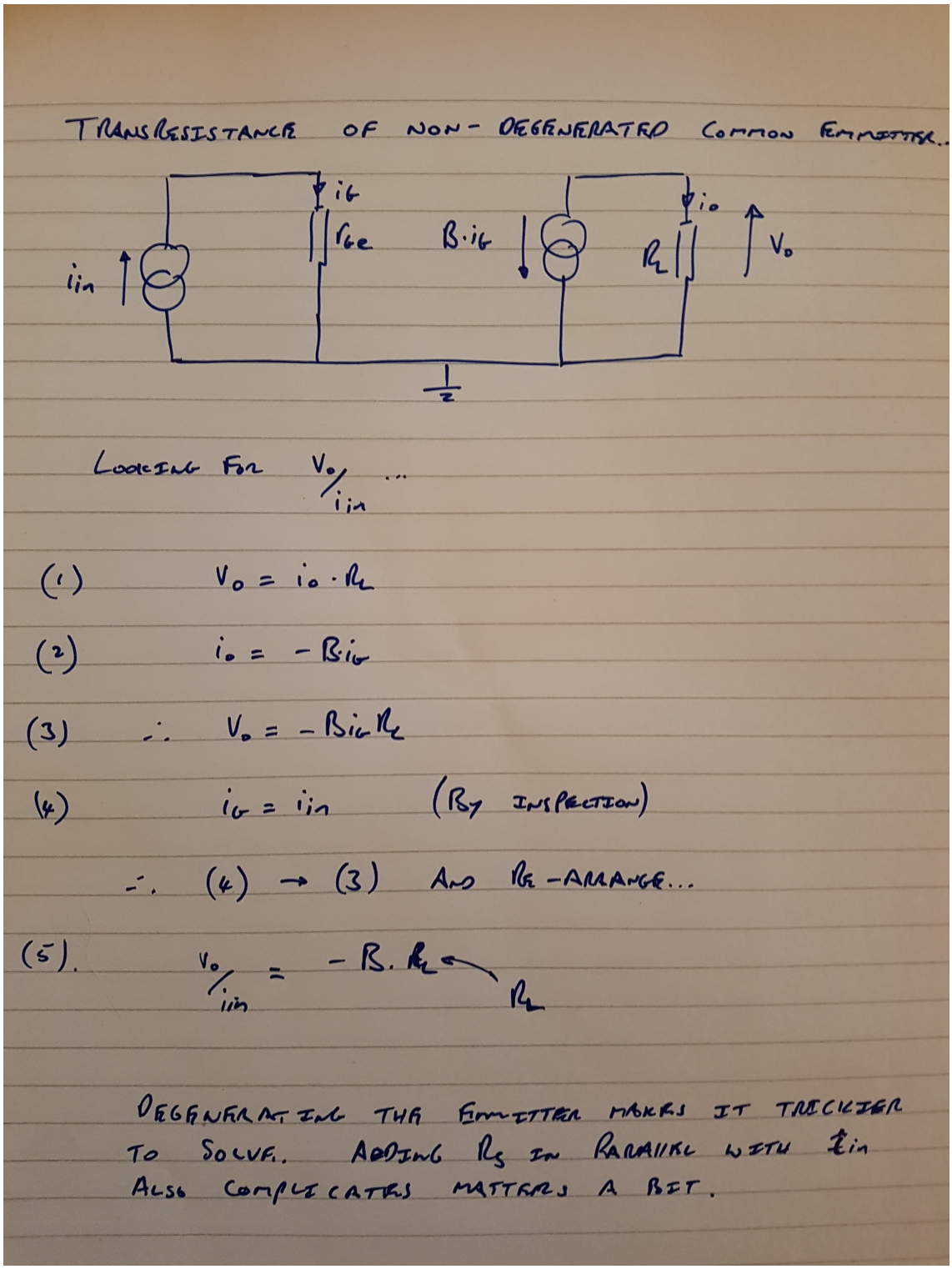


Figure 6.23: Transresistance of a common emitter stage.

rather than a resistor. The author has an interesting two part feedback scheme, but other than that this circuit should not be too troublesome for you to analyse for small signals if you needed to.

6.27 Why don't we resistively bias the stages in an op-amp?

Hi James,

Just a quick question (I'm sure you're fed up with these now). I understand that the circuits for the common emitter, common emitter with degeneration, common base etc have their biasing circuits summarised by Rs but my question is how come we do not need these when considering the op amp transistors or the circuits blocks that build up the op amp (current mirror, differential pair etc)? Is it because of the use of current sources and the loading from each stage acting on the previous stage? (i.e. why don't the transistors in the Darlington pair need biasing circuits, for example)?

Do the transistors in these circuits not need biasing circuits with resistors because they are forced into operation by current sources?

Thanks,

You are right, we try not to use resistors if we can because in integrated circuits resistors are costly to make and take up a lot of room on the die.

We discuss the one transistor circuits at length because they are a stepping stone to discussion of bigger circuits that we would probably not want to dive directly into. The analysis methods are the same for the one and many transistor circuits so practising on something smaller is always a good idea.

On the problem sheet there are no biasing resistors on the Darlington question because I want you to see, in the algebra, the effect of "stacking" the transistors without the added complexity of the biasing network as well.

Generally if we are using resistors, we try to make the biasing network with very large resistors so they have little effect Generally though, we get rid of them by using other transistor stages to provide the biasing.

6.28 Emitter follower output resistance II

Hi James,

I've got a quick question about one of the solutions on the emitter follower sheet.

On page 40, concerning the output resistance of the amplifier, you give the base current by:

$$i_b = -\frac{v_e}{(r_{be} + R_B)} \tag{6.1}$$

I'm struggling to see this simplification. I can see $i_b = \frac{v_{be}}{r_{be}}$, but I'm not sure how v_e gets involved. (I've attached a snap of this page in the solutions).

I'd appreciate some help on this!

Incidentally, there's also a typo on that page: above equation (163) - 'finr', I thought you'd like to know.

Kind regards,

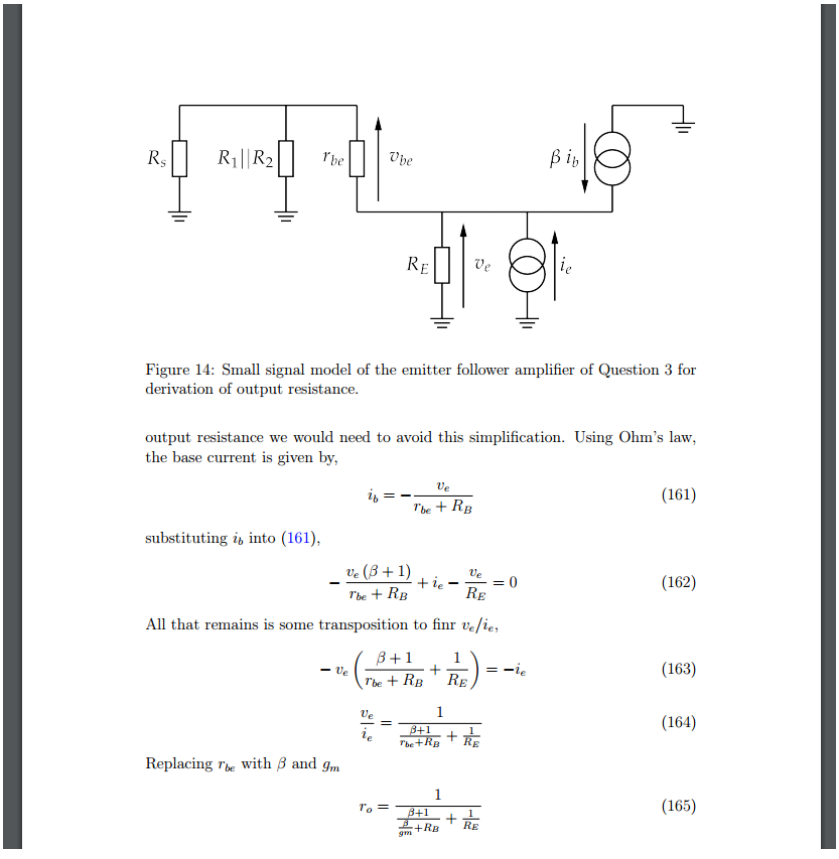


Figure 14: Small signal model of the emitter follower amplifier of Question 3 for derivation of output resistance.

output resistance we would need to avoid this simplification. Using Ohm's law, the base current is given by,

$$i_b = -\frac{v_e}{r_{be} + R_B} \tag{161}$$

substituting i_b into (161),

$$-\frac{v_e(\beta+1)}{r_{be} + R_B} + i_e - \frac{v_e}{R_E} = 0 \tag{162}$$

All that remains is some transposition to finr v_e/i_e,

$$-v_e\left(\frac{\beta+1}{r_{be} + R_B} + \frac{1}{R_E}\right) = -i_e \tag{163}$$

$$\frac{v_e}{i_e} = \frac{1}{\frac{\beta+1}{r_{be}+R_B} + \frac{1}{R_E}} \tag{164}$$

Replacing r_{be} with β and g_m

$$r_o = \frac{1}{\frac{\beta+1}{\frac{\beta}{g_m}+R_B} + \frac{1}{R_E}} \tag{165}$$

Figure 6.24: Output resistance of the Emitter follower.

I thought I'd made a mistake for a moment, but it's ok.

v_b (the voltage across $R_s//R_1//R_2$), v_e and v_{be} are all in a source free loop so they must all sum to zero (KVL). In (161), I'm doing Ohm's law on the $(R_s//R_1//R_2)+$

r_{be} combination by noting that $v_{be} + v_b = -v_e$ and that all of the base current must flow in the $R_s//R_1//R_2$ combination and in r_{be} because these are in series.

It's an algebraic sleight of hand that allows me to avoid introducing another variable (v_b) and then having to write another equation to eliminate it...

Thanks James,

I drew some intermediary circuits, and remembered that if i_b is coming up through R_B, then v_b would be pointing down the page to make $v_b + v_{be} + v_e = 0$ true. After that it's not so bad, and I think I more or less get it now.

Thanks again,

6.29 EEE225 Problem Sheet 1 Q4 part 4

Dear James,

In question four part 4, (215) on your solutions say that you're summing currents into the emitter. You've written:

$$\frac{v_{be1}}{r_{be}} + g_{m1} \tag{6.2}$$

I'm confused because surely it should be $v_{be1} \cdot g_{m1}$, not g_{m1}, for the second term. I thought g_m was $(\frac{i_c}{i_b})$, a gain, not a current?

Am I missing something obvious?

Well spotted, it should be $g_{m1} \cdot v_{be1}$

6.30 Multi-gate transistors

Hi James,

I saw this article [1] and it piqued my interest. I had a look into the GAA transistors and found out that multigate transistors [2] were a thing, I am trying to think about how they would work but I just can't seem to figure it out. I saw this presentation from the IEEE [3] but it left more questions.

This article from the IEEE [4] talks about the use of fins to reduce the effect of the device conducting during the off state due to leakage but it does not seem (at least not me) explain the benefit of multiple gates.

I have probably missed something fundamental but hopefully, you can point it

out.

Regards,

References:

1. https://techcrunch.com/2017/06/05/ibm-creates-a-new-transistor-type-for-5nm-silicon-chips/
2. https://en.wikipedia.org/wiki/Multigate_device
3. https://www.ieee-jp.org/section/tokyo/chapter/ED-15/2012/WIMNACT%2031%20presentation/WIMNACT%2031%20Huang.pdf
4. http://spectrum.ieee.org/semiconductors/design/transistors-go-vertical

The multi-control electrode devices have at least three uses.

A thyristor is a "four doping region dual BJT" – well sort of, it's a kind of latching switching transistor effectively. It latches until the current stops by virtue of the AC waveform crossing zero. There is only one 'base' electrode but it is still a four region device. It is not generally counted as a dual base device.

A dual gate MOS transistor or a dual grid valve (a hexode) can be used as a mixer (for modulation of a carrier wave by an information signal).

A dual gate MOS transistor can be connected as a transistor where each gate is connected to the same signal and the objective is to use the geometry (several short gates on a "3D" buried structure) to increase the effectiveness of a switch by allowing the short gate and therefore high switching frequency but still maintaining strong inversion and therefore more ideal switching behaviour.

Hi James,

I can't quite visualise who the effectiveness is increased by having the short gate. Surely the electrons will just travel through that (path of least resistance.) Is there a way of simulate these in LTSpice? Maybe a model might help with seeing quite what is happening.

When you say simulate, which device do you want to simulate?

A dual gate FET for high density IC processes would be simulated with something like a BSIM implementation (e.g. https://www.silvaco.com/products/analog/spicemodels/models/bsim-cmg/bsimmg.html) in SPICE. Ideally in LTSpice but the models of this type are not often free or open source and the companies that routinely use them are also using a particular foundry and it's the

foundry that provide the models for their process which is verified. Unless you're a fab-less IC company you generally don't need these kinds of models as you don't have the capacity to get a physical device that is a good approximation to the model... Of course this doesn't stop you from reading about how the models work.

If you want to simulate a power device Thyristor, Diac, Triac then a regular spice model in LTSpice will be fine for example `http://ltwiki.org/files/LTspiceIV/lib/sym/EXTRA/ST/TRIAC/Triac_st_09_09_08.lib` is a TRIAC library free on the LTWiki. there is a triac symbol in LTSpice. Just check that the gate really does link to the gate etc. Instructions on how to use libraries are on the LTSpice Wiki.

By way of example, put triaccct.asc in your `[ltspiceroot]` directory.

Put ST TRIACs.asy in `[ltspiceroot]/sym/MISC/`.

Put st_standard_snubberless_triacs.lib in `[ltspiceroot]/lib/sub/`.

Open `triaccct.asc` and run.

You should find an average power of 2.06 kW dissipated in the 24 Ω load.

Chapter 7. Op-amp Modelling & Feedback Questions

7.1 EEE204 2011 Q1

EEE204 2011 Q1 I don't understand how the transfer function is obtained when no nodes connect back to Vin (same applies to EEE204 2012 Q1).

The feedback must always be negative - that is to say it must act to reduce the size of the input signal. This is in order to find the difference between the input and the feedback, this difference or "error" is multiplied by the open loop gain of the op-amp and acts to force the output voltage to the appropriate value. Since the feedback must be negative it goes to the inverting input. This is still feedback to the input, just not the input you're thinking of. Have a look in lecture 16 of EEE118 where I discussed the generic feedback system and it should become clear (with a bit of luck).

7.2 EEE225 Problem Sheet 2 Question 3 "minus sign"

The reason for the existence of the minus sign in the solution of problem sheet 2 question 3 is derived in by hand in the next few pages.

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SHEET 2 Q3 WHERE DOES THE "−" SIGN COME FROM? (1)

$$\frac{V_o}{V_i} = \frac{1}{1 + j\frac{\omega}{\omega_0}} \qquad A_0 >> 1$$

$$\frac{V_o}{V_i} = \frac{1 - j\frac{\omega}{\omega_0 A_0}}{\left(1 + j\frac{\omega}{\omega_0 A_0}\right)\left(1 - j\frac{\omega}{\omega_0 A_0}\right)}$$

$$\frac{V_o}{V_i} = \frac{1 - j\frac{\omega}{\omega_0 A_0}}{1 - j^2\frac{\omega^2}{\omega_0^2 A_0^2}} = \frac{1 - j\frac{\omega}{\omega_0 A_0}}{1 + \frac{\omega^2}{\omega_0^2 A_0^2}}$$

$$\frac{V_o}{V_i} = \underbrace{\frac{1}{1 + \frac{\omega^2}{\omega_0^2 A_0^2}}}_{Re} - \underbrace{\frac{j\frac{\omega}{\omega_0 A_0}}{1 + \frac{\omega^2}{\omega_0^2 A_0^2}}}_{Im}$$

$$\phi = \tan^{-1}\left(\frac{Im}{Re}\right) = \tan^{-1}\left[\frac{-\frac{\omega}{\omega_0 A_0}}{\frac{1}{1 + \frac{\omega^2}{\omega_0^2 A_0^2}}}\right]$$

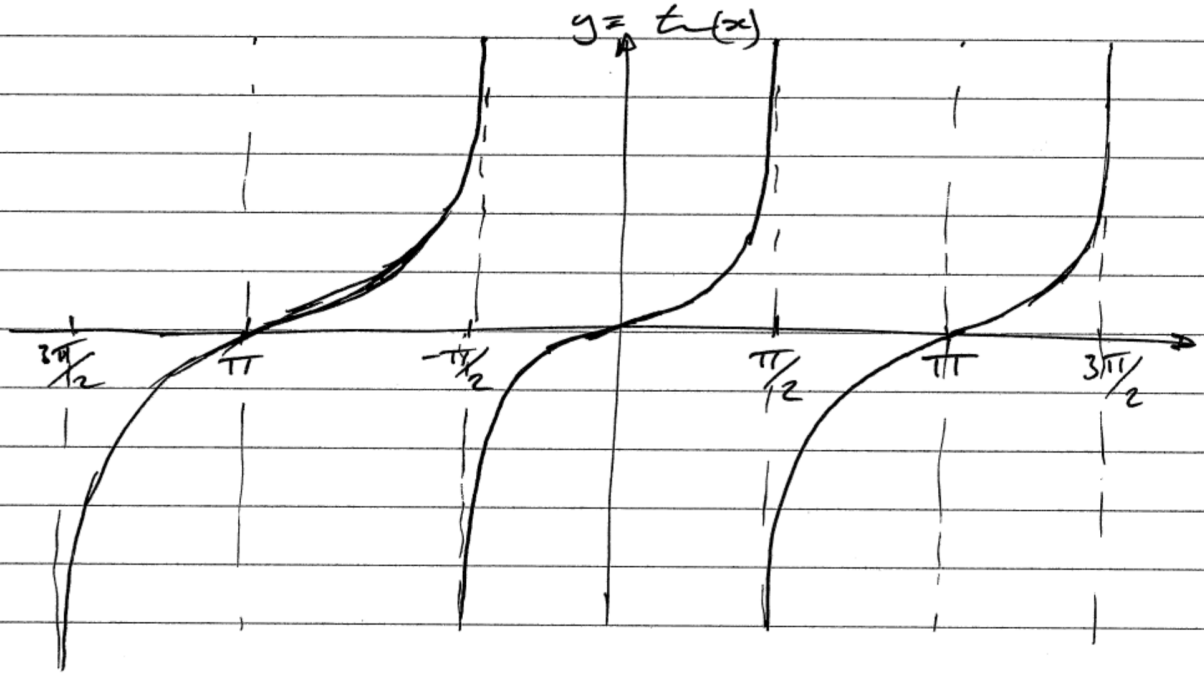
CANCEL

225

(2)

$$\phi = \tan^{-1}\left(\frac{\frac{-\omega}{\omega_0 A_0}}{1}\right)$$

BUT, THINK ABOUT $\tan(x)$ AS A GRAPH...



So $\tan(\alpha) = -\tan(-x)$ ...

NOT SURE? TAKE AN EXAMPLE... $\tan(89^\circ) = 57.28...$

AND $\tan(-89^\circ) = -57.28...$ $-\tan(89^\circ) = -57.28...$

So $\phi = -\tan^{-1}\left(\frac{\omega}{\omega_0 A_0}\right)$

HELLO!

Chapter 8. Compensation of Op-amp Questions (non inverting amplifier with unity gain compensated op-amp)

8.1 Sketch the Open Loop Gain and Phase...

> Dear James,
>
> I am working on the sample exam paper, which I am confusing the question 11 a. The second part you said sketch a open loop bode plot before and after, I checked the notes but I cannot even understand it about the figure 19. Can you give me an answer about this question.
>
> Best wishes

Try section 8.11 in "Microelectronics" by Sedra and Smith, specifically the discussion of figure 8.38. Or try Chapter 13 I think (possibly 14) in Millman. Or the lecture notes and handouts for EEE225 (the graph has a big blue bit shaded in). This question appeared in the 2014 – 2015 exam, but was a short question so a full answer was not required to obtain all the marks, looking at the solutions there would be a good idea.

If you like you can find the same information presented somewhat differently in Opamps for Everyone at http://www.cypress.com/?docID=52587 page 7-11 although I would start at the beginning of chapter 7.

8.2 Op-amp Amplifiers in Series

> Hi James,
>
> I've been working through the most recent sample paper and I am struggling to find the GBP for two op amps in series shown in question 6b. I've tried multiplying the two transfer functions of the op amps turning the circuit into a second order system but I can't seem to calculate the new -3 dB point.
>
> Thanks

This question is lifted directly from the 2012 - 2013 paper – all of the questions in the sample paper are taken from a prior exam or from this year's midterm. The prior exams and solutions are on line. Let me know if not.

The sample paper is not supposed to be a test *per se*. It's supposed to show what the new style of exam will look like in terms of the question layout. I provided it principally to give students an opportunity to see how things like timing might pan out on the day - since there are no similar exams in this style. The questions are all answerable by looking at solutions from other year's exams.

For this problem there are two first order linear and time invariant systems. When we want their combined effect, we multiply their transfer functions – as you correctly said. Therefore assuming the gains are equal we have to find a number which when squared is 64 (it's 8). So the closed loop low frequency gain of each stage will be 8 to yield a total low frequency gain of 64.

The GBP of the amplifiers is 16 MHz so each amplifier will have a -3 dB bandwidth of 2 MHz (2×8 MHz...), However that's not what you're looking for, although we do need to know it. Using the -3 dB frequency would yield the -6 dB (half voltage or half current as opposed to -3 dB which is half power) frequency of the combination. We seek the -3 dB of the combination and since dB is a log scale, when we add or subtract we actually multiply and divide in a linear scale hence we seek the -1.5 dB point of each amplifier.

Using the first order equation for a low pass system and equating the gain we want (lhs) with the magnitude of the first order expression for a low pass system where the corner frequency is the bandwidth of the op-amp with a LF gain of 8 (rhs) we have,

$$A = \frac{A_0}{1 + j\,\frac{f}{f_0}} \tag{8.1}$$

$$10^{\left(\frac{-1.5}{20}\right)} = 8 \cdot \left| \frac{1}{1 + j\,\frac{f}{2\times 10^6}} \right| \tag{8.2}$$

$$\text{or} \quad \left| \frac{1}{1 + j\,\frac{f}{2\times 10^6}} \right|^2 = \frac{1}{1 + \left(\frac{f}{2\times 10^6}\right)^2} = 10^{\frac{-3}{20}} \tag{8.3}$$

$$8 \cdot 10^{\left(\frac{-3}{20}\right)} = 8 \cdot \left[\frac{1}{1 + \left(\frac{f}{2\times 10^6}\right)^2} \right]^{0.5} \tag{8.4}$$

solve for f, $f = 1.29$ MHz.

That's fine, provided you can see how we got from the lhs of (8.3) to the middle of (8.3). If it is not clear, we can do some extra lines of working. We need to first observe that in the rhs of (8.3) we have $-3/20$ raising the 10, but in (8.2) we have $-1.5/20$. This is because we have squared the lhs of the (8.3) and so must

square the rhs too. Presuming we don't know what the shortcut is, we could try the long way from (8.2).

The long way involves using the complex conjugate to find the absolute value (the magnitude) of the rhs of (8.2) and then to square it afterwards, doing some cunning factorising and thereby arriving at the middle of (8.3).

$$A = A_0 \left| \frac{1}{1 + j\,\frac{f}{f_0}} \right|^2 \tag{8.5}$$

$$= A_0 \left(\frac{1\left(1 - j\,\frac{f}{f_0}\right)}{\left(1 + j\,\frac{f}{f_0}\right)\left(1 - j\,\frac{f}{f_0}\right)} \right)^2 \tag{8.6}$$

$$= A_0 \left(\frac{1 - j\,\frac{f}{f_0}}{1 - j^2\,\frac{f^2}{{f_0}^2}} \right)^2 \tag{8.7}$$

use $j^2 = -1$ and splitting real and imaginary parts,

$$A = A_0 \left(\frac{1}{1 + \frac{f^2}{{f_0}^2}} - \frac{j\,\frac{f}{f_0}}{1 + \frac{f^2}{{f_0}^2}} \right)^2 \tag{8.8}$$

square and root the real and imaginary parts,

$$A = A_0 \left[\left(\frac{1}{\left(1 + \frac{f^2}{{f_0}^2}\right)^2} + \frac{\frac{f^2}{f_0^2}}{\left(1 + \frac{f^2}{{f_0}^2}\right)^2} \right)^{0.5} \right]^2 \tag{8.9}$$

cancel the powers,

$$A = A_0 \left(\frac{1}{\left(1 + \frac{f^2}{{f_0}^2}\right)^2} + \frac{\frac{f^2}{f_0^2}}{\left(1 + \frac{f^2}{{f_0}^2}\right)^2} \right) \tag{8.10}$$

Expand the denominators and take the f_0^2 into the denominator of the second fraction,

$$A = A_0 \left(\frac{1}{\left(1 + \frac{f^2}{{f_0}^2}\right)\left(1 + \frac{f^2}{{f_0}^2}\right)} + \frac{f^2}{{f_0}^2\left(1 + \frac{f^2}{{f_0}^2}\right)\left(1 + \frac{f^2}{{f_0}^2}\right)} \right) \tag{8.11}$$

Expand the denominators some more,

$$A = A_0 \left(\frac{1}{1 + \frac{2\,f^2}{{f_0}^2} + \frac{f^4}{{f_0}^4}} + \frac{f^2}{{f_0}^2 \left(1 + \frac{2\,f^2}{{f_0}^2} + \frac{f^4}{{f_0}^4}\right)} \right) \tag{8.12}$$

multiply numerator and denominator by ${f_0}^4$,

$$A = A_0 \left(\frac{{f_0}^4}{{f_0}^4 + 2\,f^2\,{f_0}^2 + f^4} + \frac{f^2\,{f_0}^2}{{f_0}^4 + 2\,f^2 {f_0}^2 + f^4} \right) \tag{8.13}$$

factorising the numerator and the denominator,

$$A = A_0 \frac{{f_0}^2 \left(f^2 + {f_0}^2\right)}{\left(f^2 + {f_0}^2\right)^2} \tag{8.14}$$

cancelling common factors,

$$A = A_0 \frac{{f_0}^2}{f^2 + {f_0}^2} \tag{8.15}$$

divide through by ${f_0}^2$

$$A = A_0 \frac{1}{1 + \frac{f^2}{{f_0}^2}} \equiv A_0 \frac{1}{1 + \left(\frac{f}{f_0}\right)^2} \tag{8.16}$$

8.3 2012 – 2013 exam Q3 part b

In the exam paper 12-13 Question 3,b the solution use the low pass standard form equation to get the answer, but i do not understand why use this equation in the process...

In this course we always assume that the op-amp designer has compensated the op-amp such that it behaves as if it is a linear system with a single pole at some frequency. Being a first order system it will follow some rules many of which are shared with first order passive networks. GBP = constant, rise-time = $2.2\,\tau$ and $\tau = \frac{1}{\omega_0}$. At ω_0 the phase shift will be -45° (i.e. lagging) and the magnitude response will have dropped by 3 dB from it's low frequency value.

When we need to work out the gain at a certain frequency and we have information about the gain bandwidth product and the closed loop gain, we can use these equations along with the standard first order low pass equation to compute our answers. Consider the solution given on the website and the statements above and it should become clear. If not get back to me.

8.4 How to read a Bode Plot, the nature of poles and zeros, systems and quality factor

Dear James,

I am looking over pole-zero circuits but am still struggling to define a "pole" or a "zero". Am I right in saying that a pole is were the phase moves from 90° phase and moves towards 0° phase and a zero is just the inverse of this?

Thanks,

Poles and zeros seem to cause a lot of conceptual problems for the great majority of people. There is rather a lot made of them but in essence there is nothing magical about them that warrants the amount of conceptual trouble they seem to cause. The implications of their existence and manipulating them gives rise to much of the theory of control systems and a good deal of the theory of circuit design especially circuits using feedback. Much of our efforts are aimed at controlling their position and what happens to them as our circuits and systems operate.

8.4.1 Physical systems

This question comes up in some form or another every year and can be best answered in the form of an FAQ by posing several fictitious questions designed to deal with certain parts of the discussion needed to fully answer the original question.

Spring − mass − damper example We can start with some phenomenology, some discussion of some commonly used example systems in, kinematics, the branch of mechanical engineering that deals with forces on objects and their motion. Suppose I have a mass a spring and a damper so arranged in the style of a common A-level/IBAC physics question, that is, the mass is on the end of a spring with a damper connected between the two ends of the spring and one end of the spring attached to an immobile point. The system is free to move up and down under the influence of gravity and other forces imparted on it. We presume gravity exists and I pull down on the mass (storing energy in the spring) and then let go and we can find the displacement of the mass with respect to a prescribed fixed point as a function of time. It's going to be the classical response of a damped second order system to a step driving function. It will look like a sine wave who's amplitude decreases with time. The shape of the amplitude decay (it's envelope) will be exponential.

Pendulum example We might also take the example of a pendulum attached to a fixed structure at a single point acting under gravity. I take the pendulum from its resting position and release it. It swings back and forth. If I attach a pencil to the pendulum and put some paper on the ground under the pendulum such that the paper is just marked by the pencil and then I pull the paper along the ground perpendicular to the direction of motion of the pendulum (suppose I have a long roll of paper like a chart recorder), at a constant speed, the pencil line will describe the same shape on the page as our plot of the mass position as a function of time in the first thought experiment.

Simple harmonic motion – a mechanical oscillator Now suppose that, as the pendulum comes back towards the position from which I released it, I give it a small push just at the moment it becomes stationary at the highest point of its swing. I do this to replace the potential energy that has been lost in the last cycle of the pendulum due to the conversion from potential to kinetic energy and all the friction and drag the pendulum experiences as a result. For example friction at the point where the pendulum is attached to a fixed structure and also viscous friction of the air due to the motion of the pendulum through the air etc. We need not actually consider the air resistance, we could run the experiment in a vacuum but I have found that my laboratory is much more suited to my working in it if there is a breathable atmosphere. We add energy to overcome the losses. If we add more energy than the losses the pendulum will swing higher in the next cycle (and the losses will increase a bit). If we keep pushing it at the new "bit harder" level the pendulum will go up higher over the course of a few successive cycles until the losses per cycle equal the energy imparted by my push on the pendulum each time it momentarily stops just next to my hand.

Both of these mechanical systems (the spring with a mass and damper and the pendulum) are second order and are under damped and so both exhibit *resonance*. The pendulum is an example of simple harmonic motion because the force I impart on the pendulum with my hand each time it swings towards me is proportional to the distance through which the pendulum swings or, equivalently, proportional to the losses experienced by the pendulum per cycle. A suitable analogy to these systems is a parallel RLC filter network. We will need to return to resonance a little later on in this answer.

Emptying tank of water – a first order example Not all systems are second or higher order however. Some systems are first order and do not exhibit resonance. For example suppose we fill a sink with water. Suppose for simplicity that the sides of the sink are vertical and the bottom is horizontal with the plug hole in some suitable location in the bottom of the sink. Since the sink has been filled the plug must be "in". Gravity exists. Suppose, in advance of filling the sink we stand a ruler in the sink and fix it somehow either with some kind of stand or

perhaps by gluing it to the inside of one of the walls of the sink so that we can read the depth of water at any given moment. Also we need to assume the water is in-compressible – which is, broadly speaking, not a bad assumption and that temperature is constant throughout.

Suppose I note the initial height of the water and then pull out the plug. Initially the water leaves the sink quickly because the mass of water pushing down on the water in the mouth of the plug hole is large and this creates a pressure on the water in the mouth of the hole. The pressure is converted to kinetic energy. Suppose energy is conserved between potential and kinetic forms meaning that none of the potential energy that exhibits itself as pressure is converted into any other form. For example we must presume that this whole experiment happens in silence as pressure to acoustic waves would break our very specific rules of conservation of energy. The water leaves the plug hole because it now has kinetic energy and, for the sake of argument, I will catch it in a bucket or risk getting wet feet. I note the time at which half the water is gone, then again at the time a quarter remains and then an eighth etc. until all the water is gone. Suppose I then plot a graph of water height as a function of time. The rate of flow of water decreases exponentially with time. It does so because, after a short time of water flowing, there is less water pushing down on the water in the mouth of the plug hole so it runs out slower (gains less kinetic energy from the pressure). The more empty the sink becomes the slower the water runs out of the plug hole. This system is first order like an RC or RL filter network.

The relationship between physical systems in which energy is transferred and very probably transformed from one expression of energy to another (e.g. electrical to acoustic, pressure to motion, electric current to thermal etc.) and the poles and zeros of that system is quite direct. Each physical system has a transfer function which describes the behaviour of the system. Often for electronic and electrical engineers we use the frequency domain to write these transfer functions but we can use the method of Laplace transforms or direct inspection methods to work in the time domain if necessary. Some problems make more physical sense when viewed in the time domain but others are more amenable to explanation if we consider the frequency domain. With some practice it should be possible to look at data from one domain and interpret it such that you can tell what the system's response would be in the other domain. The transfer functions we deal with in continuous time systems (i.e. ones that exist in the real world as opposed to ones that we create in a digital system where time moves in finite (discrete) steps) make use of complex numbers. We commonly represent these as s which is equal to $\sigma + \mathrm{j}\omega$. To appreciate how poles and zeros relate to the work of an engineer we must fist have a good grounding in the field of *complex analysis*. This can be obtained by working through the relevant chapters in the books by Stroud and Booth or the books by Glyn James. It is *unavoidable* that

candidates must at some point understand and be able to do all the maths they might need to perform the engineering work and to be able to, in the future, teach themselves anything they find they need to know but which presently lies beyond their knowledge. Even if they do forget some things they never use along the way, they must be able to re-learn it at will and with only a little effort. There isn't time, space or willpower of the author, to provide a full treatment of the maths needed here, but it can not be avoided.

Let's suppose that we are all happy with the maths but are still clueless to the physical meaning of a pole and a zero. This is totally possible, probably the most common situation. It was for me when I was a student. I was clueless on the maths front too for quite a while, see section 1.4. Under this supposition we propose a system with a transfer function,

$$\frac{v_o}{v_i} = \frac{10}{100 + s} \tag{8.17}$$

It could be realised using an op-amp circuit with $A_v = \infty$ and frequency dependent feedback (by using a capacitor and a resistor as feedback components) or it could just be a passive RC circuit driven by a reasonably high source resistance but it does not matter how it is realised. It is more common for us (electronic engineers) to write this as,

$$\frac{v_o}{v_i} = \frac{0.1}{1 + s \cdot 0.01} \tag{8.18}$$

but for the discussion we are having now the form of (8.17) will probably be found much easier to work with. Looking at (8.18) however we can say fairly quickly that it is first order because the highest power of the polynomial in s of the denominator is 1. We can say it is low pass because the highest power of s in the polynomial of the numerator is 0. $s^0 = 1$ this works for anything raised to the power zero. The general form of a quotient of two polynomials in s is,

$$k \cdot \frac{c_{n_0}\, s^0 + c_{n_1}\, s + c_{n2}\, s^2 + c_{n3}\, s^3 + ... + c_{n_n}\, s^n}{c_{d_0}\, s^0 + c_{d1}\, s + c_{d2}\, s^2 + c_{d_3}\, s^3 + ... + c_{d_n}\, s^n} \tag{8.19}$$

Where c_{n_x} is the coefficient of the term in s who's index is an integer x and c_{d_x} is a similar term in the denominator.

We also know (8.18) obeys causal rules i.e. the flow of time and the incapacity of information to pass from the future into the present. We know this because the order of the numerator is less than or equal to the order of the denominator. We know that the frequency independent gain is 0.1 because the numerator can have k taken out to leave only s^0 on top of the fraction and a $k = 0.1$ multiplying the fraction. i.e.,

$$\frac{v_o}{v_i} = 0.1 \cdot \frac{1}{1 + s \cdot 0.01} \tag{8.20}$$

So we know a reasonable amount. If we so choose we can perform the inverse Laplace transform to get the time domain response or we can just recall that first order systems obey an exponential shape, or determine by circuit analysis a differential equation as a function of time that describes the system and then solve it either using Laplace techniques or by using a general solution and initial conditions i.e. a specific solution. There are several types of first order system, low pass, high pass or pole zero. Ultimately though HP and LP work on the same phenomena, PZ is a combination of these two. When driven by a step or a square and that the denominator coefficient of s^1 when the denominator s^0 term has no coefficients is the *time constant*, τ and the system will have reached $\frac{1}{e^1}$ of its final value in this time. We also know that in the frequency domain the phase shift of this system will be -45° at a frequency of $\frac{1}{\tau}$ (this is in radians/second not Hz divide by $2\,\pi$ to work in Hz). We know that the magnitude response will be -3 dB below the value of k at the frequency associated with the time constant. In short, the transfer function and the analysis tools at the disposal of the engineer tell us everything we want to know about the system. I know that this system will have all these features because it is first order and all first order systems present these features just as surely as all bears love fish and honey. We can learn the features of systems from a book (or from professor Google if we're careful about what we believe on the Internet) or we can investigate with a pad and pen(s) and Matlab/Maple or SPICE to see what common features circuits with certain transfer functions present, we could even go into the lab and measure some circuits we know to be first order until we find common things about them all. That's all these features are, things that are common to all first order systems. If I had a picture of an Owl, and you'd never seen a bird before and I outlined some key salient features on the picture: beak x1, feathers, wings x2, legs x2, talons, eyes x2 etc. and then showed you a chicken you'd probably correctly conclude it was a bird, even though it can't fly properly and doesn't look the same as an Owl. By the same method we can identify systems by their features even if their physical implementation varies (circuits & electronic systems, kinematic systems, hydraulic systems, pneumatic systems, optical systems etc.).

8.4.2 The s-plane

Returning to our original form (8.17), suppose we plot a 3D graph where one of the horizontal axes is the real part of s, (σ) and the other horizontal axis is the imaginary part of s, ($\mathrm{j}\,\omega$) and the third, vertical axis is the value of the function ($\frac{v_o}{v_i}$). We should be able to predict what we will see.

The poles of a transfer function exist at the frequencies required to make the denominator of the transfer function become zero. They are the roots of the denominator polynomial.

So we must ask, how can I solve,

$$100 + s = 0 \tag{8.21}$$

By inspection, $s = -100$. There is a pole at $s = -100 + \mathrm{j}\,0$. The imaginary part is explicitly included, even though it is zero in this case, to make clear that frequency is complex, it has a real and imaginary part σ and $\mathrm{j}\,\omega$. This is because it exists over the field of complex numbers but that's a bit like saying "it is, because I say so", it doesn't really help. If you want the mathematical interlude it's in section 8.4.5.

Since the denominator of (8.17) will fall to zero at $s = -100 + \mathrm{j}\,0$ we should expect the value of $\frac{v_o}{v_i}$ to tend towards infinity around this frequency. This is because $\frac{1}{0} \to \infty$ The plot is shown in figure 8.1 and it does show a single pole on the real axis at -100.

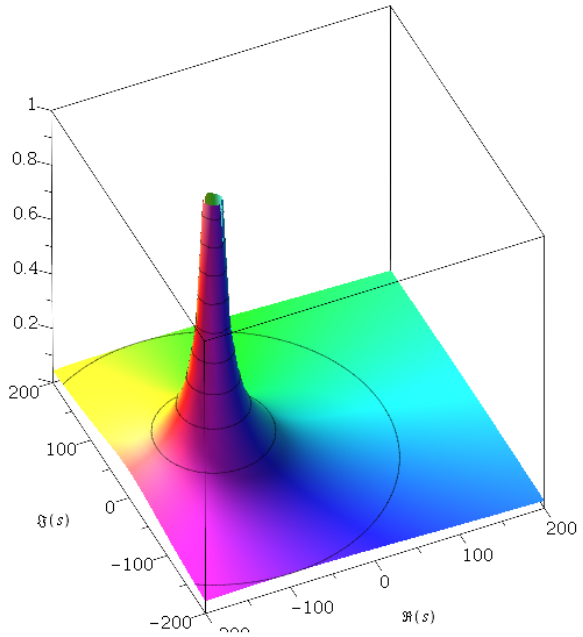


Figure 8.1: plot of (8.17) as a function of the real and imaginary components of frequency. σ is on the broadly left – right axis and $\mathrm{j}\,\omega$ is on the broadly front – back axis. The value of the function is on the vertical axis.

These 3D plots are not very easy to interpret however and engineers, especially electronic and control systems engineers, have a 2D plot that conveys the information in a much more useful way which we will use shortly. First however let's consider a more complicated system,

$$\frac{v_o}{v_i} = \frac{40 + s}{60 + s} \cdot \frac{40\,s}{s^2 + 40\,s + 1000} \tag{8.22}$$

This system is composed of a first order pole zero system and a second order band pass system (s^1 in the numerator). If we expand the numerator and denominator we should expect to find s^3 in the denominator and therefore expect 3 poles. We should find s^2 in the numerator and so expect two zeros. The 3D plot is shown in figure 8.2. We have three poles. One at $-60 + \mathrm{j}\,0$ and a conjugate pair at $\left(-20 + \mathrm{j}10\sqrt{6}\right)$ and $\left(-20 - \mathrm{j}10\sqrt{6}\right)$. $10\sqrt{6} \approx 24.5$. We also have two zeros.

Just as the poles are the roots of the polynomial in s in the denominator of the transfer function,

the zeros are the roots of the polynomial in s in the numerator of the transfer function.

Since the numerator falls to zero at the frequencies where the zeros exist the value of $\frac{v_o}{v_i}$ will become very small around these frequencies eventually becoming nothing at the frequency of the zero.

The two values of s that will make $40\,s = 0$ and $40 + s = 0$ are $s = 0$ in the first case and $s = -40$ in the second case. So we have a zero at the origin. This happens to be a zero at DC (no frequency or $f = 0$ if you prefer) and is not uncommon. Poles at the origin are also possible and are required to make a continuous time system which includes an integrator ($1/s$). This could be an op-amp circuit for some analogue computer or could be something control based like an analogue PID controller for example. Looking at figure 8.2 we can see two minima at the locations calculated. These are the zeros although they're quite hard to see.

Because this plot is of quite limited utility we usually present this information as a pole zero plot, but it's sometimes called a "root locus" plot by control systems types. This is shown in figure 8.3 and is much more amenable to inspection. The poles are crosses and the zeros are, well, zeros.

It is the case, although there is no need to dwell on it now, that causal systems only have poles with zero or negative real parts. It is also the case that many (perhaps even all, I've not thought about it very hard) oscillators maintain a non-zero and non-clipped output voltage by moving their poles, often a conjugate pair, such that they have a zero real part and a $\pm$ non zero imaginary part. This is often done by adjusting the gain of an amplification stage using a nonlinear component like a JFET or a light bulb, see section 10.1. The ideas surrounding the reaslisability and causality of systems, their convergence and if they are bounded will be discussed if you're taking digital signal processing, control theory and probably courses on communications systems (e.g. software defined radio etc.) modules at L3 and L4.

Hopefully this answer will have provided some feeling for what the poles and zeros are without just re-stating the mathematics from textbooks. The next question

and answer continues the discussion in a more practical way.

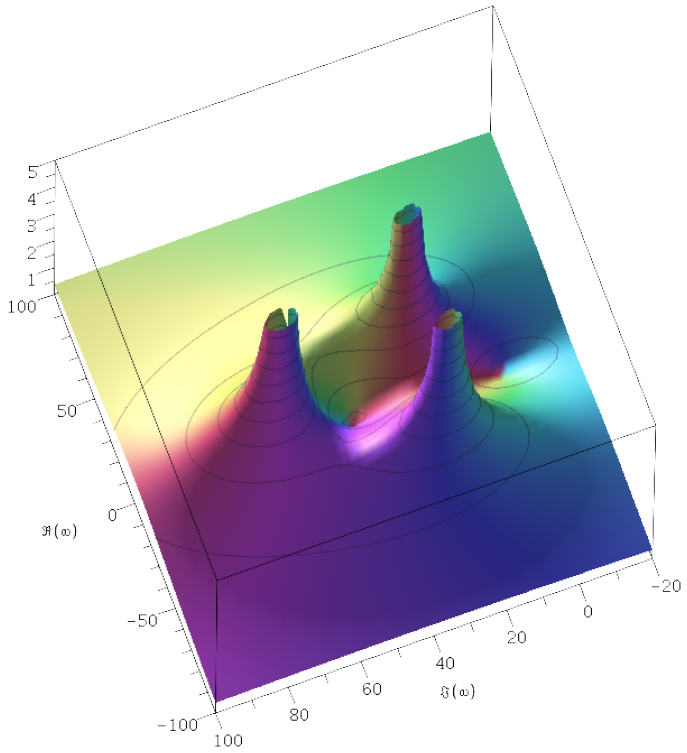


Figure 8.2: plot of (8.22) as a function of the real and imaginary components of frequency. Maple has swapped the labels on the real and imaginary axes. I don't know why.

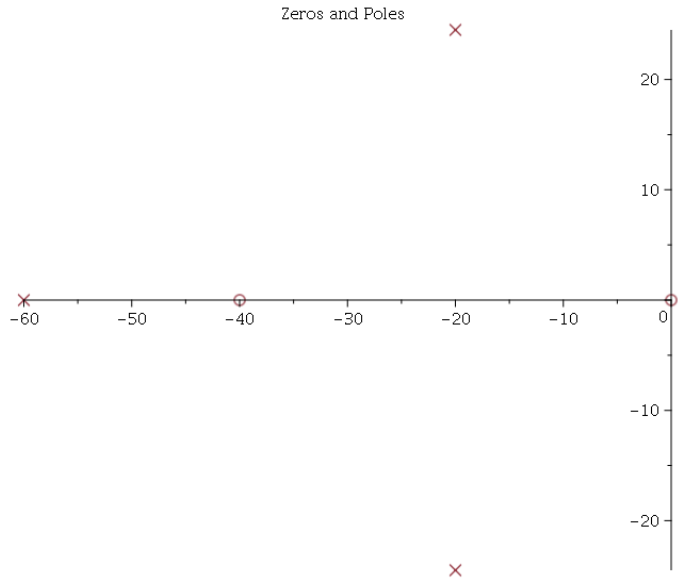


Figure 8.3: plot of (8.22) as a function of the real (horizontal) and imaginary (vertical) components of frequency.

8.4.3 What is the significance of the poles and zeros in terms of the behaviour of circuits and systems?

How do I read and interpret a bode plot to find out the poles and zeros of a system?

Practically speaking, the trick with the poles and zeros is to have a look at a bode plot and work your way from low to high frequencies thinking about the standard responses of first and second order systems and remembering that higher order systems can be made from these two.

Example with a first order system

Have a look at figure 8.4 which yields the AC response shown in figure 8.5 when the voltage across the series combination of R_3 and C_2 are the output. Then consider the following description of what we observe

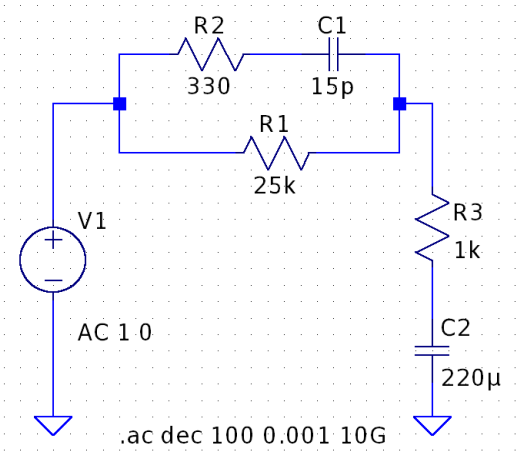


Figure 8.4: Dual pole-zero circuit schematic

We start from the left having a flat response. It doesn't last long though and the phase is quickly lagging. It started from 0° aiming for -90° (i.e. 90° lagging) but it doesn't make it all the way. The magnitude is dropping too and the gradient is -20 dB/decade. You'll need to measure only the straight part of the gradient and then infer what the value is per decade as there is less than one decade available to make the measurement. This information should cause you to conclude that a pole was passed at some point and you will note that the pole exists at the frequency where the magnitude is -3 dB compared to the low frequency value and where the phase is -45° or 45° lagging. By measurement in SPICE I have the pole at about 30 mHz. I'm looking at the phase because it's changing rapidly with frequency and therefore is sensitive to the thing I care about.

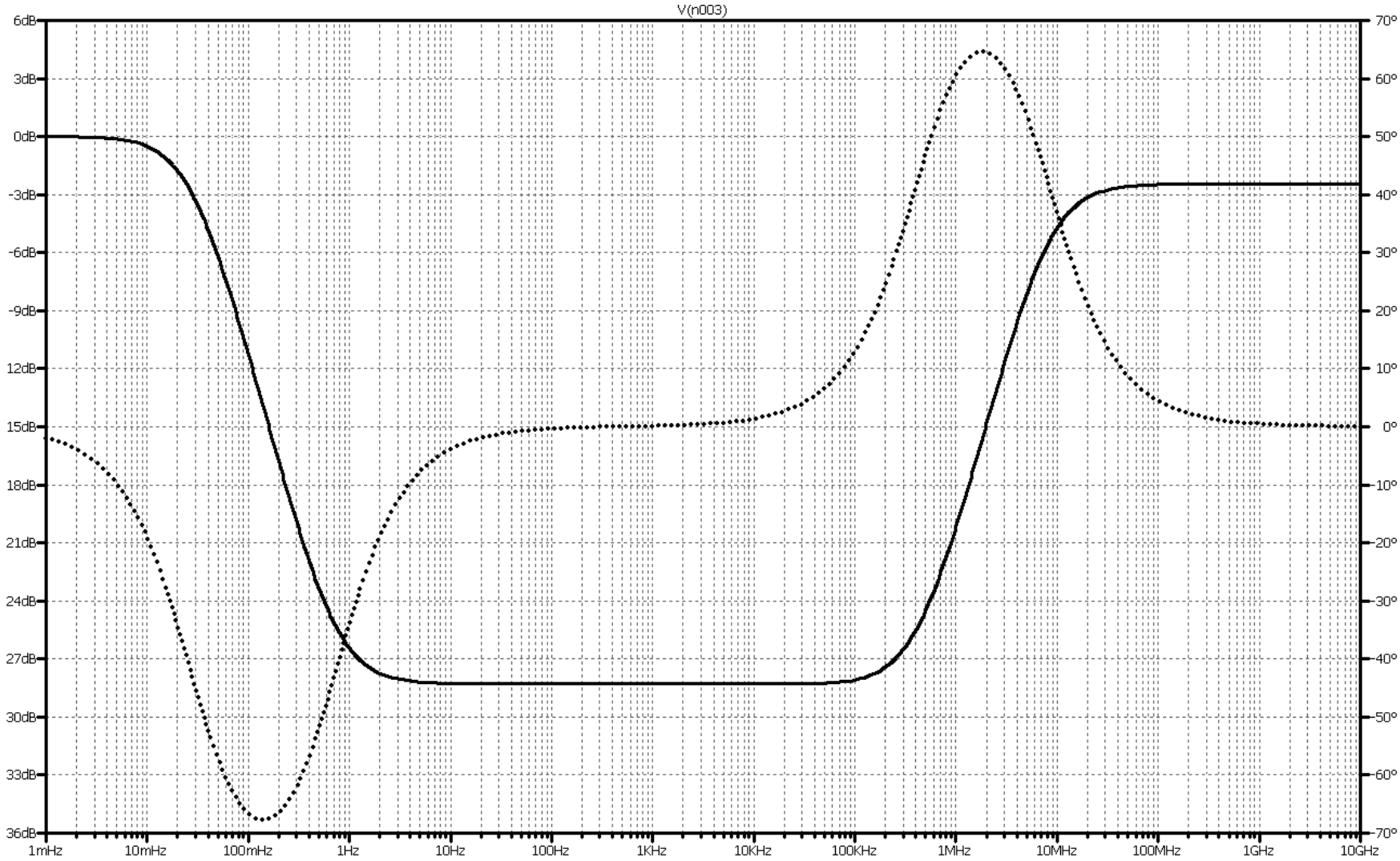


Figure 8.5: Dual pole-zero circuit AC response

As we continue we find that the phase starts heading back towards 0° and that the magnitude levels off at about -28.3 dB. The phase is heading from -90° (even though it was never at that value it's the value it was aiming for due to the pole at 30 mHz) towards 0° which is an overall lead of 90° (or +90° if you prefer). We also find the magnitude changes from -20 dB/dec to 0 dB/dec which means that +20 dB/dec was added to the magnitude. This all indicates that we passed a zero and if we find where the phase was -45° (because we are going from -90° to 0°) we see that the zero is around 660 mHz the magnitude is about 3 dB above the minima then too.

Moving to even higher frequencies we find a change of gradient of the magnitude towards +20 dB/decade and an additional phase lead from 0 to 90° (although once again it never makes it all the way). These are the effects of another zero and using the phase again its frequency is around 476 kHz.

At yet higher frequencies still we find that the magnitude response no longer increases at 20 dB/dec but has returned to flat or 0 dB/dec we also observe a return of the phase shift to 0° (this is from +90° which is what it was aiming for after we passed the zero at 476 kHz, but, again, it didn't make it all the way on that occasion). So we have a phase lag of 90° (-90°) and a change in slope of -20 dB/dec. These observations are consistent with the existence of a pole. Looking at the phase shift the pole is at 7.3 MHz and the magnitude is -3 dB compared to the magnitude at very high frequencies. Note that the magnitude does not return to 0 dB it has a constant high frequency loss of approximately -2.5 dB.

To see why the HF loss takes that value simply short out all the capacitors and open circuit all the inductors (although there are none in this example). We have 330//25 k in a potential divider with 1 kΩ.

$$\frac{330 \cdot 25000}{330 + 25000} \approx 325.7 \tag{8.23}$$

$$\frac{1000}{1000 + 325.7} \approx 0.7543 \tag{8.24}$$

$$20 \cdot \log_{10}(0.7543) \approx -2.4489 \text{ dB} \tag{8.25}$$

All this numerical stuff is "approximately equal" because I maintained greater precision in the intermediate stages than I have written out in this text. Someone re-running the numbers and only using the precision I have written out would probably run into problems with rounding errors.

To see why the LF loss is 0 dB short out all inductors and open circuit all capacitors. C_2 is open so there is no current in the circuit. If there is no current

there can be no voltage drop across the resistors ($V = I \cdot R$) and since there is no voltage drop across the resistors the output voltage must be the same as the input voltage (i.e. 0 dB).

The "rules" for interpreting the the bode plot are then,

Poles every time we pass a pole we must ultimately find ourselves aiming for an additional $-90°$ phase shift with an additional $-45°$ at the pole frequency. Also at the pole frequency the magnitude will be an additional -3 dB compared with frequencies far from the pole. Moreover the slope of the magnitude plot tends to an additional -20 dB/decade slope at frequencies higher than, and some distance from, the pole.

Zeros every time we pass a zero we must ultimately find ourselves aiming for an additional $+90°$ phase shift with an additional $+45°$ at the pole frequency. Also at the zero frequency the magnitude will be an additional +3 dB compared with frequencies far from the zero. Moreover the slope of the magnitude plot tends to an additional +20 dB/decade slope at frequencies higher than, and some distance from, the zero.

The network in figure 8.4 takes the form,

$$\frac{v_o}{v_i} = \frac{(1 + s\,\tau_3)\,(1 + s\,\tau_2)}{(1 + s\,\tau_1)\,(1 + s\,\tau_0)} \tag{8.26}$$

and is not one that we have directly studied in EEE225 but it is not such a leap to see that it is two first order pole zero responses combined (multiplied) together. LTI systems that are placed in series with each other have their transfer functions multiplied together. Having this information it should not be beyond the wit of an L2 candidate to solve the network for its transfer function and find the time constants to see how close my measurements in SPICE were. Of course you could write (8.26) as,

$$\frac{v_o}{v_i} = \frac{A\,s^2 + B\,s + C}{D\,s^2 + E\,s + F} \tag{8.27}$$

by expanding the brackets but we do not commonly do that unless the system is *irreducibly* second order and in this case I know they are all real poles. First order systems *always* have real poles and real zeros and this system is a high order system composed of several first order systems. Second order systems can sometimes have real poles (and zeros) but it is not necessarily so. It is not easy to prove that a particular system or circuit/network should have a particular form. The common method is to do the circuit analysis and try to make the transfer function fit one of the standard forms and see where it leads you. If you can not make it fit then it may not be the correct interpretation of the system. We will see an example of this later.

One might then wonder how would I know if I had two complex poles or zeros at the same frequency on a bode plot? To answer this we could use a second order example. But even without a specific example we can say that the phase would give it away and so would the resulting change in slope of the magnitude plot. We should expect to see an aim for 180° shift overall and a 40 dB/dec change in magnitude (which could be +20 dB/dec to -20 dB/dec for example as is the case in a second order band pass or 0 dB/dec to ±40 dB/dec in the case of second order high pass or low pass or any other arrangement e.g. -60 dB/dec to -100 dB/dec for example if we'd already passed 3 poles on our way to a pair of poles).

Example with a second order system capable of resonance

Take the example of a familiar second order circuit. Figure 8.6 shows the collector circuit of a transistor π model (a controlled current source) set up for AC signals and being connected to a parallel LCR network. The input is the current in the "collector" of the transistor – of course we need not model the base and emitter since we only care about the current flowing in the collector network and the resulting voltage across that network. This circuit is used as the load of both of the cascode gain stages in the first year individual construction project, so it is familiar even if it doesn't at first appear to be.

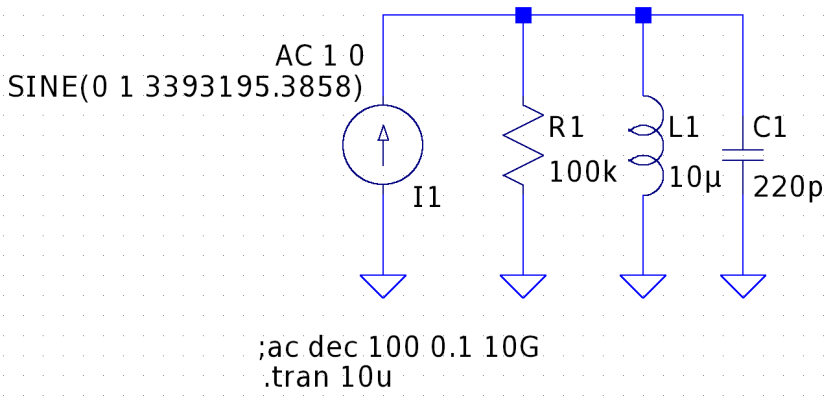


Figure 8.6: Second order parallel LCR circuit driven by a current source which represents the collector – emitter branch of a hybrid–π model. This may be found in the first year individual construction project.

If we derive the transfer function we can arrive at,

$$\frac{v_o}{i_i} = R \cdot \frac{\frac{s\,L}{R}}{1 + \frac{s\,L}{R} + s^2\,L\,C} \equiv k \cdot \frac{\frac{s}{\omega_o\,q}}{1 + \frac{s}{\omega_0\,q} + \frac{s^2}{{\omega_0}^2}} \tag{8.28}$$

where R is the frequency independent gain. $\omega_0 = \frac{1}{\sqrt{LC}}$ and q is found using the identity $\frac{1}{\omega_0 q} = \frac{L}{R}$ which arises by comparing the denominator term in s^1 with the standard form for a second order system).

Suppose we simulate some values in the frequency domain. Let's have $R = 10\ \Omega$ and $R = 10\ \text{k}\Omega$, $L = 10\ \mu\text{H}$ and $C = 220\ \text{pF}$. This yields four plots (two of magnitude and two of phase) shown in figure 8.7 in the form that a rather old school spice incarnation kicks out. The reason I've gone all dot matrix is that LTSpice, while being generally brilliant, does not implement all of the Berkeley SPICE functions. I want to use the `.pz` directive. The function of this directive is to find numerically the poles and zeros of a system after using an AC simulation.

These graphs in figure 8.7 should indicate to you that, in second order networks (circuits) or systems, poles and zeros can change from real to complex or complex to real based on the values of the components in the network. Since we know that a real number is just a complex number with a nil imaginary part we might just say that the poles and zeros can change the magnitude of their real and imaginary parts based on the values of the circuit components as this is more general and means the same thing. Higher order networks can usually be treated as a combination of first and second order systems. This changing of the nature of poles and zeros is one of the reasons that it's not easy to look at a network and say what its response is likely to be based only on its topology (circuit shape). Certainly, if there are three energy storage components in the network then it will have s^3 in the denominator but how should I try to factorise that s^3 when doing the maths?

If you don't see it in the graphs do not panic. In the top graphs we have no resonance. This is because the energy needed to be stored between cycles can not build up (more on this later) because R is too small and the energy leaves the network as heat in the resistor. On the graph the maximum value of the magnitude in dB is +20 dB which is 10 in linear. This is the frequency independent gain and has the units Ohms because the transfer function is the quotient of output voltage and input current. Looking at figure 8.6 we can choose to "ignore" the frequency dependent components. In this case we open circuit them both in the mid-band which is a little unusual. Essentially we are at a set of frequencies where the inductor's impedance has risen considerably above the resistance of the resister so it plays no part, but the frequency is not yet high enough that the impedance of the capacitor is sufficiently low as to be comparable with the resistance of the resister so it too plays no part and only the resister is significant. This *feels* right as the resistance is the only one that is frequency independent. The resistance is 10 Ω which is in good agreement with the magnitude in the mid-band. The phase shows two distinct but somewhat overlapping effects one moving from +90 to 0° and the other from 0 to -90°. The magnitude is its highest

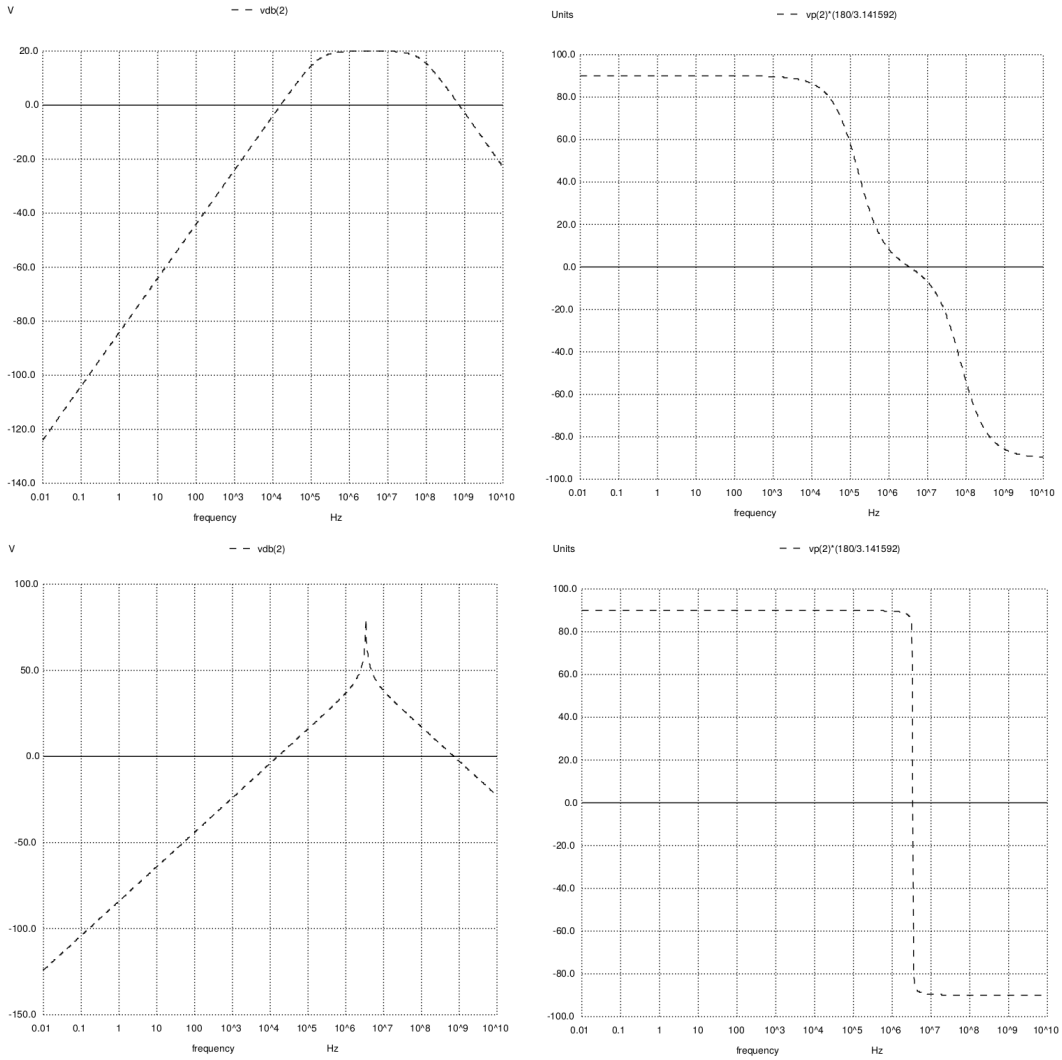


Figure 8.7: Top Left: AC magnitude and Right: phase response plot of the circuit in figure 8.6 where $R = 10\ \Omega$. Bottom Left: AC magnitude and Right: phase response plot of the circuit in figure 8.6 where $R = 10\ \text{k}\Omega$. The axes tick labels are a bit small but I presume in modern times this document will be read electronically and it will be possible to zoom in and out.

value (+20 dB) at approximately 3.38 MHz, it very slightly decays on either side of this value. The magnitude is -3 dB down at 158.5 kHz and 72.44 MHz and the phase shift is +45° and -45° respectively at these frequencies. At 3.38 MHz the phase shift is 0°. Away from the poles the slope of the magnitude plot is +20 dB/dec before the first pole, 0 dB/dec after the first pole and -20 dB/dec after the second pole. The change due to each pole is therefore -20 dB/dec and we have 40 dB/dec change in magnitude overall and 180° change in phase overall. So this second order system behaves like two first order systems that have been connected together. This may be counter-intuitive but it is not very surprising when we consider the evidence. The poles have only real components, just as first order systems do. We can figure out the pole placement on the bode plot but SPICE's .pz command yields poles and zeros with only real parts (in units of radians/second) and can put our mind to rest if we are confused,

```
Circuit:  Pole Zero Example R = 10
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning:  i1:  has no value, DC 0 assumed
No.  of Data Rows :  1201
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning:  i1:  has no value, DC 0 assumed
No.  of Data Rows :  1
pole(1) = -4.54535e+09, 0.000000e+00
pole(2) = -1.00002e+05, 0.000000e+00
zero(1) = 0.000000e+00, 0.000000e+00
```

Now suppose we make R = 10 kΩ in the example, but keep the inductor and capacitor the same. Energy is now dissipated from the network more slowly and resonance is felt strongly. This results in a high voltage measurement in the time domain and a big spike in the frequency domain at that frequency with *ultimately* 40 dB/decade change in magnitude slope and a quick phase shift too, running to a total change of 180°. Which is the same as before when R = 10 Ω. When $R = 10$ kΩ we have energy stored in the capacitor's electric field and the inductor's magnetic field across several cycles of the driving waveform and exchanged between the capacitor's electric field and the inductors magnetic field. Looking at the graphs in the lower part of figure 8.7 we still a zero at 0 Hz but the real poles have gone and we now have a pair of conjugate poles. The real part is the same and the imaginary parts are the same but with opposite sign. This is evidenced by the very sharp change of phase from +90° to -90° and the abrupt change in slope of the magnitude plot from +20 dB/dec on one side of the resonance to -20 dB/dec on the other side of the resonance. SPICE's .pz has this to say (still in radians/second),

```
Circuit:  Pole Zero Example R = 10k
```

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning:  i1:  has no value, DC 0 assumed
No.  of Data Rows :  1201
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Warning:  i1:  has no value, DC 0 assumed
No.  of Data Rows :  1
pole(1) = -2.27273e+05, 2.131886e+07
pole(2) = -2.27273e+05, -2.13189e+07
zero(1) = 0.000000e+00, 0.000000e+00
```

So the first value of R shows two real poles and the second value of R a pair of conjugate poles. It's the same circuit but with different values of R. The values provided by SPICE's .pz analysis are consistent with the AC plots shown in figure 8.7.

The two real poles do not disappear as the value of R increases from 10 Ω to 10 kΩ. They *move*, that is to say their frequency changes as the component values change. The two real poles head towards each-other, one goes up in frequency the other down, as R falls in value, until the poles meet and then they change from two real poles into a conjugate pair. Thereafter, their real part stays the same but their imaginary part gets bigger. In some circuits, especially those with gain (i.e. involving op-amps or transistors) the imaginary part of a pair of conjugate poles can reach a maxima and then decrease after a certain frequency but it depends on the specifics of the situation. The value of R that is just right to allow the poles to meet and have the same real part but not have an appreciable imaginary part is the value at which the same amount of energy is added per cycle as is lost (with a factor of $2\,\pi$ involved) and in this situation the system is critically damped, $q = 0.5$. In this situation the circuit has one pole on the real axis with a *multiplicity* of 2, or, if you like, it has two real poles with the same frequency. This effect, where poles meet and change from real to conjugate or vice versa is not always possible, it depends on the network topology. Some second order circuits, who's poles are always real, are therefore *incapable* of resonance. Should they still be called second order? Yes, they should, because the expanded polynomial in s of their denominator has degree 2. An example of this is a first order low pass followed by a first order high pass. It is not possible for more energy to be stored than is lost per cycle in this network so it can never exhibit resonance.

In that case, when I have R less than the magic value that makes the system critically damped and enables resonance, and my second order system has two real poles, should I try to use a standard form like (8.29)?

$$\frac{v_o}{v_i} = k \cdot \frac{A\,s}{(1 + s\,\tau_1)\,(1 + s\,\tau_0)} \tag{8.29}$$

Well, try it and see how you get on. You need to find some algebraic expressions involving R, $s\,L$, and $\frac{1}{s\,C}$ and preferably without using a radical ($\sqrt{\ }$) because when we use a radical there is always a chance of a negative number appearing under it, and upsetting us, by forcing a j into existence. To save you some effort (and continue the discussion) the form you're looking for in the denominator is (8.30) and I broke my rule about radicals.

$$\left(s - \frac{L - \sqrt{-4\,C\,L\,R^2 + L^2}}{2\,C\,L\,R}\right)\left(s - \frac{L + \sqrt{-4\,C\,L\,R^2 + L^2}}{2\,C\,L\,R}\right) \tag{8.30}$$

I'm also not entirely certain that the A in the numerator turns out to represent anything very meaningful. I've not bothered to toy with it too much. This is not generally considered a desirable form but it does illuminate how the poles go from real to complex as a function of the value of R. Look at the radical, when the component parts of first term under the root become larger than the L^2 term then the overall sign of the expression under the root will become negative and a j will have to appear outside the root to allow us to evaluate it. It should also strike you that I arrived at that formulation by using the good old equation for the roots of a quadratic that appears at GCSE in the UK (well it used to anyway).

This form, (8.30), is not considered desirable because it doesn't allow us to easily find the circuit component values (R, L and C) that will result in a certain response shape i.e. a certain value of ω_0 and a certain value of q or *vice versa*. These parameters ω_0 and q are features of a second order system in just the same way as the time constant τ is a feature of a first order system. When we write out our transfer functions we want to do it in a way that will expose the features of the system that the transfer function describes. So we will use the standard form of (8.28) to write out the transfer function of our second order band-pass system and we will know quickly what the values of ω_0 and q are in terms of R, L and C by comparing the transfer function we derive in its correct form (with the s^0 term having unity coefficients in the denominator and the numerator) to the standard form for that kind of second order system. It is by this method that I know that for this parallel RLC circuit the q is determined by R & L but if I used a series resonant RLC I might find that it's different. I could design a filter with a particular q and a particular resonant (or perhaps I should say "centre" or "natural") frequency by using the equations in these forms. I couldn't do that nearly as easily if I used (8.30). Just because a circuit doesn't exhibit resonance doesn't mean we can't say that it has a "resonant frequency". In fact some circuits are resonant at all frequencies, they are sometimes called "image filters" – but I will not inflict such a circuit on you now. They have nothing at all to do with image processing or machine vision.

Instead of a tricky image filter it may be useful to consider a second order network which can not exhibit resonance. One possible example which may be familiar to candidates working on audio circuits is a first order high pass followed by a first order low pass combination with corner frequencies set to span the audio range (20 Hz to 20 kHz) and be -1 dB down at those frequencies (-3 dB at about 10 Hz and 40 kHz). The general scheme of a ladder filter, of which this is a kind, will not be unfamiliar to those working in communications or microwave circuits either. The circuit is shown in figure 8.8. The magnitude and phase plot should be reasonably easy to visualise because the -3 dB frequencies are provided and the topology is fairly simple.

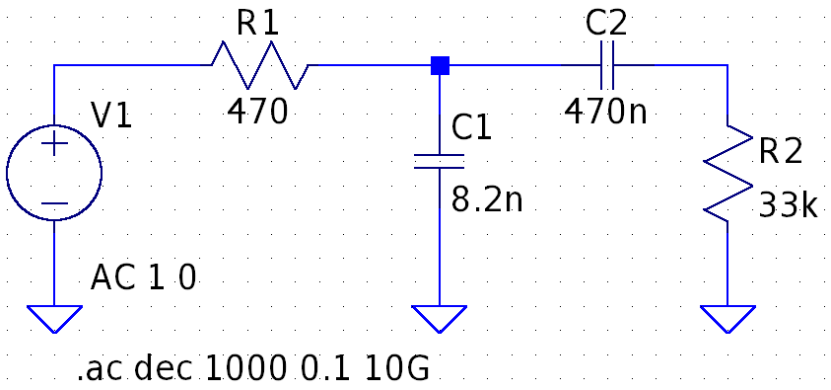


Figure 8.8: A first order high pass circuit followed by a first order low pass circuit forms a second order circuit which is incapable of resonance.

The transfer function, presuming the output is a voltage, taken across R_2 with respect to ground is given by (8.31)

$$\frac{v_o}{v_i} = \left(\frac{1}{1 + \frac{R_1}{R_2} + \frac{C_1 R_1}{C_2 R_2}} \right) \cdot \frac{s\ (R_1\,(C_1 + C_2) + R_2\,C_2)}{s^2\,C_1\,C_2\,R_1\,R_2 + s\ (R_1\,(C_1 + C_2) + R_2\,C_2) + 1} \tag{8.31}$$

Since it's two first order networks placed one after the other, is it possible to find a form similar to (8.29) in which no radical is required and the time constants are *independent* of each other? It is not possible. The networks interact with each other or put another way the second network *loads* the first to some extent. That is to say the "driving point impedance" that is seen looking out of the upper node of C_1 will be a function of R_1 *and* R_2 because R_2 can conduct a current to ground and R_1 can conduct a current to ground via the source (which we switch off and replace with its internal impedance because when we work out driving point impedances we are effectively doing superposition). It's possible to devise other arguments to show that the two networks interact but that's the one I like. The transfer function shows it too. If the network was a combination of first order systems it would have the response of (8.32)

$$\frac{v_o}{v_i} = \frac{R_2}{R_1 + R_2} \cdot \frac{1}{(1 + s\,R_1\,C_1)} \cdot \frac{s\,R_2\,C_2}{(1 + s\,R_2\,C_2)} \tag{8.32}$$

If we multiply out i.e. expand (8.32) we find (8.33),

$$\frac{R_2}{R_1 + R_2} \cdot \frac{s\,R_2\,C_2}{1 + s\,(R_1\,C_1 + R_2\,C_2) + s^2\,R_1\,R_2\,C_1\,C_2} \tag{8.33}$$

Comparing the denominators of the frequency dependent parts we have an extra term in (8.31) which is $C_2\,R_1$. This term makes it impossible for us to find algebraic values of τ_1 and τ_0 in an equation where the denominator is of the same form as (8.29). If we attempt to factorise (8.31) we will end up in the same situation as with the RLC network from earlier where we have to use the quadratic formula or completing the square. This quadratic is said to be *irreducible* over the real numbers. See section 8.4.5 for the explanation of the meaning of this. The significance of this conclusion is that we can not treat this network as a combination of first order networks without introducing a simplification (a small and in some cases acceptable error).

How do we know there can never be resonance in this network? Well if we apply the quadratic formula

$$s = \frac{-b \pm \sqrt{b^2 - 4\,a\,c}}{2\,a} \tag{8.34}$$

where a, b and c are the coefficients of the original polynomial in s

$$a\,s^2 + b\,s + c \tag{8.35}$$

we need to show that the radical can not become negative i.e.

$$b^2 > 4\,a\,c = (R_1\,(C_1 + C_2) + R_2\,C_2)^2 > 4\,(R_1\,R_2\,C_1\,C_2) \tag{8.36}$$

provided this is true while R_1, R_2, C_1 & C_2 are all real and positive, this second order system can not exhibit resonance. It may help to remember that resonance requires a conjugate pair of poles. I leave the proof of (8.36) as a small challenge.

The SPICE I used here other than LTSpice is called ngspice. Binaries for common OSs and source code are available. Although, winspice is good for Windows if you can find a copy *and* make it run stable on a modern PC.

8.4.4 Can you explain what the significance of the quality factor, q, is?

Let's consider what will likely happen in the time domain when we simulate figure 8.6 because we need to have an understanding of what happens to the energy if we are to discuss second order systems and understand the phenomenology.

In figure 8.6 current flows in the inductor and capacitor and resistor and some is stored in the inductor and capacitor. The current in the inductor is 180° out of phase with that in the capacitor at the resonant frequency and it is this phase shift (it can be thought of as a time delay between the waveforms and therefore the stored energy if you wish) which allows energy to be transferred back and forth between the inductor's magnetic field and the capacitor's electric field thereby storing up energy over several cycles and apparently magnifying the voltage across the components considerably above that which one might expect to find. One might expect to find 106 V in the R = 10 kΩ case. This is obtained from 1 A flowing in the parallel impedance of the three components at the resonant frequency, R = 10 kΩ,

$$X_{\mathrm{L}} = 2\,\pi\,f\,L \approx 213\ \Omega \tag{8.37}$$

and

$$X_{\mathrm{C}} = \frac{1}{2\,\pi\,f\,C} \approx 213\ \Omega \tag{8.38}$$

The parallel impedance is then approximately 213/2 = 106 Ω and since 1 A flows we just apply Ohm's law yet looking at figure 8.9 (of which more shortly) we see nearly a peak voltage of nearly 4.7 kV across the RLC network.

In the 10 Ω case only 10 V may be expected. X_{C} and X_{L} have not changed because we keep the frequency the same yet R has dropped and now dominates the parallel combination of the three components. In the case of $R > X_C//X_L$ at resonance (≈ 108 Ω in this case) the network is under damped i.e. $q > 0.5$. In the case of $R < X_C//X_L$ at resonance the network is over damped i.e. $q < 0.5$ and for a critically damped ($q = 0.5$) second order system $R = X_L//X_C$ at the resonant frequency.

The key to resonance is that the *extra* energy stored due to the present cycle of the driving waveform adding energy to the system, is at least equal to the energy that's lost as heat in the resistor during this cycle. We will see later in (8.41) that when this condition holds with a factor of $2\,\pi$ involved then the system is critically damped. For the 10 kΩ case there is a large resonance effect and this can be simulated in SPICE. We can find the stored energy in the inductor,

$$E_{\mathrm{L}} = \frac{1}{2}\,L\,I^2 \tag{8.39}$$

and in the capacitor

$$E_{\mathrm{C}} = \frac{1}{2}\,C\,V^2 \tag{8.40}$$

and the energy lost in the resistor $I\,V$ as a function of time and plot them.

In the time domain we can watch these quantities build up over a few tens of cycles of the driving waveform which is very instructive in my opinion. Figure 8.9

uses $R = 10$ kΩ to provide a high q factor making the situation more apparent. The figure shows, in the lowest graph pane, the stored energy in the inductor's magnetic field (black) and the capacitor's electric field (blue). The units are Joules but LTSpice doesn't figure that out because it has no way of knowing the units of the inductance and capacitance which I have typed in manually. In the second graph pane from the bottom the power dissipation in the resistor is shown in red. In the middle pane the inductor current is shown in cyan and the capacitor current is shown in magenta. In the second from top pane the voltage across the resonant circuit with respect to ground is shown (in grey). In the upper-most pane the total stored energy in the resonant circuit is shown in blue (Joules on the right vertical axis) and the power added to the system from the current source is shown in green. This is the same as the red curve in steady state. It transpires that the current source supplies only the energy lost in the resistor if the system is in a steady state i.e. the quantities of voltage & current (and therefore energy) are oscillating (because they are sinusoidal or some function of sinusoids) but are the same in this cycle as in the one before and in the next one. That is to say the state of the system is steady (not changing) over successive cycles. When the system is first energised by the source then the source has to supply the current to charge the inductor's magnetic field, the capacitor's electric field and the energy dissipated in the resistor. This can be seen in the first two or three cycles where the green curve in the upper most graph pane (power entering the system) has a larger amplitude than the red curve in the second from bottom graph pane which is the power leaving the system as heat. If you set this up yourself in LTSpice don't forget to set the series resistance of the inductor to zero, LTSpice defaults to 1 mΩ ruining everything and possibly causing some confusion.

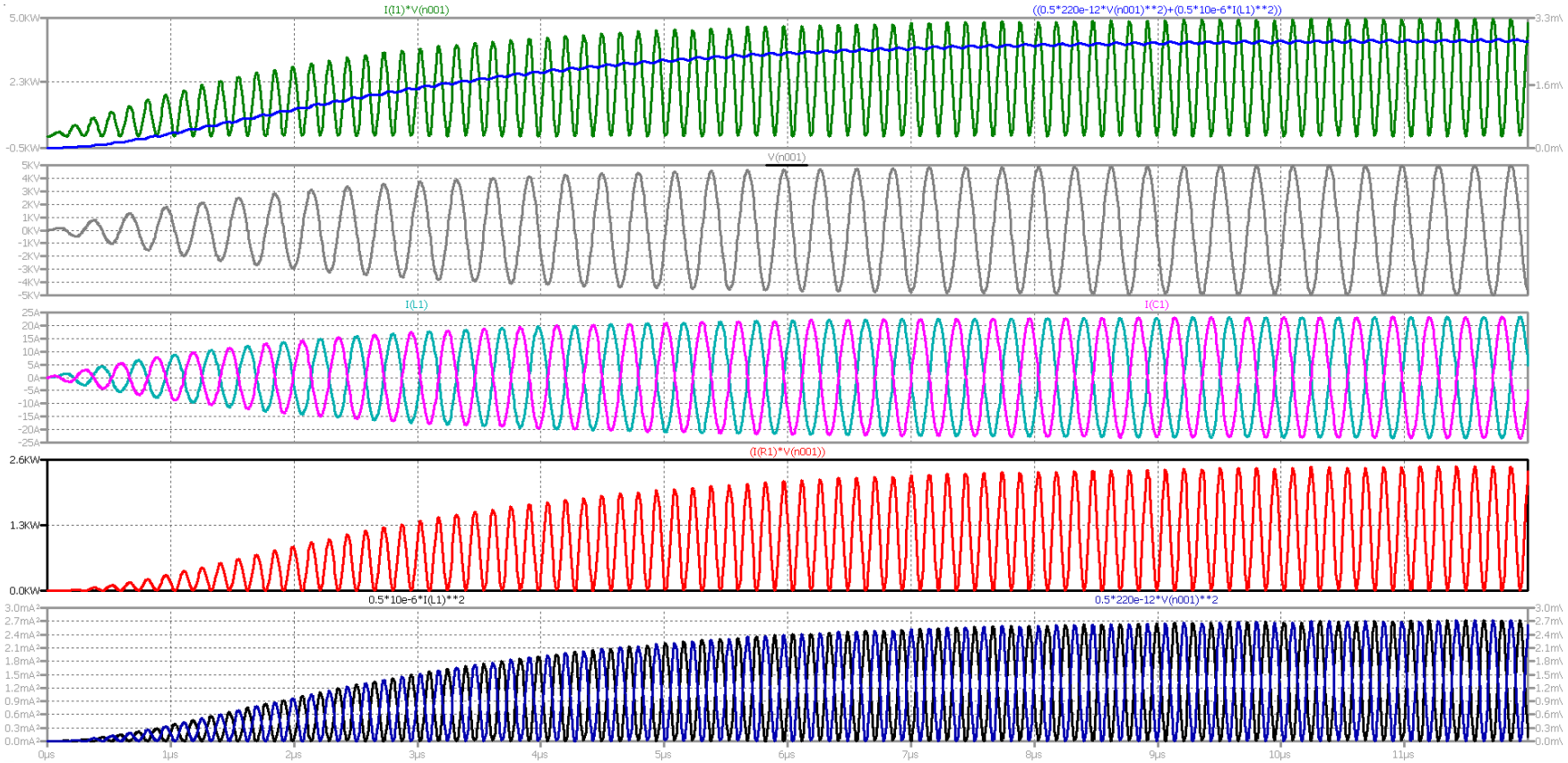


Figure 8.9: Time domain response of the parallel LCR network shown in figure 8.6 with $R = 10$ kΩ. in the lowest graph pane, the stored energy in the inductor's magnetic field (black) and the capacitor's electric field (blue). The units are Joules but LTSpice doesn't figure that out because it has no way of knowing the units of the inductance and capacitance which I have typed in manually. In the second graph pane from the bottom the power dissipation in the resistor is shown in red. In the middle pane the inductor current is shown in cyan and the capacitor current is shown in magenta. In the second from top pane the voltage across the resonant circuit with respect to ground is shown (in grey). In the upper-most pane the total stored energy in the resonant circuit is shown in blue (Joules on the right vertical axis) and the power added to the system is shown in green.

We can go further in the time domain and consider the definition of quality factor, the relationship between stored and lost energy.

$$q = 2\,\pi \cdot \frac{\text{Total stored energy in the network}}{\text{Energy lost from the network per cycle}} \tag{8.41}$$

Still using figure 8.9 we can take the average value of the total stored energy (blue solid line in the upper most graph pane) and the energy lost per cycle – this is a little more complicated but we can set the horizontal axis up to be only from 10 μs to 10.2947075 μs which is the length of time taken for one cycle at the resonant frequency. Having done this we can use the ALT key to integrate the power and see the energy lost from the network over the cycle. God help you if you're a MAC user – but it really is your own fault! Try http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html for lists of keyboard shortcuts. Performing all this yields,

$$Q = 2\,\pi \cdot \frac{2.7586343 \times 10^{-3}}{367.78 \times 10^{-6}} = 47.128 \tag{8.42}$$

In the frequency domain we can observe the phase of the capacitor inductor and resistor currents and if we try we can look at the energy but I don't find it as useful or easy to see the physical significance of what I'm looking at. We can use the other compatible definition of quality factor $Q = \frac{f}{\Delta f}$ in the frequency domain however and this is much easier to deal with than all the sine waves and energy conservation. This yields $f \approx 3.3932$ MHz and $\Delta f \approx 72.072$ kHz so $q \approx 47.081$. This data is taken from an expanded version of the lower right graph in figure 8.7.

The two methods for obtaining the q, one in the frequency domain, one in the time domain are compatible with each other. The derivation of the frequency domain definition and the energy transfer definition can be found in the course notes for EEE117 in the appendix to section 10.

8.4.5 Why do we need a mathematical description of frequency in which frequency is a complex number?

Why does frequency have to be complex when I can go into the lab and use a signal generator that only produces sine waves (i.e. frequencies) with a real part and no imaginary part?

Have you considered Euler's formula,

$$\sin(x) = \text{Im}\left(\mathrm{e}^{\mathrm{j}\,x}\right) = \frac{\mathrm{e}^{\mathrm{j}\,x} - \mathrm{e}^{-\mathrm{j}\,x}}{2\,\mathrm{j}} \tag{8.43}$$

Just because the units on the signal generator don't have a j in them doesn't mean that the mathematics that supports the description of how the generator works doesn't itself rely on the existence of complex frequency. But that does not say why it's necessary, just that you might be using things in the lab that perhaps don't seem related to the mathematics but, in fact, they are...

There are a number of possible arguments that lead to the same conclusion but since we're thinking about poles and zeros we will consider some polynomials. It should be possible to express any continuous time system (realisable or non-causal) using a quotient of polynomials in s. For now lets suppose that s is a real number. That is to say s can only have a real part, it is not permitted to have an imaginary part. Now suppose I ask you to solve for the poles of a system who's transfer function is,

$$\frac{v_o}{v_i} = \frac{1}{s^2 + 40\,s + 1000} \tag{8.44}$$

You must find the roots of the polynomial in s in the denominator. That is to say we need the values of s that will make the denominator equal to zero. It can not be done! There are no real numbers that s could be which will make the denominator zero, yet it must be the case that this transfer function, this system, has poles. We must (perhaps grudgingly) admit s to the field of complex numbers not just the real numbers, because it is necessary. The problem is we can formulate a polynomial in s with complex coefficients (but with the imaginary part of all those coefficients equal to zero) that does not have real roots. This is because the field of real numbers is not algebraically *closed*. The fundamental theorem of algebra (which according to some sources is neither fundamental or a theorem but that is beside the point) tells us that,

"*every non-constant single-variable polynomial with complex coefficients has at least one complex root. This includes polynomials with real coefficients, since every real number is a complex number with an imaginary part equal to zero*".

So we ought to be looking at the possibility that some polynomials with real coefficients have complex roots. But we can go further by looking at the irreducibility of a polynomial over a field. Irreducibility is just a flashy way of saying if an expression can be factorised or not. If an expression can be factorised then it is not irreducible. So, also by the fundamental theorem of algebra,

"a univariate (having only one variable i.e. s) *polynomial is absolutely irreducible if, and only if, its degree is one."*

In other words our polynomial of degree (degree is just another word for order) two (8.44) must be factorisable and those factors must lay outside the real numbers, if they didn't, we'd be able to find them. We could say then that "(8.44) is irreducible over the real numbers but not over the complex numbers". What are

the roots of (8.44)?

$$\left(s + \left(20 - 10\,\mathrm{j}\sqrt{6}\right)\right)\left(s + \left(20 + 10\,\mathrm{j}\sqrt{6}\right)\right) \tag{8.45}$$

The real numbers can not provide solutions for (i.e. the frequencies of) the poles of certain networks or systems we have to use a larger field of numbers and one that is *closed*.

8.5 Poles and Zeros

Dear All,

You seem to be collectively a bit "adrift" when it comes to poles and zeros, how engineers usually represent them and the effects they have on circuit performance. I hope that a lot of the maths/systems information which you need to be able to follow the circuit work we are doing in EEE225 has already been presented in other modules, but the links may not be sufficiently clear for you to follow how this new 225 information latches on to what has already come before.

To give you a chance to scaffold the 225 stuff onto whatever you've had in 227 and in maths, I provide a list of book chapters and some YouTube videos, which can fill in any material which you are missing.

Poles & zeros ... from a mathematics perspective G James, D Burley, P Dyke, J Searl, N Steele and J. Wright, "Advanced Modern Engineering Mathematics" pp 1 - 87 Chapter 1: "Functions of a Complex Variable". Singularities are on page 56.

K A Stroud and D J Booth, "Advanced Engineering Mathematics" Fourth Ed. pp 821 - 937. These are the chapters on "Complex Analysis" which is the branch of mathematics we rely on for our modelling of systems and circuits. Singularities on page 915.

I would expect a student at Christmas of year 2 to be fully familiar with a number of Chapters of Glyn James's book including Chapter 1. I'll get the maths syllabus and see what they're including lately and when it is taught in the year.

... from an Analogue Circuits perspective Feedback systems esp. related to op-amp frequency response and stability.

J Millman and A Grabel, "Microelectronics", Second Ed. pp 564 - 608 & pp. 634 - 643. These are parts of chapters that deal with the frequency response, stability and compensation of feedback amplifiers from a circuits point of view.

P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer " Analysis and Design of Analog Integrated Circuits", Fourth Ed. Chapter 9 "Frequency Response and Stability of Feedback Amplifiers". As for Millman but told a little differently.

Sedra and Smith will have similar chapters. as both Millman and Gray.

... from a Control Systems Bishop & Dorf, "Modern Control Systems" tenth Ed. Chapter 8: "Frequency Response Methods".

If you like to learn via Matlab (by numerical example etc) you might find http://uk.mathworks.com/videos/series/using-bode-plots-95148.html useful.

Lastly (but probably the best for control in my view). The YouTube user katkimshow is a tenured professor in South Korea (in other words a lecturer in the UK system) who has excellent modules on control, including Bode plots and stability. She also lectures on the use of English in technical writing. This lecture (https://www.youtube.com/watch?v=ANRrwj_JHhE) should be familiar. When I need to re-learn some undergrad control stuff that I've not used for a while she is usually my teacher.

8.6 Compensation of non-inverting Op-amps III

> Could you please tell me how to answer sample exam Q11, part a?

Have a look in Millman pages 634 - 641. This will tell you what you need to know. Especially the diagrams. If you've not got a copy of Millman to hand, try Op-amps for Everyone by Mancini http://user.unob.cz/biolek/vyukaVA/skripta/OpAmpsForEveryOne.pdf Chapter 7 (7-1 – 7-4).

8.7 DC Offset in Op-amps

> Dear James,
>
> Can you please explain how to do EEE204 2011 - Q1 v as there is nothing on this subject in the notes?
>
> Kind Regards

Offsets are no longer taught in the course. No need to worry about it. Information for general reading if you are interested, which of course I'm sure you are... ;-) is in offsets.pdf

8.8 EEE225 2015 paper

I am attempting the 2015 225 paper and on question 4(b) you are required to show that

$$\omega_0 = \frac{1}{1 + j\,\omega\,C\,R_2} \text{ and } \omega_1 = \frac{1}{1 + j\,\omega\,C\,(R_2 + R_3)} \tag{8.46}$$

but when I did it I got the correct k term but for the ω terms I got them without the $1 + j\,\omega$ part in the denominator,

$$\omega_0 = \frac{1}{C\,R_2} \text{ and } \omega_1 = \frac{1}{C\,(R_2 + R_3)} \tag{8.47}$$

Would you be able to explain how I may have gone wrong?

You're solution is correct, I made a mistake in the question.

8.9 Sketching Bode Plots

I would like to ask why there is two different methods to get the y-axis when drawing a bode plot (figure 8.10)?

One is smoothed to be more realistic, the other is "asymptotic" which is not wrong, but it's only realistic in the corner frequencies and the slopes. The actual shape of the asymptotic graph is stylised for ease of drawing they represent the same thing.

Both are acceptable in the exam.

8.10 EEE225 Lecture example of first order op-amp calculations

Could you please tell me why the v_o/v_i is 50 in figure 8.11.

We are interested in the -6 dB frequency of the particular amplifier. -6 dB is 0.5 in linear. The low frequency gain of the amplifier is 100. Half of 100 is 50 so we seek the frequency at which the closed loop gain has fallen to 50. Substitute values into the equations and solve for f.

8.11 EEE225 Op-amp Problem Sheet Q8

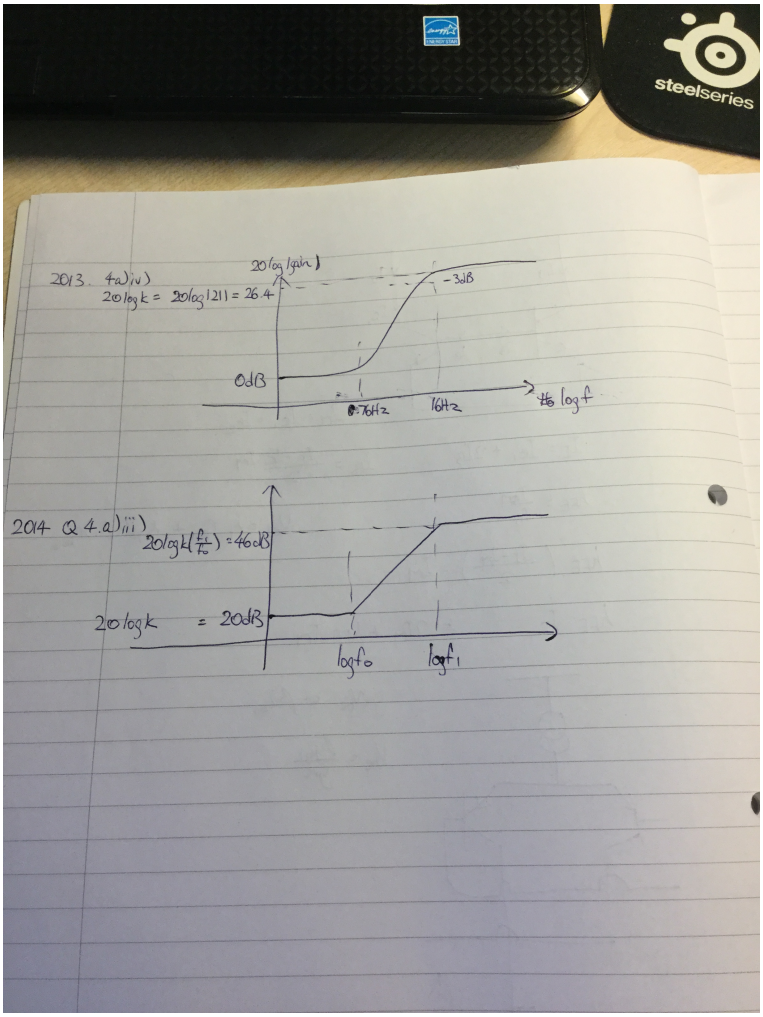


Figure 8.10: Styles of Bode plot.

For the Op-amp tutorial sheet question 8. Can you please show me how to solve the formula of the first order op-amp when a low pass filter was added at the output stage?

This is fairly easy actually, there is a "trick". The op-amp is pole zero where the zero lies at a higher frequency than the pole. We can get the transfer function by standard methods $v^+ = v^-$ etc. etc. To add the low pass filter we derive the transfer function of the low pass separately, presuming that it is driven by a negligible i.e. zero, source impedance (which is the output resistance of the op-amp). Then we note that both the op-amp and the low pass filter are linear time invariant (LTI) systems and this means we can multiply their individual transfer functions to get the overall transfer function. You don't therefore have

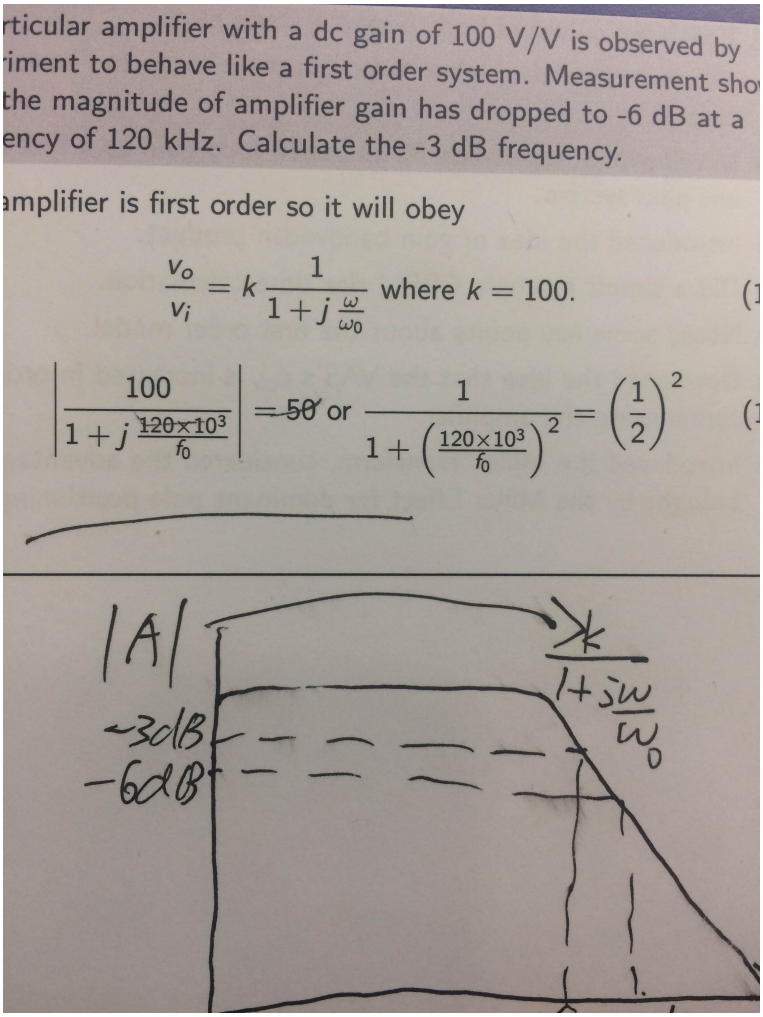


Figure 8.11: Opamp question from the lectures.

to derive the whole thing in a single step. If, for some reason, you wanted to, it is possible using usual techniques of circuit analysis from 117, 118 and 225 - consider it a challenge! ;-)

8.12 EEE225 2016 Exam Q4

Hi James,

Regarding question 4 part b past year paper 2016, the time constant given in the solution only consider R_3. Why the capacitor only discharge into R3 but not $[(R_1//R_2) + R_3]$?

Regards,

The pole is formed by R_3 and C. This is the term in s in the denominator of the transfer function. To see this, we could just derive the equation but that will not lead to much insight beyond a capacity to do linear algebra, and I suspect most student's mathematics is not a key deficiency despite their general hatred of it and many academics, myself included, protestations that "they don't do enough maths" often starting "When I was an undergraduate..... blah blah blah, Maxwell's equations... three dimensional complex Fourier integral... quantum field theory... shape of the universe... apples falling from trees etc. etc."

To get some real insight we must consider the virtual earth. Alternatively if you like Monty Python you could consider the Lilly (https://www.youtube.com/watch?v=9czBBKof7Yo), but the virtual earth is much more fruitful in this case.

It will help to have the circuit in front of you when reading this, it is shown in figure 8.12. The inverting input of the op-amp is forced equal to the non-inverting by the infinite open loop gain. This means that R1 will have a current of v_i/R_1 in it and this current is not dependent on the value of R_3 and C but only on the input voltage, v_i and the value of the resistance R_1.

The current in the $R_3 + C$ branch will increase with increasing frequency and that in conjunction with the magnitude of the current R_1 is what leads to the position of the zero (the root of the numerator), but you asked about the pole. As it turns out the zero is harder to pin down, in terms of it's underlying cause, by just thinking it out in words. If you use the LTSpice model at the end of this answer you can set up an AC simulation (as opposed to the transient that I used) to see what happens to the ratio of the R_1 to $R_3 + C$ current at the location of the zero in the frequency domain.

Anyway considering the pole... The current in R_2 is only dependent on the current in $R_1//(R_3 + \frac{1}{sC})$ as this current and the current in R_2 must be equal to each-other. If not current would be created or destroyed on the inverting input node and this would break KCL.

Current does not flow into the input of the op-amp because we presume the input resistance is infinite. This assumption is compatible with the infinite open loop gain assumption.

Because the inverting node is at ground, currents flowing in R_1, R_3 and C cannot also flow in R_2 (and *vice versa*). The fact that the two currents are equal is imposed by the op-amp, they are not the same actual electrons in both branches it just so happens that two currents that flow into a good approximation to ground near to each-other on the circuit diagram have the same magnitude. Consequently R_2 can not interact directly with C, R_3 and R_1 and therefore R_2 can not appear in the time constant of the pole or the zero.

Now, imagine we take a battery (DC source) and a switch which is initially off and place them in series with each other and then connect them to v_i and ground to form a loop involving $(R_3 + C)//R_1$, the switch and the battery where the lower end of the battery is connected to ground.

We throw the switch (on). C charges through R_3 up to a maximum voltage of v_i and a current of v_i/R_1 flows in R_1 but does not depend on the current in $R_3 + C$. The shape of the voltage waveform across C will be an exponential rise to maximum. This is because the voltage left available across R_3 falls the more C charges up hence the charging current falls with time yielding the exponential rise to maxima. We know that this shape is associated with low pass circuits and low pass circuits must have at least one pole so when we conduct this thought experiment we are looking at a pole in the circuit and it's position on the complex s plane (or it's time constant if you prefer) is set only by R_3 and C.

In that case you might ask why the output voltage looks distinctly dominantly high pass. Well, to see the logic there you might think about the mass of an unladen swallow (https://www.youtube.com/watch?v=liIlW-ovx0Y) but it would be better to think about the current in the feedback network as that is what controls the output voltage (effectively). This seems weird, like Monty Python, but the feedback current is set by the input current and KCL on the v^- node, the output voltage will have to comply... The feedback current flows through a feedback resistance and Ohm's law applies. The output voltage has to assume a certain value in order for the circuit to work the way it does and for the laws of nature to be obeyed. Now the current in R_3 may be falling as C charges after we throw the switch but when we actually throw the switch the current in R_3 is, very briefly, as big as it's ever going to be. This current flows in R_2 but in the opposite direction such that the positive $\mathrm{d}v/\mathrm{d}t$ input pulse leads to a negative $\mathrm{d}v/\mathrm{d}t$ output pulse whose voltage is proportional to the magnitude of the sum of the currents in $C + R_3$ and R_1...

I attach an LTSpice circuit that should help. It contains a behavioural op-amp with an open loop gain of 1×10^{12} which is more or less infinite. It is possible to inspect the currents and voltages to see how the circuit develops the waveforms it does and where the time constants come from. You could even investigate the consequence of non-infinite O/L gain if you like.

LTSpice is available from: http://www.linear.com/designtools/software/

I wouldn't expect many candidates to get this "talky talky" approach, it's not easy. I suspect that's why people tend to learn how to derive the equations and pick up most of the marks without having a deep understanding of what's going on, unfortunately. If you can explain it to someone else, and they can explain it back to you, and they have no further questions that you can't answer, you

probably understand it.

File: 2016PZcctwithbehaviouralopamp.asc

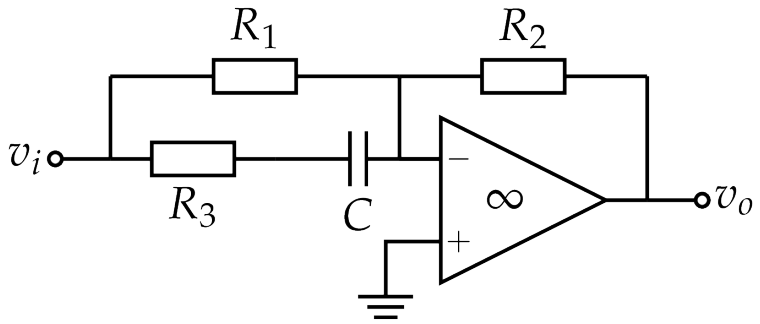


Figure 8.12: Op-amp pole zero circuit.

8.13 EEE225 2013 Question 3

Hi,

Am a bit confused about question 3biii of the 2013 exam: gain needed for amplifier circuit. 8 was obtained in the solution sheet but the explanation not sufficient.

Thanks

The gain is the numerical value of the transfer function, v_o/v_i.

The transfer functions of linear time invariant systems are multiplied together to find the total transfer function of the whole set of systems connected together. Therefore working backwards you have two systems who's gain has to come to 64 so take the second root of 64 to yield the the gain that both systems need to have to meet the specification. If it was three amplifiers who's total gain was 64 we'd take the 3rd root.

Chapter 9. Noise Questions

9.1 EEE204 2013 Q3

EEE204 2013 Q3 I am unsure why the noise voltage source is squared by

$$\left(\frac{6.8\ \text{k}\Omega}{12\ \text{k}\Omega + 6.8\ \text{k}\Omega}\right)^2 \tag{9.1}$$

For instance why was it not the 12 kΩ resistor on top?

For the 6.8 kΩ question, we want the output noise across the 6.8 kΩ resistor the $6.8/(12 + 6.8)$ is a good old potential divider. The squaring is due to the way uncorrelated noise sources are combined. Have a look at the noise lecture notes and videos to see how that comes to be.

9.2 Source Resistance (R_S)

Dear James,

I got a question about the Noise Equivalent Circuit of Op-amp. What is "R_S" and What is the function of R_S?

Many Thanks!

R_S is the internal resistance of the noiseless (Thvenin or Norton, but we only use Thvenin in 225) source which drives the system being analysed. The mean squared noise of this source is $4\,K\,T\,R\,\mathrm{V}^2/\mathrm{Hz}$ where R is the resistance of the source, T is the temperature in Kelvin and K is Boltzmann's Constant. Generally speaking $R_S$is fixed or at least has a minimum value below which we cannot reduce it depending on the question or the application we're designing for.

For example if we wanted to make a pre-amplifier to play a phonograph record we would expect an output impedance from the cartridge that was quite high. We could add more series resistance, but that would probably only add more noise. The only way to get a lower R_S would be to choose a different cartridge head which has a lower R_S. The cartridge is a sensor that runs in the grooves of the record and turns the mechanical movement in to electrical signals. Phono equipment is audio bandwidth and therefore is not impedance matched.

In impedance matched systems we would expect R_S to be equal to the input resistance of the system we were analysing, in order to minimise reflections on the transmission lines and provide maximum signal (and noise) power transfer from the source to the system under analysis. The noise power available per unit bandwidth in an impedance matched system is $K\,T$ multiplied by the bandwidth. Where K is Boltzmann's constant and T is the temperature in Kelvin. The proof of this is in one of the lectures 10 or 11 I would think. It is also in the handout on noise.

Best,

James

9.3 EEE225 Noise problem sheet Q5

I got some questions on the Noise problem sheet, I'm confused about how to get S_O in Q5 part (ii). The solution says $S_O = (50 \cdot 10^{-6} \cdot (5/7) \cdot 100)^2$? Does "5/7" mean the voltage divided by r_i?

In problem sheet 3 Question 5, the 5/7 in the solution comes from the potential division of the source voltage by the ratio of the source resistance and the noise free input resistance

$$50 \text{ uV} \cdot \frac{50 \text{ k}\Omega}{(50 \text{ k}\Omega + 20 \text{ k}\Omega)} \text{ A}^2 \tag{9.2}$$

where 50 uV is the input signal voltage and A is the gain of the stage in V/V. Since all the resistors are in kΩ we can ditch the power of 3 as it will cancel.

9.4 Neglecting R_S when r_i is not very large

Hi James

For the Lecture 12, 6th slide. It says that when r_i is not very large, say less than 10 MΩ, then R_S can be removed. Can you please show me how to derive it?

Thanks for your help

Best regards

Sorry it's a bit later than I said, I'm a bit tied up at the moment with various things.

The noise equation simplifies as follows, but it is not a derivation as such...

In the slide we are experimenting with ways to find in and v_n, which are the equivalent noise generators of an amplifier containing many noisy components. By the time we get to the equation that interests you we have already dealt with v_n by setting $R_S = 0$ such that there is no noise voltage at the input due to in (noise equivalent current generator) flowing through any r_i (input resistance) or R_S (source resistance) because R_S and r_i appear in parallel and R_S shorts r_i out and takes all the current from the input noise current generator without having a voltage i.e. $R_S = 0$ and

$$v_{\text{input}}|_{i_n} = i_n R_S \tag{9.3}$$

You should read this as "the noise voltage at the input due to the equivalent input noise current generator equals the input noise current multiplied by the source

resistance". We are effectively doing a superposition in which v_n is switched off and so is the signal source.

If r_i is unknown (really huge or we just don't know for sure how big) we can't get to a value for i_n by taking away the input signal source resistance and allowing in to flow through r_i and then measuring the voltage at the output and dividing by the noise gain and the size of r_i to get to i_n, because we don't know how big r_i is... Therefore we must set $R_S = 0$ and use the in flowing through a known R_S (where R_S is much much smaller than whatever r_i might be) such that we can know the resistance through which in flows and develops a voltage over. In this case we must use the full equation...

However there is a simpler situation where we know the value of r_i exactly and it is reasonably low (less than 10 MΩ, which is quite small when talking about the input resistance of an op-amp). In this second case we don't need to add any R_S at all because r_i is known and we can allow in (the noise current...) to flow through only that resistor (by not connecting the source up to the circuit at all) and then use the gain and the value of r_i to get from a measured output noise voltage back to a value of i_n directly (presuming that we have already worked out the appropriate value of v_n by shorting the input to ground and measuring the output noise voltage and then dividing by the noise gain). For this case the equation simplifies as shown on the slide because R_S doesn't exist.

This is all probably fairly confusing in words so it may help to read section 6 in the noise handout (not the slides, the typed notes) which relates to this question.

9.5 EEE225 Noise Problem Sheet Q11

Hi James,

I'm a little confused on the voltage generated by noisy resistors, for example in question 11.A of the 2015-16 past paper. The solutions say that the voltage from the noisy resistor 1.5 kΩ is

$$v_n = 4\,k\,T\,R_1 \left(\frac{R_2}{R_1 + R_2}\right)^2 \tag{9.4}$$

and the 3 kΩ resistor is

$$v_n = 4\,k\,T\,R_2 \left(\frac{R_1}{R_1 + R_2}\right)^2 \tag{9.5}$$

could you explain the $\frac{R_1}{(R_1+R_2)}$ and the $\frac{R2}{(R_1+R_2)}$ part?

Thanks in advance,

The noise sources, both the ones that are shown and the ones that exist due to the noisy resistors, are subject to the same circuit laws (Ohm's law, KVL, KCL, resistors in series add, resistors in parallel reduce) as periodic waveforms (sine, triangle etc.).

If I was working out this one I'd do it by superposition. Start by working out the noise voltage across the output nodes due to each source in turn (there are four to consider). The noise at the output due to the 3 pA/$\sqrt{\text{Hz}}$ source for example would be obtained by,

1. Switch off all other generators. All other generators are Thvenin sources so they go short circuit.
2. By inspection the two resistors are in parallel. As an aside the noise current flows through them both in the inverse of the ratio of their resistances (Millman's Theorem - yes *that* Millman, as in "Millman and Grabel" also known as the "current divider rule" if you prefer) which is the same as if it was a sinusoidal current for example.
3. Apply Ohm's law

$$\overline{V_{no}^2}|_{i_n} = i_n^2 \cdot (R1 \,//\, R2)^2 \tag{9.6}$$

read as "the mean squared output noise voltage due to the current noise source labelled i_n is equal to the product of the mean squared value of i_n and the parallel combination of R_1 and R_2 squared". Dimensionally this stacks up as we have volts squared on the left and amps squared multiplied by Ohms squared on the right...

You'd attack the other three sources by similar means and find that the amount of noise at the output depends somewhat on where the noise generator is in the circuit and the circuit topology.

To get the Thvenin resistance you can either do it by inspection or by brute force. If it's inspection we essentially do a little superposition by switching off all the sources and then inject a current into one of the output nodes (and extract it from the other) or impress a voltage across the output nodes from a test source, just the same as if we were trying to calculate the output impedance of a current source/amplifier etc. "Measure" (mathematically) the voltage that appears due to the injected current or the current that flows due to the impressed voltage. Apply Ohm's law to get the Thvenin resistance. The brute force method is to compute the open circuit voltage and the short circuit current then divide them – you'd either need to do this by superposition or by loop/node analysis which would be unnecessarily laborious, inspection is certainly easier in this case.

For the case of the v_n source the output is taken across the 3 kΩ resistor and the two resistors form a potential divider. Hence

$$\overline{V_{no}^2}|_{vn} = (5 \times 10^{-9})^2 \cdot \left(\frac{3 \times 10^3}{(3 \times 10^3 + 1.5 \times 10^3)} \right)^2 \tag{9.7}$$

where the first part is the 5 nV source and the second part is the potential divider equation. Same argument applies to the noise sources associated with the internal noise of the two resistors.

Best thing to do with these questions (any circuit problems actually, either in theory or on the test bench) is draw out the circuit diagram with all the sources drawn in so you can see what's going on visually, it's well worth the 20 seconds or so that it will take in this case. In fact I think a lot more good work would be done generally if people drew more diagrams and, dare I say it, remembered a few less equations.

9.6 EEE225 Noise Problem Sheet Q4

I'm confused on the equivalent voltage generated by noisy sources. For example, in Q4 of the noise problem sheet, why $V_{ab} = V_3 + V_4$ not $V_{ab}^2 = V_3^2 - V_4^2$? Is it because $2 \cdot V3 \cdot V4$ is too small?

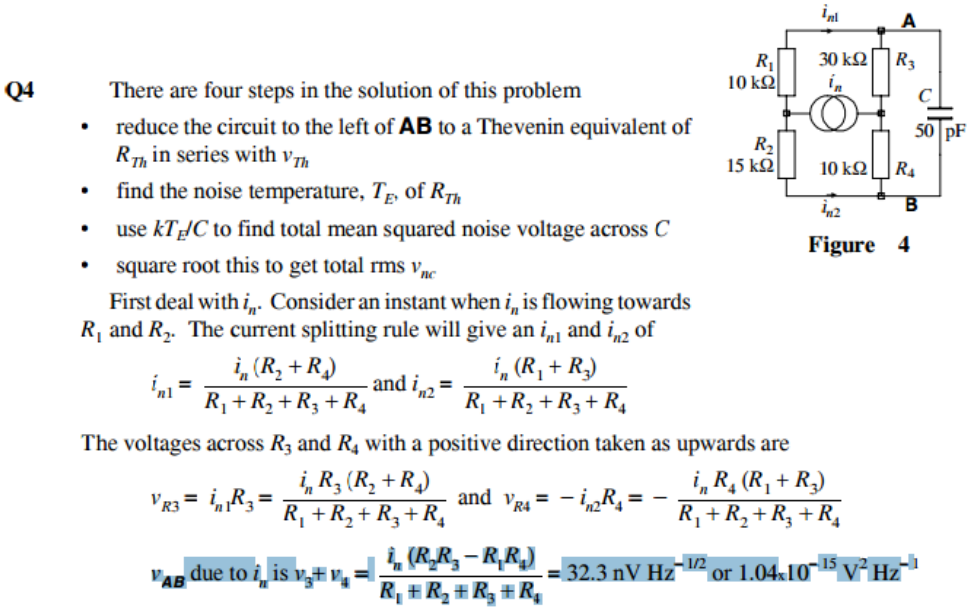


Figure 9.1: Noise Problem sheet Question 4.

If this wasn't a noise question, just a regular question with a sinusoidal or DC source in it, and we wanted the voltage between node A and node B you'd say "well it's the voltage across R_3 added to the voltage across R_4", right?

The fact that the source "signal" is aperiodic doesn't change the laws of circuit analysis... Some of i_n flows through R_1 and R_3 and the portion of this that contributes to the magnitude of the voltage across nodes A – B is the R_3 bit. Similarly some of i_n flows through R_2 and then through R_4 and the portion of this that contributes to V_{AB} – is the R_4 bit.

Or, looking only at R_3, R_4 and C we have a loop and KVL says the voltages around loops must sum to zero (provided there are no induced currents in the loop due to magnetic flux cutting the loop).

When I'm dealing with noise if the problem is somewhat involved e.g. Section 12 and the appendix of http://iopscience.iop.org/article/10.1088/0957-0233/23/12/125901/pdf*, I try to do all my algebra using $\mathrm{V}/\sqrt{\mathrm{Hz}}$, $\mathrm{A}/\sqrt{\mathrm{Hz}}$ and Ohms. There are none of those pesky squared signs everywhere causing trouble. When it comes to numbers I will probably switch to V^2/Hz, $\mathrm{A}^2/\sqrt{\mathrm{Hz}}$ and Ω^2 but this is just a habit I've picked up over time, there is no reason you can't do it all in V or A $/\sqrt{\mathrm{Hz}}$ or indeed in V^2 or A^2 /Hz. As long as you're careful with what you square and keep an eye on your dimensional consistency and don't break any standard circuits rules, it'll be fine.

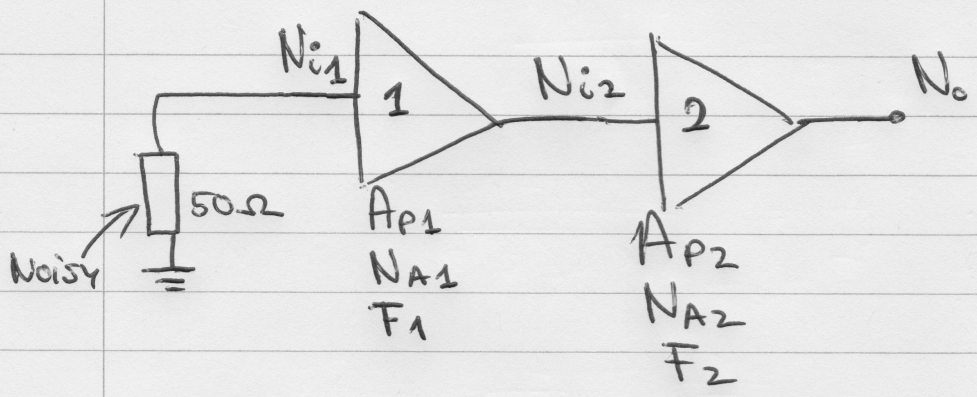
*Yes! See! Research lead teaching. In case you're now worried, noise in BJTs is *not* part of EEE225 but from the paper you can pick up fairly quickly how it is done. The methods are the same as for the questions in the problem sheet.

9.7 Noise Factor Derivation (UNANSWERED)

> Dear Dr. Green,
>
> I have attached below my derivation of the noise factor, after we have talked today in the problem class. I agree that the result does not look correct. But I am not sure what I am doing wrong.
>
> Thank you for your time. I look forward to hear from you soon.
>
> Respectfully,

I don't know why but for some reason I didn't get round to answering this. I'll do it eventually.

NOISE FACTOR OF A TWO STAGE IMPEDANCE MATCHED SYSTEM:



N_{i1} - NOISE POWER AT THE INPUT OF AMP 1

A_{P1} - GAIN OF AMP 1

N_{A1} - NOISE ADDED BY AMPLIFIER 1 (NOISE POWER)

F_1 - NOISE FACTOR OF AMP 1

N_{i2} - NOISE POWER AT THE INPUT OF AMP 2

A_{P2} - GAIN OF AMP 2.

N_{A2} - NOISE ADDED BY AMP 2 (NOISE POWER).

F_2 - NOISE FACTOR OF AMP 2

$$N_o = N_{i1} A_{P1} A_{P2} + N_{i2} A_{P2} + N_{A2}$$

$$N_{i1} = K T_o \Delta f$$

(AS THE SYSTEM IS IMPEDANCE MATCHED).

T_o - temperature of environment.

$$N_o = N_{i1} A_{P1} A_{P2} + N_{A1} A_{P2} + N_{A2} \quad (1)$$

(2) $N_{i1} = kT_0 \Delta f$ (AS THE SYSTEM IS IMPEDANCE MATCHED)

T_0 – temp. of environment

$$F_1 = \frac{N_{A1}}{A_{P1} \cdot N_{i1}} + 1 \iff N_{A1} = (F_1 - 1) A_{P1} N_{i1}$$

$$\iff N_{A1} = (F_1 - 1) A_{P1} kT_0 \Delta f. \quad (3)$$

$$F_2 = \frac{N_{A2}}{A_{P2} \cdot N_{i2}} + 1 \quad (4)$$

$$N_{i2} = N_{A1} + A_{P1} N_{i1}$$

$$N_{i2} = (F_1 - 1) A_{P1} kT_0 \Delta f + A_{P1} kT_0 \Delta f.$$

$$N_{i2} = F_1 A_{P1} kT_0 \Delta f. \quad (5)$$

Using (5) in (4):

$$N_{A2} = (F_2 - 1) A_{P2} A_{P1} F_1 kT_0 \Delta f. \quad (6)$$

On handout, it is WRITTEN:

$$N_{A2} = (F_2 - 1) A_{P2} kT_0 \Delta f.$$

DISAGREEMENT

Substituting (6), (3) (2) into (1)

$$N_o = kT_0 \Delta f A_{P1} A_{P2} + (F_1 - 1) A_{P1} A_{P2} kT_0 \Delta f + (F_2 - 1) F_1 A_{P1} A_{P2} kT_0 \Delta f \quad (7)$$

(1 ← ONE)

$$F_{TOTAL} = \frac{N_o}{N_{i1} A_{P_1} A_{P_2}}$$

Using (4):

$$F_{TOTAL} = \frac{kT_o \Delta f A_{P_1} A_{P_2} + (F_1 - 1) A_{P_1} A_{P_2} kT_o \Delta f + (F_2 - 1) F_1 A_{P_1} A_{P_2} kT_o \Delta f.}{A_{P_1} A_{P_2} kT_o \Delta f.}$$

$$F_{TOTAL} = 1 + (F_1 - 1) + (F_2 - 1) F_1$$

$$F_{TOTAL} = 1 - 1 + F_1 - F_1 + F_2 F_1$$

$$F_{TOTAL} = F_2 F_1$$

WEIRD RESULT. I DON'T SEE WHAT I AM DOING WRONG THOUGH.

9.8 Question about Noise Factor

Dear Dr. Green,

I have a very short question about noise. For a given device, is the noise figure F constant or is the noise added by the device Na constant?

I am basing my question on equation,

$$F = 1 + \frac{N_a}{(A_p\, N_{in})} \tag{9.8}$$

Where A_p is the gain of the amplifier (constant) and N_{in} is input noise.

Input noise is a variable so one of them must vary as well, which I find a bit weird. If F would vary with the input nose, that wouldn't make it a good parameter to define the noise performance. On the other hand, I don't see why the noise added by the amplifier should depend on the input noise either.

Sorry to take up your time. Thank you very much.

Respectfully,

N_a and A_p both depend on frequency and so the noise factor F is a function of frequency too. N_a also depends on the quiescent (DC) conditions in the active components.

Have a look at the graphs on the data-sheets for the two Minicircuits amplifiers I discuss in lecture 10 or 11 of EEE225. It will only show F and A_p but you can presume that N_i is constant and see what's happening to N_a.

Chapter 10. Other Analogue Questions

10.1 Bridge Oscillators

Dear James,

This the question from the EEE224 (2013-14) oscillator (shown in figures 10.1 and 10.2. In the quest part(c), there is mention the RC circuit should be 1 kΩ and 1.59 nF. As I ask on the street I have no idea what is the "right" value of RC in this circuit. Can you do a detail explain for this, please.

Kind Regards,

For a bridge oscillator one needs positive *and* negative feedback. If there is

frequency dependent feedback between the output and the non-inverting input, then that feedback will be regenerative or positive (as opposed to negative or degenerative). If there is feedback to the inverting input the feedback will be negative.

In the case of the circuit in the question, it is a band pass circuit with a centre frequency given by the equation in the question. All that is required here is to get the transfer function. When we derive the transfer function we will find that the frequency independent gain, k, is 1/3. Therefore your loop gain must be at least 3 to start the feedback loop oscillating (hence the R, 2R combination in the negative feedback part of the op-amp circuit in the solution)

As for the frequency of oscillation, the circuit can only oscillate at frequencies where the gain is more than unity (overall) and where the feedback is positive. The time constant of the band pass network is therefore set to give the desired resonant frequency, however the exact value of R and C doesn't matter (within limits). The limits are defined by two factors. Firstly, all resistors have a parasitic capacitance and so do op-amp inputs. These capacitances are often between 1 pF and 5 pF. If we choose to make the capacitance in the band pass network a similar value to the parasitic capacitance then we should expect a large error in the oscillation frequency. Therefore we must make C significantly bigger than the parasitic. This is one reason why we don't build wide band circuits on "bread board", it has the most horrific parasitics due to the way it's constructed. On the other hand we need to put a significant $\mathrm{d}v/\mathrm{d}t$ across the capacitance and if we make the capacitance too big then that will necessitate a large i (because $i = C\,\mathrm{d}v/\mathrm{d}t$). A real op-amp can only source and sink about 20 mA or so (e.g. TLO81, OP07, OPA134, NE5532 for example). This slew rate limit means that we mustn't make C too big either. Hence we must not only select R and C to give a particular time constant but also C and therefore R must be bounded at high and low values.

The simulation file listed below may be instructive. The bridge oscillator is as described in the question. There is a positive feedback loop consisting of the band pass filter. and a negative feedback pathway involving the 20 kΩ and the 680 Ω in series with 8.2 kΩ and the channel resistance of the 2N3819 JFET. This circuit or ones like it can be found all over the internet. This one is purposely made from EEE118 circuit blocks other than the JFET.

The job of the JFET is to change its channel resistance according to the magnitude of the gate – source voltage, v_{gs}. The gate – source voltage is proportional to the peak average value of the negative half cycles of the output waveform. Effectively J_1, R_8 & R_7 form a voltage controlled resistance. D_1, R_5, R_4 and C_3 are a peak detector. When $V_{gs} = 0$ the saturation current of the JFET flows (JFETs have to be switched off by making V_{gs} negative) and the resistance of J_1's

channel is small hence the gain of the non-inverting amplifier is approximately,

$$\frac{(20\text{ k} + 0.680\text{ k} + 8.2\text{ k})}{(0.680\text{ k} + 8.2\text{ k})} \tag{10.1}$$

which is somewhat more than 3. As a result there will be a range of frequencies over which the amplifier can oscillate due to the positive feedback with a gain greater than unity applied to the non-inverting input. This will be a small range of frequencies around 100 kHz. The oscillator settles into the resonant frequency because that is the frequency at which the circuit can oscillate with the minimum amplifier gain.

As oscillation begins the peak detector charges C_3 slowly through R_5. The time constant of this network is at least several cycles of the oscillation frequency. The voltage on C_3 is below the ground level and as it increases negatively it acts to switch off J_1 somewhat. This switching off effectively reduces I_d while V_{ds} is essentially constant. Both the current and voltage are sinusoidal at the same frequency so while they do go up and down, they do so together therefore we can consider the JFET channel as having a resistance that varies slowly compared to the oscillation frequency. Try plotting $V(\text{ctrl})$ and $V(\text{out})$ in LTSpice over each other to see the effect of the variation of J_1's resistance on the stability of the oscillator. I have purposely designed the control loop to be somewhat underdamped such that the oscillator saturates initially and then has some ringing in it's control loop which is manifested as amplitude modulation in the output waveform. After 2 ms or so the control loop stabilises and the oscillator produces 10 V_{pk} at 100 kHz with about 1% distortion.

If you're wondering about the two 100 kΩ resistors. They linearise the JFETs channel resistance as a function of V_{GS}. Useful if you've got ideas for an audio compressor or something (although there are other methods involving OTAs which are better for that sort of fun). The logic of the two 100 kΩ resistors is described at (for example) https://goo.gl/DDG8wU.

One thing I've not said anything about so far is how to determine if an oscillator will start in Spice. One needs to "prod" the circuit a bit by having spice ignore the initial conditions and start all the power supplies from zero, just like in a real circuit on the desk which is switched on when the PSU comes up. Of course in reality electronic fluctuations in the circuit components will cause a self-sustaining oscillation to begin, if we don't ask Spice to consider noise it will pretend there is none and as a result sometimes spice will find a steady state for the oscillator in which it is not oscillating. Using the `UIC` and `STARTUP` commands in the simulation function encourages most oscillators to start appropriately.

The trick to these feedback oscillators (and the phase shift oscillator too) is to think about the gain "around the loop", you'll know that you've mastered

it when you can say why 3 is the magic number for this circuit. The same considerations dominate the compensation of op-amps but in that case we want to avoid oscillation not encourage it.

Yet another way to discuss oscillators is to think about the poles and zeros of the circuit using a Nyquist diagram or Root Locus diagram. Stability is having your poles in the left half plane and instability is the right half plane. To get an oscillator to run with a bounded output voltage (i.e. not saturated against the PSU rail(s) but also not diminishing as a function of time) we need to keep a pair of conjugate poles sat on the imaginary axis with no real part. If they move into the right half plane the oscillation amplitude will get bigger until saturation occurs. If they move to the left the circuit will decay into a stable state after a period of ringing. The use of a voltage controlled circuit element like the JFET (or a filament lamp) allows us to move the poles into just the right place. It would be impossible to use a variable resistor by hand to do this. Bridge oscillators are discussed in terms such as these in Vacuum Tube Oscillators By Eadson (http://www.tubebooks.org/Books/vto.pdf) an old but very good book on the subject. A more modern book but perhaps more difficult to find is R W Rhea, "Oscillator Design and Computer Simulation" published by Scitech.

Anyway, it's getting late...

BridgeOsc.asc.

10.2 Forward Recovery time of a diode (e.g. in a switching circuit)

Hi James,

As I'm sure you have a large number of emails as we are approaching exam time I can only apologise in adding to this list, but hopefully my question is small and simple.

I'm trying to understand the reasoning behind overshoot or the forward recovery voltage in a diode that is switching from reverse bias to forward bias. I have attached a photo of what I mean by overshoot for clarity but I'm sure you understand what I mean.

An article I read tried to explain it but all I can understand from it is it's something to do with the movement of charge and the capacitance of the p-n junction?

Fairchild Semi: https://goo.gl/KdAgHd

Maybe you have a chapter from a book that may explain it in basic terms for

EEE224

5. a. Briefly describe the conditions that have to be met for a closed loop system to act as a linear oscillator. **(2)**

b. In the circuit of figure 5.1, v_1 is a driving voltage applied as shown and v_2 is the measured output voltage. Show that v_2 and v_1 are in phase when

$$f = \frac{1}{2\pi CR}$$

and that at that frequency, $\frac{v_2}{v_1} = \frac{1}{3}$. **(5)**

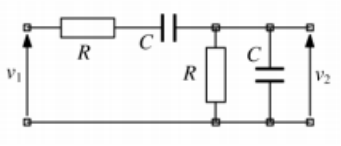


Figure 5.1

c. Draw a circuit diagram to show how the network of figure 5.1 can be used with a suitably configured operational amplifier circuit to form a Wein Bridge oscillator. Suggest suitable values for all the components in your circuit if f is required to be 100 kHz. **(6)**

d. How could you "tune" the output of your oscillator? (that is, how could you vary the output frequency of your design.) **(2)**

e. Why is a non-linear element necessary somewhere in the circuit of part **c.** if the amplitude of the oscillator output signal must not change significantly with output frequency, time and temperature?

Show how such a non-linear element could be included in your circuit and explain briefly how it stabilizes the amplitude of the output sinusoid. **(5)**

Figure 10.1: Phase Shift Oscillator Question.

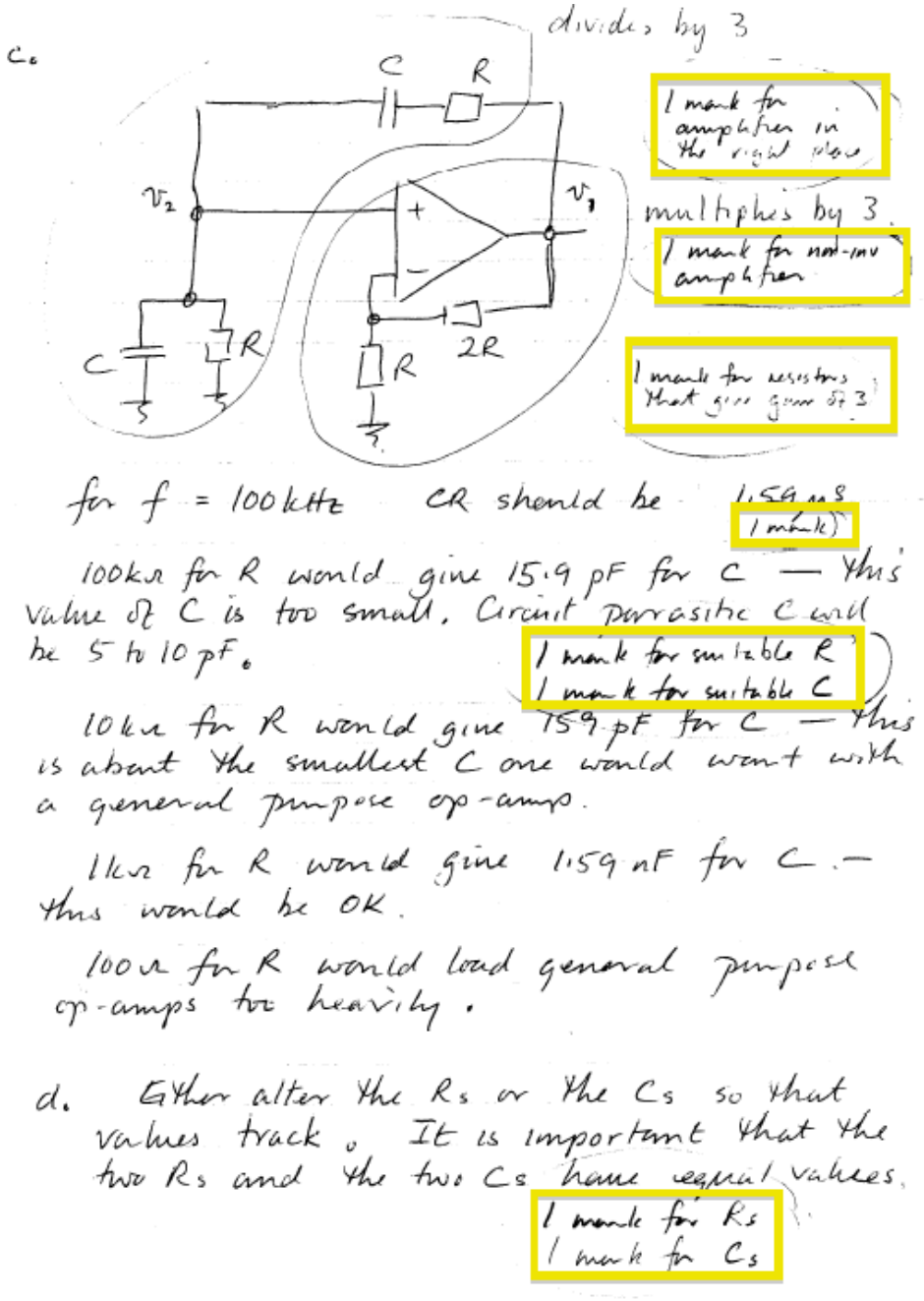


Figure 10.2: Phase Shift Oscillator Solution provided.

a more simpler mind like mine.

Many thanks,

Not yet. Actually, I don't think the panic has set in yet amongst the candidates.

With respect to your diode question it's EE223 stuff. Page 98 of E. Ramshaw, "Power Electronics Semiconductor Switches" https://goo.gl/LTm2Vj has a nice description. It's all to do with clearing the stored charge from the depletion capacitance before conduction can begin... Told you all semiconductors was important! ;-)

If you don't like Ramshaw you could try books by W K Chen or "Physics of semiconductor devices" by S M Sze and Kwok K Ng. It will certainly be in there too.

10.3 How do you produce such nice circuit diagrams?

Dear Dr. Green,

Sorry about disturbing you but I may have a problem. Currently I'm looking for a software which can draw some circuit diagrams but it is hard for me to find a proper one.

I've checked LT spice, but it may not be able to performs as expected, because the layout and colour of the diagrams it produced look a little weird. Also, the symbol for resistor is using American standard.

I've also tried some other software or websites, like Multisim or EasyEDA , but none of them can produce circuit diagrams which are as good as the ones in lecture handouts.

Could you give me some suggestions, please? If possible, could you please tell me what software you usually use to draw circuit diagrams?

Thank you.

Kind regards,

The materials I provide are composed in three different systems of software which are related to each-other but are independently developed.

1) Latex: pronounced "Laytec": A typesetting scripting language which is compiled directly into PDF. Mittlebach is the book https://www.amazon.co.uk/Latex-Companion-Frank-Mittelbach/dp/0201362996 and CTAN is the website, https://www.ctan.org/?lang=en. Latex runs on windows and Linux, MikTex and TexLive are the most popular distributions respectively and many GUIs

exist to assist in editing such as TeXnicCenter or WinEDT for windows and Kile for Linux under KDE. Latex takes some getting used to but it does provide dependable results with none of the glitches one gets with MS Word. It's more like programming than typing a document however so I usually write what I want to say in MS Word and then typeset it in Latex. The source code is a text file and is therefore incorruptible.

2) Circuit Diagrams: Circuits Macros https://ece.uwaterloo.ca/~aplevich/Circuit_macros/ The circuits macros require M4 (a macro language) which compiles to dPIC or GPIC drawing languages which is in turn interpreted by PSTricks a bolt on post-script drawing language for Latex. It seems like it shouldn't work because it's just too complicated but the evidence is there that it does work and produces beautiful diagrams. Some nifty scripting allows me to code diagrams and compile them with one button and then view the PDF output directly on a second monitor. In Linux the PDF reader Okular re-loads the PDF every time it changes so one can see the result in near real-time.

3) Graphs and general diagrams (not circuit diagrams) are written in PSTricks directly and compiled by Latex. Usually I draw these by hand on graph paper first and figure out the coordinates of all the vertices etc. before coding the diagram. This may seem like overkill but it has some very pleasant side effects: I have a very good idea of what I want to create when I start coding because I've already drawn it by hand. A good diagram may be worth 1000 words but a bad diagram can confuse you forever. If I write in my text that a graph is an exponential then it really is an exponential, not an approximation. The line of code that will generate the exponential line on the graph will be an expression of the function of the line. There is no fudging, sketching, guessing or approximating.

4) Lecture slides: are done in latex using an add-in package called 'Beamer'. I generally re-use diagrams between the pros notes and the slides.

One can make really good lecture notes in MS Word. Guang-Jin Li's advanced machine control course notes are all done in Word and MS Visio and they're really very good notes for learning machine control. I just happen to like a typesetting approach. I've been using Latex for 7 years, I've typeset two books using it, a number of scientific papers and two undergraduate courses. There are still so many things I struggle to do with it but the support on the web, especially stack exchange, is good. Often when I can't do something and I can't find an example of it anywhere else, the package developers are the ones who answer the questions.

There are other ways to do circuit diagrams with Latex and other flavors of Latex too e.g. XeTex (which is good for non Roman alphabets). A former research associate of our department uses Latex in windows and then uses Tikz (an equivalent of PSTricks) to compile down his circuit diagram code which is

created using a different set of macros: Cirkuitikz. I have to say, I prefer the circuits macros listed above but hey ho. An example of his sort of macros is at https://www.overleaf.com/5402902nkzsqm which also happens to be an online latex compiler. Essentially a web application that pulls "text" i.e. your code from a glorified form and then runs latex on it in the server side (cgi-bin) of a web server and pushes the pdf back to the client side – could also be done by PHP. Yet another approach for on the move was concocted by a former PhD student. He had a Linux box watching is Dropbox and if a latex file changed it would automatically recompile it. He could edit the source code on his phone while on the train, and have the new pdf arrive on the phone within 20 seconds – of course I have it all on a laptop and have the laptop with me... anything else is just showing off!

Collaborative works can cause problems. If I write a paper with some other authors and they are going to take part in the editing process I will do it all in MS Word. When they're all happy I spend the evening latexing it up. Not all lecturers are happy for students to use Latex so if you decide to go that way for a third year project you might want to check with the supervisor first. In essence it's your choice, but there is not an easy way to provide feedback on a document via tracked changes etc. when it's compiled directly to PDF. This can sometimes lead to frustration.

I have found that writing lecture slides requires between 10 and 12 hours of my time input to create a 50 minute lecture. About half of this is deciding what to say and drawing the diagrams by hand. The coding is the other half. Doing it in Word and Visio takes about the same amount of time.

One should really do all the editing in a word processor like Word or LibreOffice and then only when the text is ready typeset it using a typesetting package. The main typesetting packages are Adobe InDesign, PTC Arbortext, Corel Ventura (obsolete), QuarkXpress and Latex. All are very expensive except latex which is FOSS. Most publishing houses (e.g. penguin, random house, Bloomsbury etc.) don't do their own composition (typesetting) they just pass the files that the author provides to a composition company (e.g. http://www.techset.co.uk/) who's business is the typesetting of books and printed media. Latex is not widely used in the composition industry but a lot of academic journals who do their own typesetting (including IEEE, I think) will convert everything out of MS Word directly into Latex and then start their in-house composition work (pagination, float setting etc.).

Hopefully that gives you some idea of how I like to do it. To do the diagrams by my method you'll need the first two pieces of software (psTricks comes with Latex) and to spend a few hours getting it running. MS Visio is much quicker to get started but I feel it is limited in the end because everything is lined up by eye

on a grid. It really depends what kind of precision/repeat-ability you're looking for.

10.4 Transformers in LTSpice

Hi James,

I'm trying to design a power supply for my 2nd year design project, however I can't find a transformer building block in LTSpice.

Is there any predefined building block for transformers or do I need to make one using inductors and changing parameters?

Thank you.

Best regards,

Lay down two or more inductors (keyboard "L") then place a "spice directive" of the form "K1 L1 L2 0.97" where K1 is the name of the coupling, L1 and L2 are the two inductors to be coupled and 0.97 is the coefficient of coupling. Zero is uncoupled, 1 is fully coupled. Even a reasonable transformer will have a coupling factor of considerably more than 0.9. When the directive is placed, dots will appear on the inductors to denote the "dot" and "non-dot" end for the purposes of assessing current convention.

Chapter 11. Audio Questions

11.1 I'm building a Power Supply for audio stuff...

Hey James,

I'm building some musical stuff (EQ, crossover, blah blah) over summer and need a +/- power supply to power it all, the Op-amps and other chips involved run off +/-9V from the data-sheets, and I was wondering what you'd search for when looking for power supplies, are they called split rail? something similar? Or do you just get two single 9V supplies and put them in series, taking a 0V from the middle? would this interfere with the grounding of the metal enclosure by the in/out sockets?

Also would it be worth getting something like a +/-15V power supply, and using 7809 regulators (or equivalent) for stability?

I still need to calculate the total current requirement, but thought it was worth

an ask before splashing out on the wrong sort of thing and buggering everything up...

Cheers

So you want a bench PSU, or to make a PSU from scratch built in to your equipment, or to buy an OEM PSU and install it in your equipment?

If you're buying a bench power supply for testing use, try to get a second hand Farnell one on eBay or from an auction of a company that's folded up. These are linear power supplies of a quality not manufactured in modern times. Quiet, reliable, stable... Not like the switching supplies made to a tight budget these days.

If you're building one then a toroidal transformer followed by smoothing caps and a LM317 LM337 pair of regulators will be fine. Use shunt transistors if you need more than 1.5A. The datasheet will show you how. You can also implement a current limit with these ICs which while adding complexity is on balance a good investment. Similarly the datasheet has an example schematic which you should be able to deal with no problem.

I'd avoid OEM supplies. They cost nearly as much as the bench ones and do nothing that one you make yourself wouldn't do.

My favourite op-amp for audio is the OPA134, excellent distortion and good noise properties. The the NE5532 was the industry's choice in the 1980s there's still loads of kit with them in. Even the venerable TL081 is also a good choice. Everything recorded from 1965 - 1975 was done on a mixing desk and effects rack that contained either 741 or 709 op-amps or was valve or discrete circuits and the music sounds fine! Still, we can do better these days, without much extra cost.

Let me know if you need any more info.

I've got an old bench supply, I'm talking more a built in PSU, either bought or home built. You think 223 knowledge would be enough to build a decent PSU for reasonable price? I found a good web-page on winding transformers. (https://Ludens.cl/Electron/trafos/trafos.html)

I'll have a think about those op-amps.

Another question is about phase after the crossover network. I'm planning on implementing second order Sallen and key filters, but after splitting the frequencies the phases go all over the place.. do you think this will be a problem? I've been looking at some phase correction circuits, (linkwitzlab.com) but since these just do 180, 360,... 180n, etc I'm not sure if they'd actually solve any phase issues? What are your thoughts? Should I spent time trying to tackle

this or just not bother...

What effects does phase actually have on audio..? From my understanding it is only audible at low frequencies where it can cause dead spots In a room?

PSUs I would have thought 118 would be enough along with the LM317 / LM337 datasheet. If you're doing audio stuff I'd stay away from the switching supplies, you'll hear some artefacts. The human ear is fantastically sensitive (and should be looked after!) If you're dead keen on making your own linear regulator then 223 should be enough to see you right, but the LM318 really is very venerable, you'll not better it with any discrete design unless you spend years perfecting it.

I can send you some other notes that cover the same topics if you have gaps or just would prefer another take on it. You can send me your schematics or simulations (in LTSpice) if you like.

Speaker Boxes The position of a speaker in a room with respect to a listener or the position of a listener and two speakers with respect to each other (be it tweeter and woofer or two woofers with L & R channels) all affect the frequency response observed by the listener and two listeners a short distance apart will experience a different perception of the program material. This is because the wavelength of the sound waves and the objects in the room (and even the room itself, which is a resonant cavity) will affect the wave propagation. Ideally you'd have a speaker of infinite dimensions and zero mass, infinitely far away from the listener and the whole thing would be set up in a spherical universe which is otherwise empty except for a suitable medium. No floor... Since we can't easily obtain this, we have to make do. The crossover networks just make this situation more troublesome. Fortunately in most domestic situations the shape of the room and the use of passive crossovers doesn't pose a serious problem. Some people believe that passive crossovers are so bad that they use one amplifier per speaker driver in a so called bi-amped or tri-amped system. This is probably as close to ideal as one can expect to get but I've never bothered.

If you want a cookbook approach to loudspeaker box design try https://www.amazon.co.uk/Loudspeaker-Design-Cookbook-Vance-Dickason/dp/1882580478

If you want to know what's going on try https://he.kendallhunt.com/product/introduction-electroacoustics-and-audio-amplifier-design - I have a hard copy but no PDF exists anywhere on line as far as I can tell. If you buy it, don't by the ebook it has a time limit. Also beware of shipping charges and import fees from the USA. Kendallhunt are quite USA centric in their outlook.

If you want to read the original papers on closed box and vented (ported) box loudspeaker design then they're by A N Thiele and R Small. Much of what

Leach (above) has to say about speakers is an explanation of these papers and demonstration of their application.

If you want a good primer on acoustics generally then Acoustics by Leo Baranek, the first edition of which is now probably so old it's out of copyright. He died last year while we were doing EEE225. Obituary at http://acousticalsociety.org/sites/default/files/Leo_Beranek.pdf

Crossovers With regard to crossover networks then there is a book by Douglas Self, it's not too expensive. Also try the website of Rod Elliot (Elliot sound products) http://sound.whsites.net/projects-0.htm#xvr & http://sound.whsites.net/articles.htm#cros. I wouldn't get too carried away with Linkwitz this, elliptic that, minimum in-band ripple the other... etc. In truth humans are easily fooled about the direction in which sound comes from and they're not that sensitive to it any more than is necessary from an evolutionary standpoint and that is little more than: ahead, behind, left, right, above, below. You may think you can pinpoint where sounds come from with great accuracy but that is not the case, you're guided by hearing but the source location work is done mostly with your eyes.

If you're looking for simulation software then the industry standard is LEAP and is expensive but you could use something that does coupled multiphysics simulations like COMSOL. The sort of simulations you'd want to do are the magneto-statics to get the force on the cone given an AC signal current and a fixed magnetic field, then to do the mechanical simulation of the cone as it oscillates at different frequencies due to the force on the cone. Then you'd want to look at the far field pattern in the air pressure. Along the way you'd like to look at the effects of temperature rise in the coil etc. etc. so there's plenty of simulation to do. Of course if you want to know how it will work in your listening room you need to build a model of the room, sofa, windows, coffee table. You could take it way too far and it wouldn't achieve much!

11.2 Books about Audio Amplifiers and associated things

Dear All,

I said a while ago that I would send out some books about amplifiers and similar, but I haven't got round to it yet. Usually we don't use ISBN because the ISBN depends on the edition of the text and textbooks get revised quite a lot but for brevity I will just list the ISBNs and the salient information, title, authors publisher etc. This list then it will go out of date eventually as the ISBNs will change when new editions come out.

Analogue IC Design

- 978-0470245996 – Grey – Grey is the book. Probably one of the only books about circuits I still look at (when I'm stuck).
- 978-0072380323 – Razavi – Almost as good as Grey - some stuff on oscillators too which is missing from Grey.

General undergrad circuits text (including aspects of analogue design)

- 978-0521809269 – Horowitz & Hill (Third ed). (note the 3rd ed is not the same as the 2nd (apparently it's just an update to the 1989 classic which has mostly new material)).
- 978-0521370950 – Horowitz & Hill (Second ed).
- 978-0199339136 – Sedra & Smith
- Anything by Jacob Millman, Terman or Sealey.

Amplifier Books written for the amateur/serious non-professional:

- 978-0750626293 – Duncan - mostly rubbish, don't bother.
- 978-0071341196 – Sloan - big circuits most transistors in this book unavailable - descriptions iffy in places in my opinion.
- 978-0240526133 – Self, is a grumpy bear who's arrogance rivals even my own.
- 978-0071640244 – Cordell, a measured factual discussion of the key elements. Well written in my opinion.
- 978-0757572869 – Cracking book by Leach, good for loudspeaker enclosures as well.

Others by, for example, John Lindsay Hood - variable in quality, best avoided in my view, little good info that's not available elsewhere really.

A Seminal Patent: H. C. Lin, "Semiconductor Amplifier Circuits," United States of America Patent 2,896,029, 1959

Books on Noise:

- 978-1465200662 - Leach (good book, not too expensive)
- 978-0471577423 - Motchenbacher & Connelly

SPICE:
978-0071349550 - good general book to describe what's going on inside SPICE and describes what happens when one presses the run button. Doesn't cover the serious stuff that Si foundries will supply like BSIM models but this book is still my go-to when spice is acting funny and I can't see why.

If you're feeling brave...
Chung-Wen Ho; Ruehli, A.; Brennan, P., "The modified nodal approach to network analysis" IEEE Transactions on Circuits and Systems Volume 22, Issue 6, Jun 1975 Page(s): 504 - 509

Electro-acoustics and "audio engineering" including the design of audio amplifiers and speaker cabinets
978-0757503757 - Leach (good book. Leach was an excellent Lecturer)

Loudspeaker Enclosure Design
Papers by A N Thiele and R Small from 1965 – 1967 and 1973 – 1975 in the Journal of the audio Engineering Soc. are also invaluable but the same information can be obtained from The Loudspeaker Design Cookbook 978-1882580477. The fundamentals behind all of this are in "Acoustics" by Beranek 978-0883184943

Modern books about valve amplifiers

- 978-0080966403 - Jones
- 978-0080966380 - Jones (construction techniques)
- Quite a few others in this category in recent years but I don't own them (yet). Jones was one of the first of what we might call "revival" publishers.

Old books about using valves transistors etc. in circuits:

- Thermionic Valve Circuits, E Williams (very nice introduction, well written. I learned the concepts of small signals from this book)
- Electronic and Radio Engineering, F E Terman = Grey from 60 years ago.
- Electron Tube Circuits, S Seeley
- Vacuum Tubes - Spangenberg K R - Mcgraw Hill 1948 - design of vacuum tubes.
- Radiotron Designers Handbook 4th ed.
- Network analysis and feedback amplifier design - H W Bode 1945 or later editions
- Anything from the "MIT Radiation Laboratory Series (1946)"

For out of copyright books try:
http://www.tubebooks.org/technical_books_online.htm and Archive.org: For example https://archive.org/details/ElectricityMagnetism2ndEd - Bleany

and Bleaney, a very famous and seminal book about electro-magnetism.

Mathematical Foundations:
If you're looking for a mathematical foundation for the stability and compensation ideas in 225, and Grey (top) isn't enough, then I suppose the ultimate starting place is Nyquist's paper, but be warned it's very very heavy going! You may not have come across a "Nyquist Plot" either so it would be a good idea to look those up first before attacking http://people.tamu.edu/~mvrajesh1/ECEN605/LECTURE1/Nyquist_1932.pdf - I really wouldn't bother though. I've never made it all the way through. The book by Bode (above) is a bit easier.

Also Black's seminal paper concerning the invention of the feedback amplifier https://www.ieee.org/documents/proc_black.pdf (also requires understanding of the "Nyquist plot" as the Bode plot had not been invented at that time.)

Could also try "Feedback" by F D Waldhauer, Wiley, 0471053198.

People:
Articles (and books) by Bob Pease & Jim Williams in (for example) EDN magazine, electronics and wireless world. Jim wrote "EMC for product designers" as well as several other text books. Bob is widely regarded as one of the most influential analogue designers of the last 40 years.

Books about building stuff:

- 978-1625950192 - ARRL handbook - very good new one comes out every year.
- 978-0750680714 - Practical Electronics Handbook (so so but its a difficult bunch for construction skills.)
- See also Jones (above)

Popular Science: Books for light reading.

- M. Kumar, Quantum: Einstein, Bohr and the great debate about the nature of reality: Icon Books, 2008.
- D. Sobel, The Planets: Fourth Estate, 2005.
- G. Watson, The Civils: The story of the Institution of Civil Engineers: Thomas Telford, 1988.

- R. W. Clark, Einstein: Hodder & Stoghton, 1996. (A bit slow at times)
- A. I. Miller, Empire of the Stars: Little Brown, 2005.
- M. Smith, Station X: Channel 4 Books, 1998.
- R. Holmes, The Age Of Wonder: Harper Press, 2008.
- D. Bodanis, E = MC2 : Macmillan, 2000.
- A. Smith, Moon Dust: Bloomsbury, 2005.
- B. Bryson, A Short History of Nearly Everything: Random House, 2004.
- D. Sobel, Longitude: Fourth Estate, 1998.
- D. Berlinski, A Tour of The Calculus: The Philosophy of Mathematics: William Heinemann, 1996.
- D. Bodanis, Electric Universe: Abacus, 2006.

Lots of others in this list now as pop-sci has had an explosion of interest in the last two decades.

Chapter 12. Power Electronics

Chapter 13. Machines

Chapter 14. RF Microwaves and EMI

Chapter 15. Control Systems