

Characterisation of Geiger Mode APDs

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This work is dedicated to Richard Rhodes. A friend and peer, who graduated from this university in July. Richard passed away on the 18th of August after a motorcycling accident.

Abstract

Excess noise measurement of avalanche photodiodes (APDs) is required in the region of 10MHz. Present systems use operational amplifiers. The APD junction capacitance causes a significant problem. This report discusses the design of a discrete transimpedance amplifier (TIA) using a common base connected transistor. The present measurement system is discussed and pertinent literature is reviewed. The relative merits of operational amplifiers and transistors with respect to TIAs are discussed. A circuit optimisation is given allowing acceptable frequency response to 20MHz with APD junction capacitance of 200pF. Noise is considered and estimated. Testing and biasing methods are discussed and prototype circuits reviewed.

Acknowledgements

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Thanks to my parents for supporting me. Finally thanks to my girlfriend Pippa for being generally fantastic and for not running away when I ramble on about the un-ending annoyances of high frequency circuits.

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1. Introduction

1.1. Optical Networking

Optical fibre networks are the ‘backbone’ of most medium and large companies, universities, institutions, governmental organizations and the internet. ‘Media companies’ such as the Virgin Media Group must offer new services regularly to avoid loosing custom to their competitors.

The accessibility of information, combined with the continual advancement of content technologies, such as video to mobile devises and high definition television require higher bandwidth networks. The continual development of optical communication networks is necessary to meet demand. At present 10 Gb/s optical fibre networks are standard, 40 Gb/s are being developed and 100 Gb/s are forecast.

1.2. Detectors and Measurements

Avalanche photodiodes (APDs) are preferable for use as detectors in long haul (>100km) networks, due to increased sensitivity [1] [2]. As a result of the mode of operation excess noise is generated. The noise is of interest in a 4MHz bandwidth centred on 10MHz. The APDs grown at Sheffield for research purposes have differing values of junction capacitance. This capacitance acts to destabilise the first stage of the present measurement system. And cause a peak in its response in the region of interest. The purpose of this project is to design, fabricate and verify the operation of a stable, capacitance invariant, low noise TIA. And use it to measure APDs.

2. Literature Review

The present state of research is summarised here. First, APDs are discussed in order to appreciate the origin of problems faced by the present system. Next the existing measurement system is outlined. Then single transistor circuits and bandwidth enhancement are considered. Finally noise sources in transistors are discussed. Several other papers make interesting background reading but are not worthy of comment [3] [4] [5] [6] [24].

2.1. Avalanche Photodiodes

The APD is a two terminal semiconductor device. It is used to convert light signals into an electrical current.

2.1.1. Theory of Operation

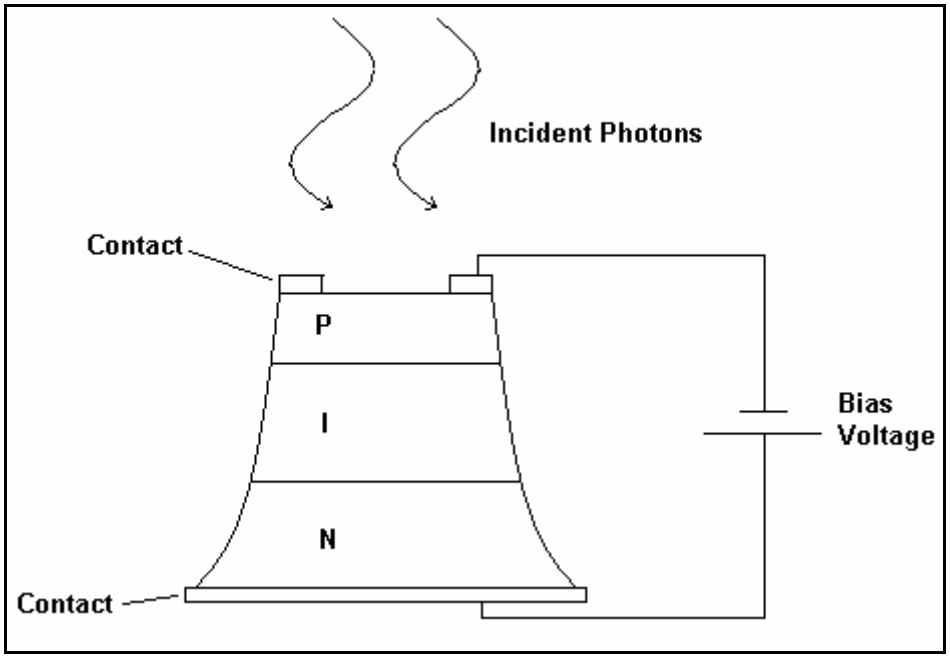


Figure 1: Reverse Biased PIN Diode [7]

The device is shown in cross section (Figure 1). The intrinsic layer may be doped lightly n-type. The PIN structure is only an APD when biased into the region of reverse breakdown. In this mode, photons enter through the p-type region and electron-hole (e-h) pairs are created. The photon looses energy equal to the band gap and promotes an electron. The electron is swept into the intrinsic region and the hole 'moves' towards the negative end of the cell. The first electron may collide with the lattice, promoting another electron and

loosing velocity. The result is two low velocity electrons. This process is termed impact ionisation. The electric field in the intrinsic region is large and the electrons are accelerated again. Eventually they will collide with the lattice and promote more electrons. This process is shown diagrammatically in [8]. Due to impact ionisation, the APD appears to have current gain.

2.1.2. Small Signal Equivalent Circuit

The interaction of the APD with the existing measurement system is a primary concern. In order to perform circuit analysis a small signal model (Figure 2) of the APD is required.

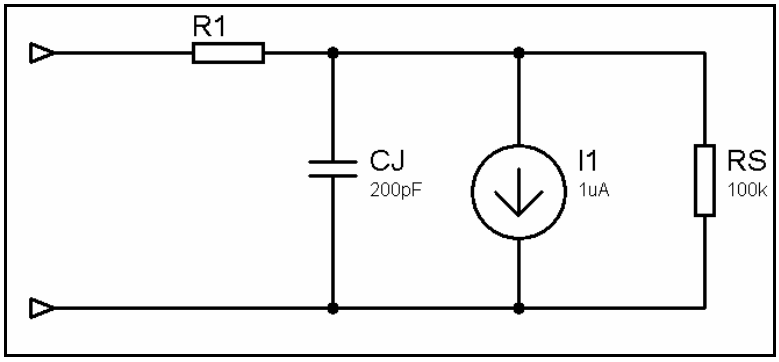


Figure 2: Small Signal Model of APD [9]

In Figure 2 the current source I_1 represents the current due to generation of e-h pairs and impact ionisation. The value of I_1 is proportional to the device efficiency, current gain and the incident luminous flux. The resistor R_S is the equivalent (Norton) source resistance of the device. The value of R_S is around 100kΩ. R_1 is the bulk resistance of the semiconductor and the contact. It is the resistance seen by an electron generated in the device when leaving to flow in an external circuit. The bulk resistance can be neglected for most samples. c_j is the capacitance formed by the mobile charge in the device and the junction depletion width. This capacitance interacts with the present measurement system [10] [11] [12], this is discussed later.

2.1.3. APD Noise

The components of the APD noise are of interest, and it is useful to understand the origins of the sources. In the frequency region of interest the noise seen at the terminals of the APD has principally three sources.

2.1.3.1. Shot Noise

Shot noise affects all semiconductors carrying a DC current. It is defined as $I_{sh} = \sqrt{2 \cdot e \cdot I_{bias} \cdot \Delta f}$ [1][13]. It is due to the quantum nature of current passing across a barrier. It affects all frequencies equally (it is spectrally white) and is irreducible.

2.1.3.2. Excess Noise[2]

There is excess noise [14] also called avalanche noise [15] produced by the APD. This noise arises from the impact ionisation process and is spectrally white. e-h pairs are generated by photons entering the semiconductor and promoting an electron. The point of creation affects the time taken for the electron to leave the device. This causes the current leaving the device, due to a continuous non-varying luminous flux, to have a DC component and a white noise component. This is the dominant noise source [16]. It is also the source under investigation. Excess noise is related to shot noise [14].

Excess noise can be modelled using Monte Carlo techniques. Several models based on device physics exist, however they have shortcomings [17]. Noise models can be split into local and non local. Non local noise models consider the carriers past. In the discussion above, after the second ionisation event there are two *low velocity* electrons in the lattice. No ionisation can occur when the velocity of the electron is too low. It must first be accelerated by the high electric field. The minimum possible space between ionisation events is called ‘dead space’. Local models do not take account of this. Instead it is assumed that the probability of an ionisation event is equally likely at all times.

2.1.3.3. Thermal Noise

The APD operates above absolute zero therefore it must have an associated thermal noise. Thermal noise is caused by the random motion of carriers [18] and is spectrally white.

---

[1] e is the electronic charge I_{bias} is the DC bias current and Δf is the bandwidth of measurement

[2] In the discussion electrons are considered, however holes are also accelerated, in the opposite direction, by the high filed and can cause ionisation events.

2.2. The Present Measurement System

The existing measurement system is described. This is necessary to understand the design criteria for the new TIA. A comprehensive summery of different detection methods, used by previous researchers, is given in [19].

2.2.1. System Overview

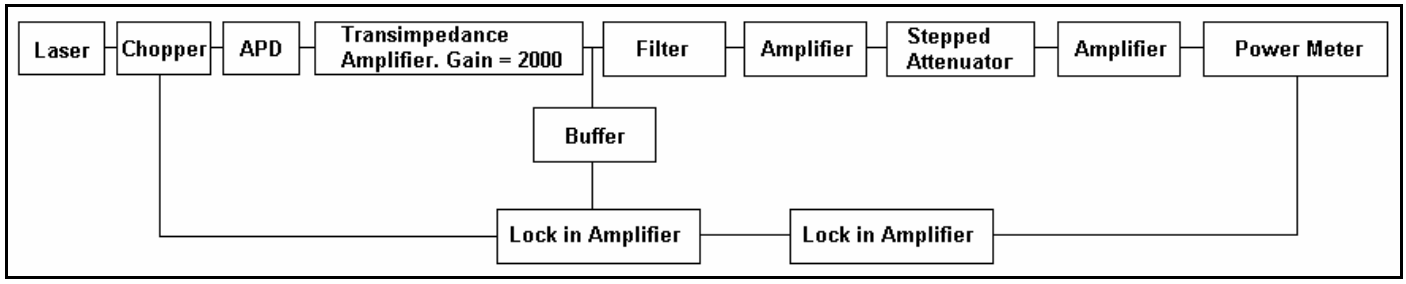


Figure 3: Measurement System Diagram [20]

The above diagram shows the measurement system. The laser, chopper, APD, and lock in amplifiers (LIAs) form the phased locked detection. At the output of the TIA there will be a continuous noise due to the TIA and APD shot and thermal noise. Superimposed on this will be a square wave of around 180Hz containing the APD excess noise. Figure 4 shows an example of the expected output. The filter which follows is band pass, the pass band lies between 7.9MHz and 12.1MHz. The filter minimises the possibility of flicker noise [21] entering the measurement system. Amplifiers and a precision stepped attenuator follow the filter. They scale the signal so that it is suitable for the power meter.

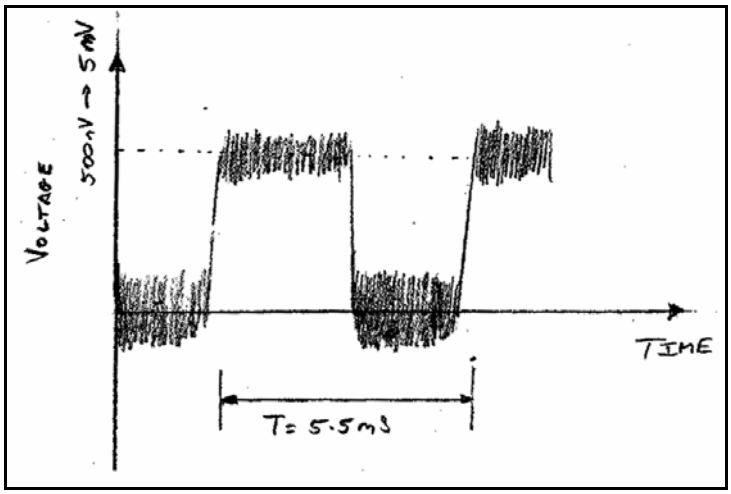


Figure 4: Example of the expected output from the TIA

2.2.2. Phase Sensitive Detection

When continuous noise signals with the same spectral density are present, it is impossible to find the noise due to individual sources. For example shot, excess and thermal noise. This is the problem faced in the APD measurements. Excess noise is present when light falling on the device generates e-h pairs. If the light falling on the device was continuous the excess noise would be indistinguishable from the other noise sources. By chopping the light, with a rotating slotted disk, the excess noise can be modulated onto the chopping frequency separating it from the other continuous noise sources. An LIA is used to recover the modulated signal. The chopper operates between 170Hz and 180Hz with a 1:1 mark space ratio.

2.2.3. Lock in Amplifier Operation

LIAs operate by the same principle as phase locked loops. An LIA is a three terminal device with two inputs. One input is supplied with the signal from the chopper, which acts as a reference. The other is supplied with the signal containing the noise from the APD. These have the form $V_r \sin(\omega_r + \theta_r)$ and $V_s \sin(\omega_s + \theta_s)$ respectively. These expressions are multiplied together by the LIA. The result is $V_o = 0.5V_sV_r - 0.5V_sV_r \cos(2\omega_s t + 2\theta_s)$[22] it contains a DC term proportional to $V_r \cdot V_s$ and a term at twice the chopping frequency, which is ignored.

2.2.4. The Operational Amplifier based TIA

The present TIA makes use of an operational amplifier in the following configuration (Figure 5)

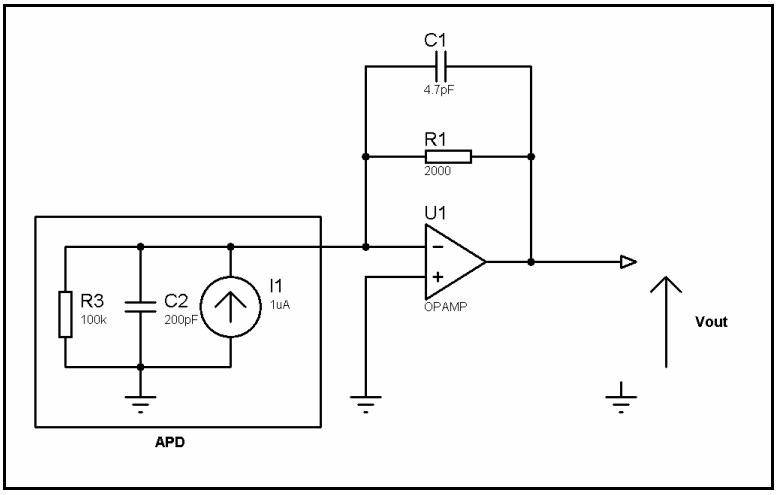


Figure 5: Existing Op Amp Based TIA

The transimpedance gain is set by R1. The op amps in use are externally compensated this allows the designer some control over the bandwidth and stability. C_1 is the compensation capacitance. I_1 c_2 and r_3 form a modified small signal model of an APD. Blocking capacitors and biasing components are omitted for clarity. It is shown in [23] that the junction capacitance of the diode and the feedback capacitance of the op amp interact. The result is a gain peak in the region of interest. The same reference shows that the output noise of the TIA varies over the range of interest. Both characteristics are undesirable.

2.3. Bandwidth Enhancement Techniques

A common [24] [25] bandwidth enhancement technique is compensation. Compensation is the cancelling of an unwanted characteristic by the addition of elements or networks. A tuned load (in a transistor amplifier) is an example of compensation. For a standard case treated in several texts [26] [27] [28] an inductance is added in parallel with a capacitance (Figure 6). The bandwidth is defined by the q of the load. The resonant frequency is given by L_1 and C_1. The use of a tuned load with a transistor is shown in [29] & [30].

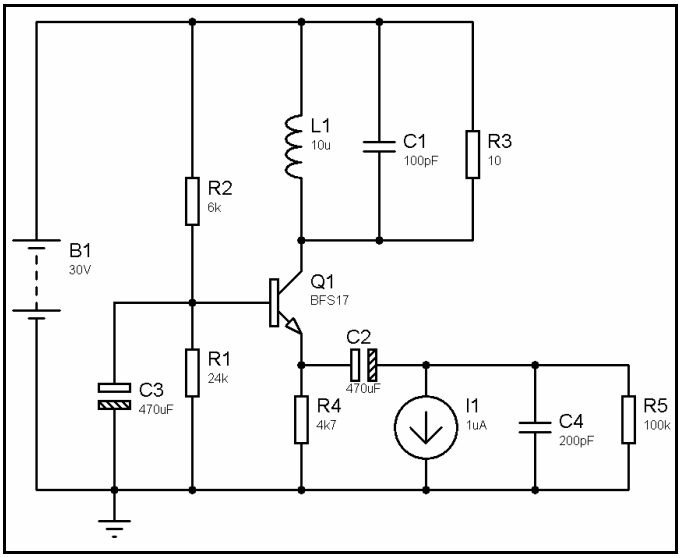


Figure 6: Shunt Peaked Common Base Amplifier

An interesting double tuned amplifier is presented in [31]. A tetrode (U_1) is shown with an LC load (Figure 7).

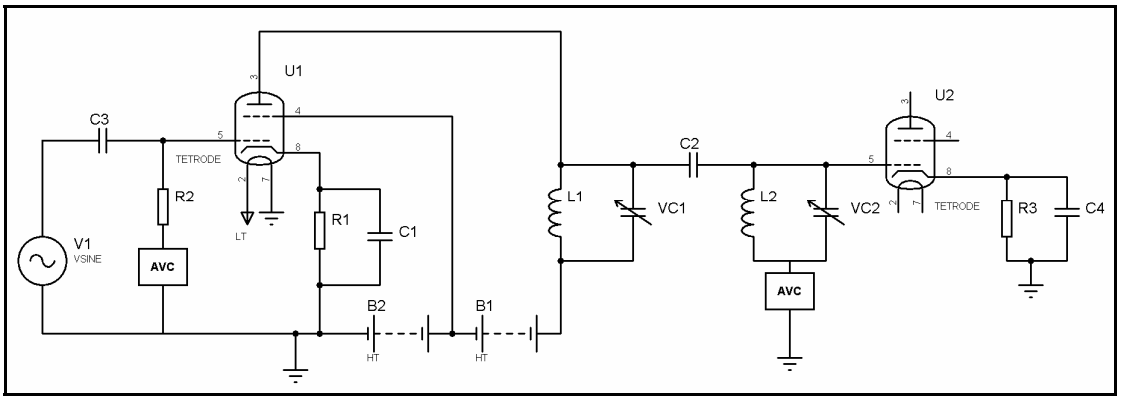


Figure 7: One of Barden's Patent Diagrams [31]

This stage is AC coupled to another common cathode stage. The impedance from the grid to ground in the second stage is set by a parallel LC network[3]. This interacts with the load of the first valve. A small signal model can be used to show this more clearly. The patent claims that the two networks are used to extend the width of a pass band. The grid LC network should be tuned to the lowest frequency of interest and the anode network should be tuned to the carrier frequency.

[3] In the patent [31] Automatic Volume Control is shown. It can be ignored for this discussion. It appears due to the authors' use of a radio receiver as an example use of his invention.

More recent texts [32] cover double tuned amplifiers. However in this reference the tuning networks are discussed in terms of coupled inductances. Neither the coupled inductance tuning nor Figure 7 are suitable as they are band pass techniques. They are interesting because the networks can be made low pass.

In a recent paper [33], a summery of bandwidth enhancement techniques is given for amplifiers with two and four terminal loads. This paper gives the theoretical limit of the bandwidth enhancements discussed.

2.3.1. Two Terminal Loads

In Figure 8 a BJT model is shown with its parasitic output capacitance (c) and output resistance (r). The bandwidth is limited by the capacitance. The gain bandwidth product (GBP) is $\frac{gm}{2\pi \cdot c}$. The gain falls due to the dominance of the capacitive reactance. That is the impedance of c in parallel with r falls as frequency tends to infinity. It is approximately equal to X_C when X_C is much less than r.

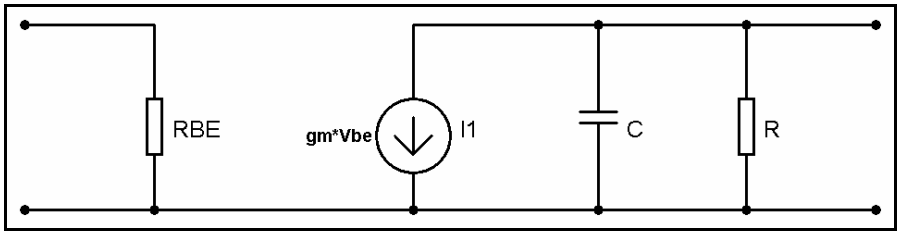


Figure 8: Standard Transistor Small Signal Model

To enhance the bandwidth a network can be added in parallel with the output. Lumping the elements into an impedance (z) it can be shown as Figure 9.

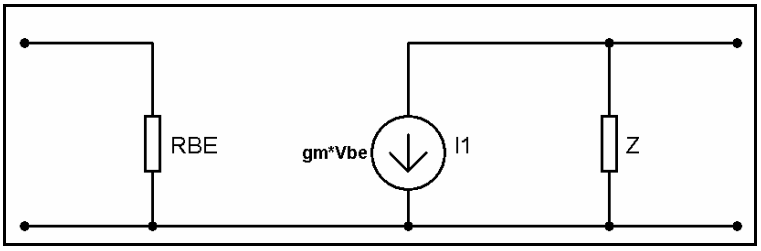


Figure 9: small signal model as above with C and R appear inside 'Z'

The maximum enhancement of this arrangement is given by the Bode-Fanno limit $GBP_{\max} = \frac{gm}{\pi \bar{c}}$ where $\bar{c} = \lim_{\omega \to \infty}\left(\frac{1}{j\omega z}\right)$ z is an impedance function. It is the transfer function of the network including the parasitic capacitance (c). Comparing the GBP originally stated and the Bode-Fanno limit, an enhancement factor of two is theoretically possible.

2.3.2. Four Terminal Loads[4]

In Figure 10, r_1 and c_1 are elements of the transistor. c_2 and r_2 are input elements of the next stage. The bandwidth is limited by the capacitances. The GBP is $\frac{gm}{2\pi(c_1 + c_2)}$. c_1 and c_2 can be separated by a passive network (Figure 11). Separating the capacitances reduces their effect and increases bandwidth.

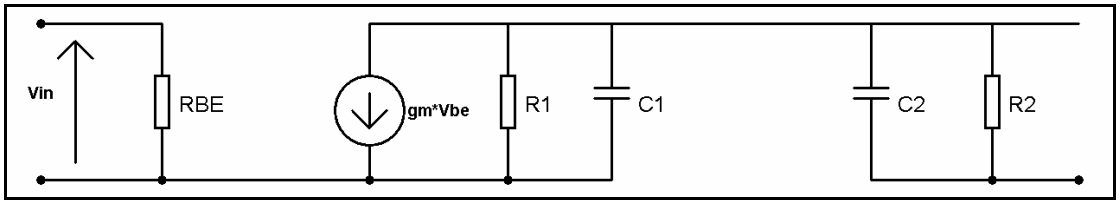


Figure 10: Small Signal Model of Untuned Amplifier and Next Stage Input Network

In Figure 11 r_1, c_1, c_2 and r_2 are the same as in Figure 10. The block N(jw), c_1 and c_2 form a four terminal network. The separation of c_1 and c_2 changes the maximum GBP to $\frac{gm}{\pi \cdot C_1}$. Using a constant - k ladder network with $c_1 = c_2 = c/2$ can enhance the maximum GBP to $\frac{gm}{\pi \cdot C}$. When compared with the earlier case of Figure 10, and given the design restriction of capacitances ($c_1 = c_2 = c/2$), the bandwidth is enhanced by a factor of four.

[4] Cherry & Hooper, "Amplifying Devices and Low-Pass Amplifier Design", Wiley, 1968, pgs 631 - 725 may also be of interest.

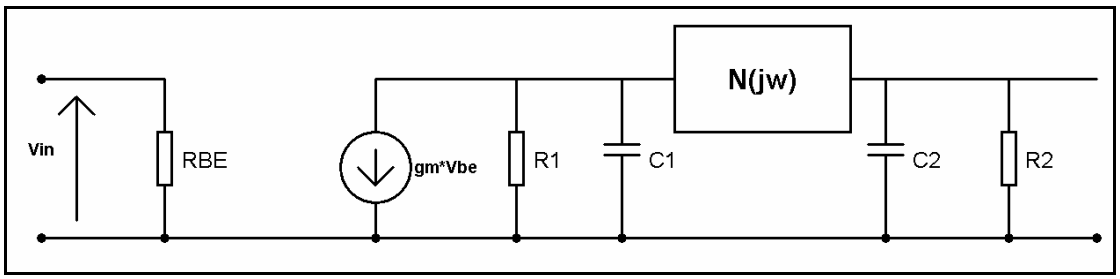


Figure 11: Small Signal Model of General Load Network

2.4. (Amplifier) Noise

The noise produced in the first stage of a measurement system of greatest importance. Signal to noise radio is heavily dependant on the noise of the first stage. Noise produced in the first stage will be amplified by all the stages that follow. Leach [13] gives a comprehensive summery of noise sources in various common devices and their treatment during design. Noise in amplifiers and feedback amplifiers is discussed. The frequency dependence of noise in devices is considered. Several texts are devoted to noise including [21] and [34][5]. Noise is also discussed briefly in [15].

2.4.1. En-In Noise Model

Chapters 2 and 5 of [34] include a discussion of the standard amplifier noise model, and of the noise sources in transistors respectively.

In Figure 12 a noiseless amplifier with input impedance Z_{in} is shown. Connected to it are two sources E_n and I_n which represent the noise of the amplifier. A source resistance and a generator to represent its thermal noise is shown. Finally the signal source is included.

[5] [34] is preferred by the author over [21]

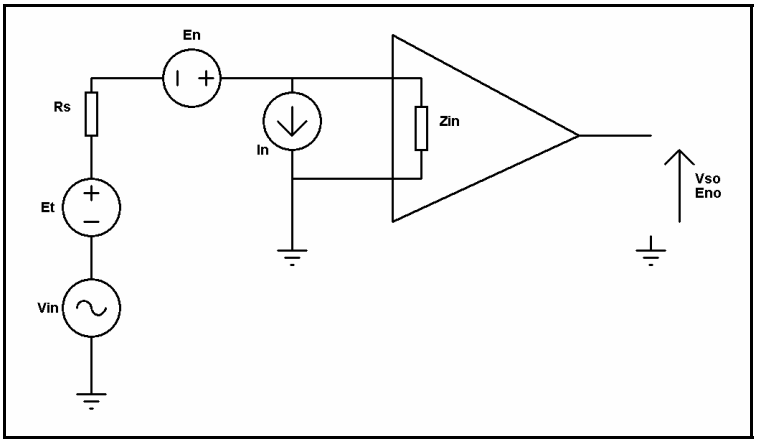


Figure 12: Standard Noise Representation of an Amplifier

The E_n –I_n model of noise is preferred to modelling each noise artefact in the small signal model (of for example a transistor) separately. It is preferred for design purposes because the signal to noise ratio is easily found when the noise is referred to the input.

The E_n-I_n noise sources can be reduced to one equivalent input noise power[6] [35] (E_{ni}^2). $E_{ni}^2 = E_t^2 + E_n^2 + I_n^2 R_s^2$ The terms on the right are shown in Figure 12.

The signal to noise ratio is then $\frac{Input_Signal_Power}{E_{ni}^2}$

2.4.2. Noise Factor / Figure

Noise factor is a number given on datasheets such as [36]. It is a measure of quality of a system (e.g. an amplifier or network). The noise factor is defined

$$F = \frac{Total_Output_Noise_Power}{Output_Noise_Power_due_to_the_Thermal_Noise_of_the_Source_Resistance}$$

It is also the ratio of the input signal to noise ratio and the output signal to noise ratio. $\frac{Si/Ni}{So/No}$. A value close to one is desirable. Noise figure is the noise factor given in decibels $NF = 10\log_{10}(F)$. Noise figure (or factor) can be used as a method of comparing impedance matched systems for a low noise design. A value close to 0dB is desirable.

[6] The equation stated for E_{ni}^2 is true if the noise sources are uncorrelated.

2.4.3. BJT Noise

The hybrid π BJT model can be extended to model noise for a common emitter stage (the source resistor is base to emitter and the emitter is treated as the common terminal) Figure 13.

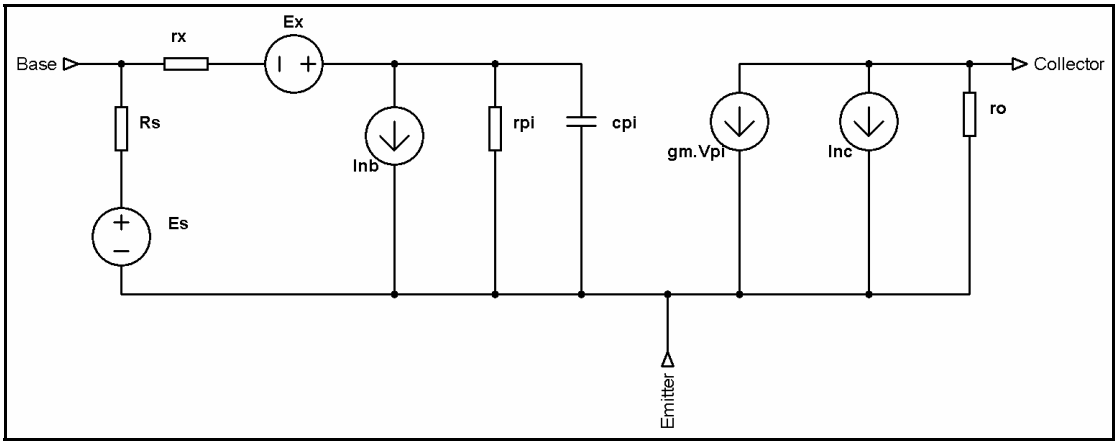


Figure 13: h-π BJT model with noise sources [37]

With reference to Figure 13, r_x is the base spreading resistance. It is the resistance from the leg of the package to the active part of the (lightly doped) base region. E_s is the thermal noise voltage of the source resistance r_s. E_x is the thermal noise voltage of r_x. I_{nb} is the shot noise for the base emitter junction. r_π is the resistance across which the controlling voltage, V_π, is developed. c_π is the input capacitance. gmV_π represents the gain of the device. I_{nc} is the shot noise for the collector base junction. r_o is the output resistance. r_π and r_o are not real resistances. They match the observed device characteristics to the model. They do not have thermal noise associated with them.

In Figure 13 the collector to base feedback components have been omitted as has the flicker noise source. Flicker noise has a 1/f characteristic; it is a low frequency effect and can be disregarded. From [38]:

$$E_x^2 = 4kTr_x$$
$$I_{nb}^2 = 2qI_B$$
$$I_{nc}^2 = 2qI_C$$
$$E_s^2 = 4kTR_s$$

To find the signal to noise ratio E_{ni}^2 is first found. The noise sources are referred to the input. That is, the gain of the stage is found and the output noise is divided by it.

$$E_{ni}^2 = 4kT(r_x + R_s) + 2qI_B(r_x + R_s)^2 + \frac{2qI_C(r_x + R_s + r_\pi)^2}{\beta_0^2} + 2qI_C(r_x + R_s)^2\left(\frac{f}{f_T}\right)^2$$

The first term is the thermal noise of r_π and R_s. The second is the base emitter shot noise. The third term is the low frequency collector base shot noise. The last term models the collector base shot noise at high frequencies.

To obtain E_n the noise due to the source resistor R_s is removed from the above equation for E_{ni}^2.

$$E_n^2 = 3kTr_x + 2qI_Br_x^2 + \frac{2qI_Cr_\pi^2}{\beta_0^2} + 2qI_Cr_x^2\left(\frac{f}{f_T}\right)^2$$

I_n is given from the method described in [38] as:

$$I_n^2 = 2qI_B + \frac{2qI_C}{\beta_0^2} + 2qI_C\left(\frac{f}{f_T}\right)^2$$

From the equation for E_{ni}^2 and the relationships given in the previous section the signal to noise ratio or noise factor can be found.

3. Common Base Bipolar Junction Transistor Connection

The common base amplifier is a current buffer. In the next two sections the large bandwidth (cf. common emitter) and low input impedance will be exploited to produce a wide band, low noise, current driven amplifier. This section deals with the resistively loaded common base circuit and a circuit realisation of an APD model. The problems associated with injecting and retrieving signals are discussed in Section 4.

3.1. Resistive Loaded Common Base Amplifier

The T model is used in [30] [39] [40] to treat the common base amplifier. The hybrid π model is preferred and is used throughout. A standard common base connection with an APD model is shown in Figure 14. The input is applied at the emitter, the output taken from the collector. R_2 and R_3 bias the device. C_3 grounds the base, giving the stage its name.

The common base amplifier does not suffer the miller effect. This is the main cause of HF roll off in the common emitter topology. Because the base is signal ground, the collector to base capacitance can be moved from its usual position to that of Figure 15.

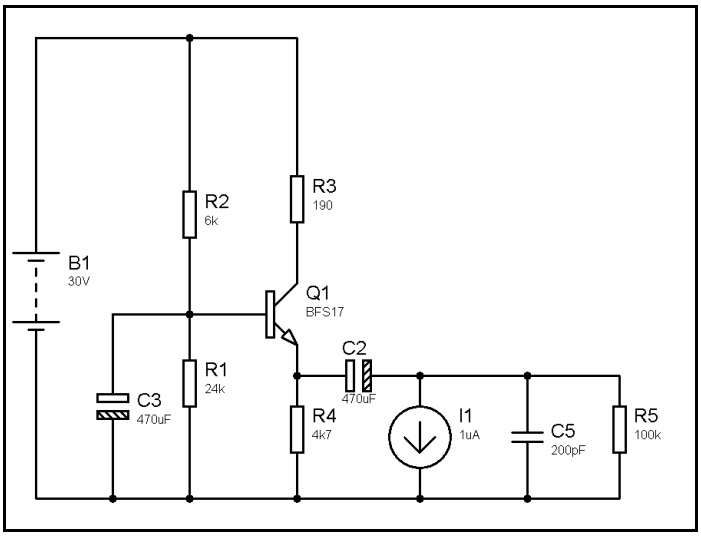


Figure 14: Resistively Loaded Common Base

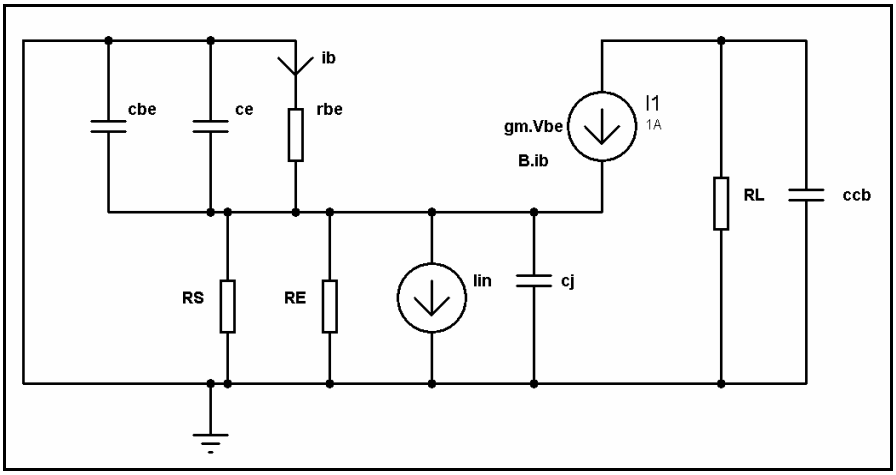


Figure 15: Common Base with APD Hybrid pi Small Signal Model

This small signal model can be reduced further to Figure 16.

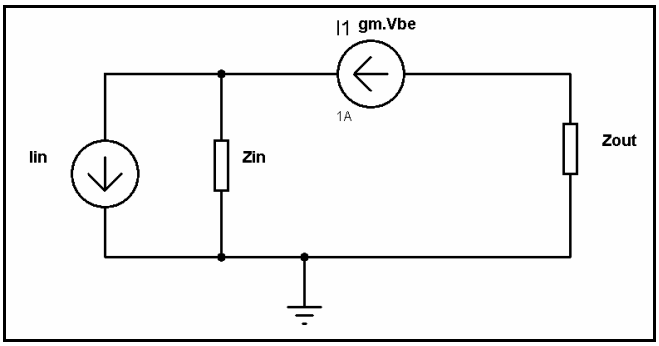


Figure 16: Reduced Common Base Small Signal Model

Z_{out} and Z_{in} are the resulting impedances of lumping the paralleled components at the input (emitter - base), and output (collector - base) terminals. The analysis given in Appendix 1.2 shows the transimpedance gain of this network is

$$\frac{V_o}{i_{in}} = \frac{gm \cdot z_{out} \cdot z_{in}}{1 + gm \cdot Z_{in}}$$

It is approximately equal to R_L (Figure 15).

3.1.1. Input Capacitance and Optimisation of Operating Conditions

When the APD junction capacitance becomes larger than the sum of the other capacitances in the input circuit ($c_j > c_e + c_{cb}$), it dominates the HF response. The largest junction capacitance considered is 200pF. This is 75 to 100 times greater than the other capacitances in a high frequency transistor such as the BFS17W.

Consideration of the small signal model (Figure 15) provides a starting point for optimisation. A pole is formed by the input capacitance and resistance. It is desirable to move the pole up in frequency. This is achieved by control of the resistances.

The method of controlling r_{be} is well defined with respect to the DC conditions. Considering the input circuit in Figure 17, the impedance of c_{be}, c_e, r_{be}, R_E and c_j is

$$Z_{in} = \frac{RE // r_{be}}{s(RE // r_{be})(c_j + c_{be} + c_e) + 1}$$

Where // signifies the parallel connection of two components. R_s is approximately 100kΩ and is neglected. r_{be} is given in terms of the operating condition by[7]

$$gm = \frac{eIC}{kT}$$

$$rbe = \frac{\beta}{gm}.$$

R_E can set r_{be} via I_C. The designer can vary R_E while maintaining I_C by judicious choice of R_1 and R_2 (Figure 14)

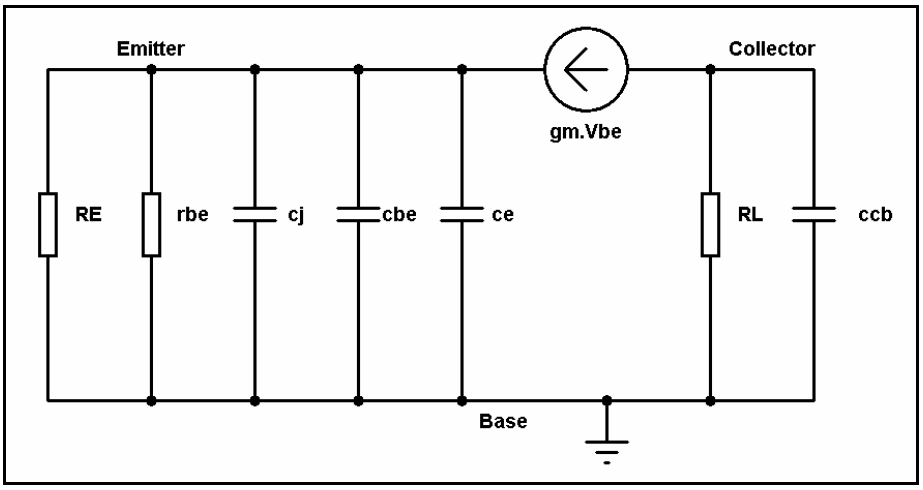


Figure 17: Rearranged common base small signal model

[7] e is the electronic charge, I_C is the quiescent collector current, k is Boltzmann's constant, T is the absolute temperature. β is the devices small signal current gain at the operating point [43].

r_{be} is made the dominant resistance (lowest, as all resistances are in parallel). There are several reasons for this. Firstly it necessitates high gm, r_e'[8] is approximately 1/gm. Low r_e' is desirable so the majority of the photocurrent flows into the transistor. Secondly, it makes the pole due to the input circuit high frequency. Lastly R_E provides stability, it should not be made as low as r_{be}. Assume V_{be} = 0.7V and V_{RE} is << 0.7V. If I_C increases (for example due to temperature rise) the increase in V_{RE} will be negligible. The collector current can rise enough to destroy the transistor. In a situation where V_{RE} is significant with respect to V_{be} (e.g. V_{RE} > 2V), a rise in I_C will increase V_{RE} by a significant amount. V_{be} must fall as V_{R1} is constant (Figure 14). This turns the transistor off slightly, reducing I_C.

R_E should be greater than re' to avoid significant photocurrent flowing to ground. The choice of R_E is limited. It contributes thermal noise at the input. If I_C is to be maintained through an increasing resistor value the voltage across that resistance must rise. The supply rails will eventually limit the value. Figure 18 shows the effect of I_C on frequency response. A value of I_C greater than 1mA is satisfactory. This figure is generated using the small signal transfer function in Appendix 1.2

Transition frequency [41] provides another way of finding a high bandwidth operating point.

$$f_T = \frac{eIC/kT}{cbe + ce + ccb}.$$

It is preferable to obtain a high transition frequency. From the equation, larger collector current is desirable. It is not possible to extend the transition frequency indefinitely [42]. The optimum value of I_C (for maximum f_T) is sometimes graphed on datasheets [43]. Noise generally requires low DC currents. This is discussed shortly.

[8] r_e' is the impedance looking into the emitter of a transistor. Its value is derived in Appendix 1.1

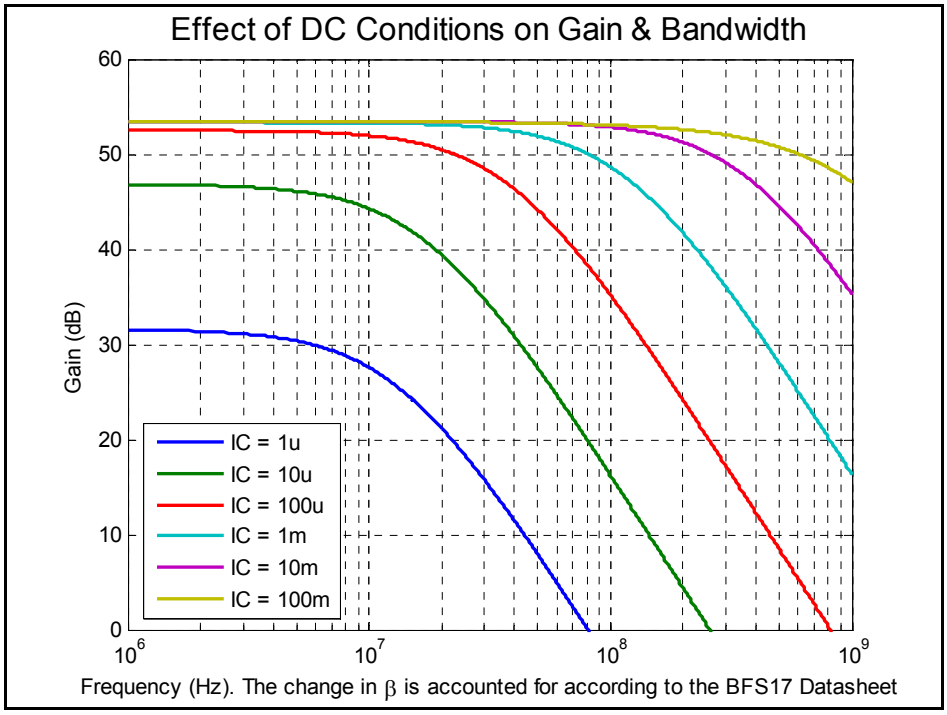


Figure 18: Graph showing the effect of DC conditions on frequency response. Modelled with the transfer function given in Appendix 1.2

3.1.2. A Circuit Realisation of an APD Model

A model of an APD is used to characterise the TIA. The network analyser swept source is considered a perfect voltage in series with 50Ω. The APD small signal model is a current source (Section 2.1.2). A large resistance is used to convert the voltage in to a current. A high frequency model of a resistor in a 1206 package is the resistance in parallel with approximately 1pF of capacitance. There is also a small inductance in series with the resistance. It has not been found necessary to include it[9].

An experiment was conducted to find the parasitic capacitance. In Figure 19 the voltage at R6 & R7 was measured. Measuring with a 50Ω probe at this point loads the circuit; however the relevant information is the shape of the graph. The resulting graph (Appendix 1.3) has a first order rise in magnitude at the frequencies where the parallel capacitance dominates the resistance. In practice only a small portion of this rise is visible. Artefacts, due to the length of the HF connecting cables, hide the circuit response. It is not favourable to measure at the emitter. At this point the resistance to ground is approximately

[9] The 1206 resistor is inductive below a few hundred ohms. Above this it is capacitive [51].

5Ω. Noise swamps the signal when attempting to measure the voltage developed by the small current across this resistance.

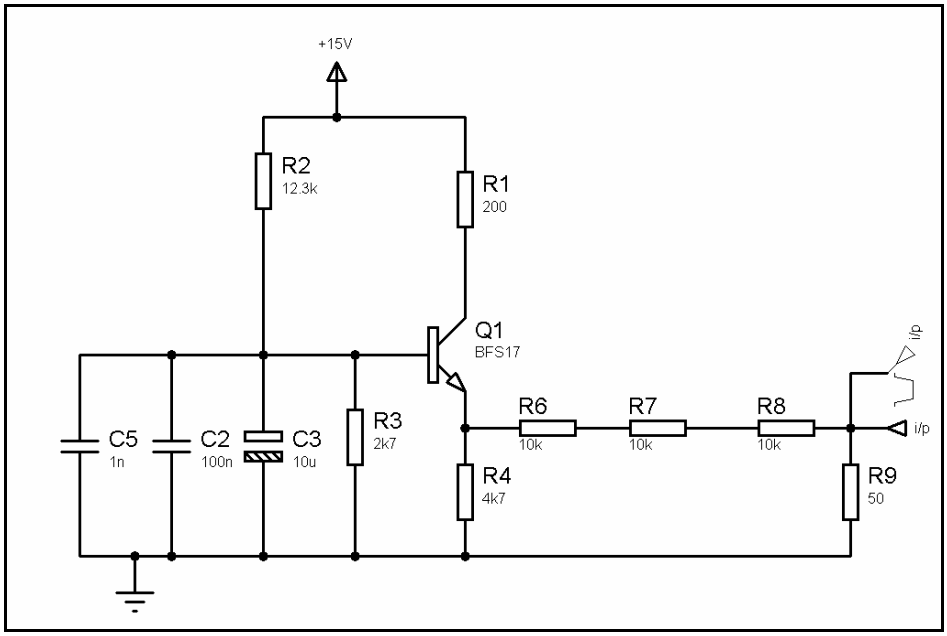


Figure 19: Common base circuit and resistor chain

The parasitic capacitance in Figure 20 was incremented until the simulated response (measured at C5(2)) closely matched that observed in testing.

The 5Ω resistor (R7) represents re'. R5 is the source resistance. R6 is the terminating resistor and C10 its parasitic capacitance. R1, C4, R2, C5, R3 and C1 form the voltage to current resistors and parasitic capacitances.

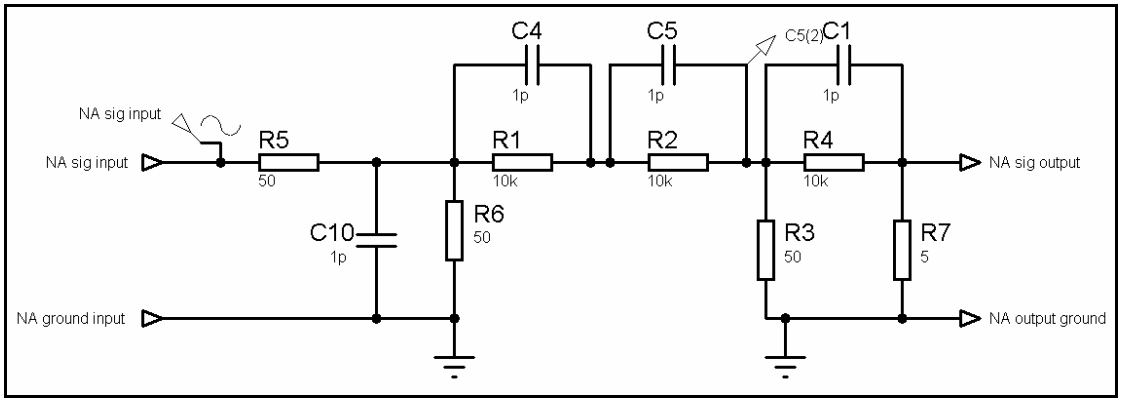


Figure 20: Simulation of parasitics affecting the voltage to current circuit

This circuit was simulated for parasitic capacitances between 0.5pF to 1.5pF. The result suggests a value between 1pF and 1.2pF. The experimental and simulation data is located in Appendix 1.3

It is necessary to obtain a result which is not obscured by noise. It is also necessary to avoid the resistor chain affecting the response of the amplifier. Two methods have been considered to determine the most suitable resistance value for the chain. The first is to cancel the inductive and capacitive effects of the resistors by judicious choice of resistance and by various parallel and series connections. The other is to reduce the resistance. This increases the frequency where the capacitance becomes a problem. The successful method appears to be the latter. Simulating[10] three 2.2kΩ resistors gives a response which rises by 0.3dB from its mid band value by 20MHz, and by 0.08dB at 10MHz. The low value of resistance necessitates a small input voltage. To cause 1μA to flow into the emitter of the transistor the input voltage should be 6.6mV. Noise is visible on the result. It is averaged over 16 sweeps to lessen the effect.

3.1.3. Gain Bandwidth Restrictions

The transition frequency (f_T) of a transistor is a figure of merit relating to gain and bandwidth. The transition frequency of a transistor can be considered similar to the gain bandwidth product of an op amp. A higher gain circuit will have less bandwidth. The transition frequency is related to the transit times of the carriers across the device junctions and the cross sectional capacitances. The largest possible gain should be achieved. A substantially flat response is required from 200Hz to 20MHz. SPICE demonstrates graphically the trade off between gain and bandwidth when load resistance is stepped and the frequency response plotted[11] (Appendix 1.4).

3.2. Compensation, Neutralisation: Bandwidth Enhancement Techniques

A part of the early work of this project was based on [44]. That work is on a common base TIA designed with a compensation network as the load. This network may take a form such as Figure 6 and is described in [44] as neutralisation. Williams [45] does not reveal the problem with the terminology. But Terman [46] gives a more precise definition of neutralisation. It appears

[10] $c_{paracitic}$ = 1.1pF

[11] In this simulation the quiescent reverse bias of the collector - base junction is decreased as R_L is incremented. This increases junction capacitance by reducing the depletion width. c_{cb} is not the dominant capacitance the error is not significant.

that neutralisation must include some feedback mechanism as Terman describes it in terms of energy transfer. A compensation network increases the HF gain by increasing the load impedance at HF in order to compensate for the loss in gain due to the unwanted capacitance. This does not require feedback and so is not neutralisation.

3.3. Noise

The noise contribution of the first stage is of critical importance. It sets the SNR (signal to noise ratio) for the rest of the system. A Noise analysis was undertaken after the design of the common base TIA was found acceptable in terms of bandwidth and gain. Using SIMetrix [47] a result for the noise referred to the input of 7.97pA per root Hz was obtained using the circuit given in Appendix 1.5. The standard SPICE capacitor is noiseless, additional input capacitance has no effect in noise simulation.

3.3.1. Definition of Noise Signal to Noise Ratio

In this project the signal that is being studied is a noise signal. The 'noise signal to noise ratio' (NSNR) is the ratio of the magnitudes of the noise signal of interest (APD) and the unwanted noise of the TIA.

3.3.2. Published Commentary on Common Base Circuit

Grey describes the common base stage as "generally *unsuitable*" [48] for the purpose described here. The noise current flowing into the collector (due to the load resistor and transistor) appears at the emitter without attenuation because $\alpha \approx 1$. This is not problematic; the value of load resistance is restricted by gain bandwidth considerations. For R_L = 500Ω the input noise current due to R_L is approximately equal to that due to the transistor[12]. Uncorrelated noise sources combine as the root of the sum of their squares. For example for two noise currents (per root Hz) I_a and I_b and a total I_t

$$I_t = \sqrt{I_a^2 + I_b^2}$$

If one noise current is three times larger than another its effect is nine times that of the former. Having neither source dominant is optimal. This is shown with a simple example containing arbitrary data.

[12] 5.977pA per root Hz for the transistor and 5.757pA per root Hz for the load resistor

Ia	Ib	It
6	0	6.000
5	1	5.099
4	2	4.472
3	3	4.243
2	4	4.472
1	5	5.099
0	6	6.000

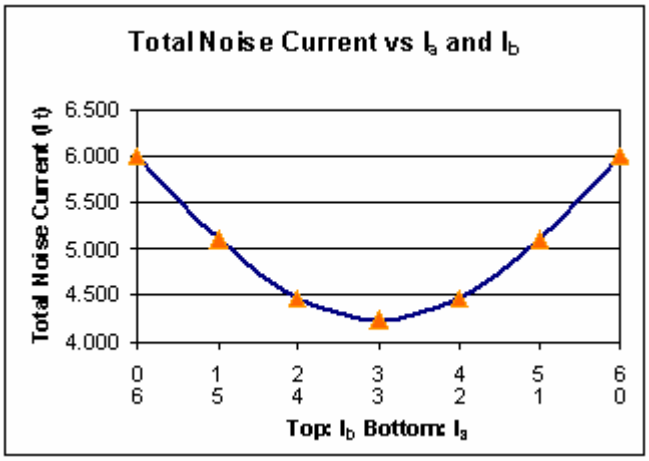


Figure 21: Optimum Noise Combination

3.3.3. Introduction to the Noise Analysis

The BJT noise is given by the DC currents and the real resistances. The noise model of the common base connection is found in [49][13]. The transistor noise mechanisms are combined as a current flowing into the collector. This is combined with the noise current flowing into the collector due to R_L, to give the 'total noise'[14]. The 'total noise' is then referred to the input.

The analysis is presented here from the point where the transistor output noise current has been found in terms of the internal noise sources. The analysis of the transistor noise mechanisms is found in Appendix 1.6 where

[13] Leach, like some other authors (see Section 3.1), uses the T model. Motchenbacher and Connelly (see References) use the hybrid π model however they do not present the common base connection.

[14] This is not literally the total noise. As the 2.2kΩ emitter resistor is neglected. This is justified in Appendix 1.6. The base biasing resistors are noisy, but are shorted to ground by a large capacitance.

small signal diagrams and an extended explanation of the analysis can also be found.

The noise current at the output of the transistor due to the thermal noise of the source resistance

$$I_{no}E_s^{\ 2} = \frac{E_s^2 \cdot \beta}{\left(r_{be} + z_b - R_s(1+\beta)\right)^2}$$

The noise current at the output of the transistor due to the Shot noise of the Base – Emitter junction

$$I_{no}I_{nb}^{\ 2} = \frac{I_{nb}^2\left(\beta \cdot \left(R_s + z_b\right)\right)^2}{\left(r_{be} + z_b - R_s(1+\beta)\right)^2}$$

The noise current at the output of the transistor due to the Shot noise of the Base – Collector junction

$$I_{no}I_{nc}^{\ 2} = \frac{I_{nc}^2\left(R_s + z_b + r_{be}\right)^2}{\left(r_{be} + z_b + R_s(1+\beta)\right)^2}$$

The noise current at the output of the transistor due to the thermal noise of the base spreading resistance

$$I_{no}E_{zb}^{\ 2} = \frac{E_{zb}^2 \cdot \beta^2}{\left(r_{be} + z_b + R_s(1+\beta)\right)^2}$$

3.3.4. Calculation of Noise Signal to Noise Ratio

Two routes are possible, a lengthy symbolic route incorporating all of the above into one equation. Or a more tractable numerical solution for a set of operating conditions. The preferred set of operating conditions[15] is known. They have been chosen by the necessity to trade gain for bandwidth. A numerical result will be pursued.

The total transistor noise current

$$I_{no}^2 = I_{no}E_s^{\ 2} + I_{no}I_{nb}^{\ 2} + I_{no}I_{nc}^{\ 2} + I_{no}E_{zb}^{\ 2}$$

$$I_{no}^2 = 5.977 \times 10^{-23}$$

The thermal noise (current) of the load

[15] The operating conditions and constants are given in Appendix 1.6.5

$$I_n R_L^2 = \frac{4kT}{R_L}$$

$$I_n R_L^2 = 3.314 \times 10^{-23}$$

Combined output noise current

$$Stage_I_{no} = \sqrt{I_{no}^2 + I_n R_L^2}$$

$$Stage_I_{no} = 8.298 \times 10^{-12}$$

Input Referred Noise

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\alpha = 0.976$$

$$I_{ni} = \frac{Stage_I_{no}}{\alpha}$$

$$I_{ni} = 8.498 \times 10^{-12}$$

The noise signal to noise ratio at the input is

$$NSNR = \frac{\sqrt{2 \cdot q \cdot 1 \times 10^{-6}}}{I_{ni}}$$

$$NSNR = 0.067$$

$$NSNR = -23.48dB$$

The noise signal is full shot noise derived from 1μA of photocurrent. If measurements can confirm this it will be approximately equal to the present system in use at Sheffield [50].

4. Biasing Circuits

4.1. Introduction

The standard common base amplifier Figure 14 is not well suited to testing APDs. Figure 22 shows the standard circuit with a large signal APD model.[16] Problems occur at the input and the output. At the input, C2 is used to block the APD bias and it forms a time constant with r_e' (5Ω). The capacitance must be large, to allow the ~200Hz chopping frequency to pass into the amplifier. This capacitor will be electrolytic. The construction and capacitance necessitates a large package. Typical dimensions for a radial, surface mount, 470µF capacitor are: 7mm radius, 7mm high on a 10mm square SMT Base. For example Rubycon TZV range of Aluminium Electrolytics. The datasheet for this range claims low impedance at 100 kHz. It is likely that above 100 kHz the impedance rises due to series parasitic inductance. The HF response of the circuit will be compromised before the signal reaches the transistor.

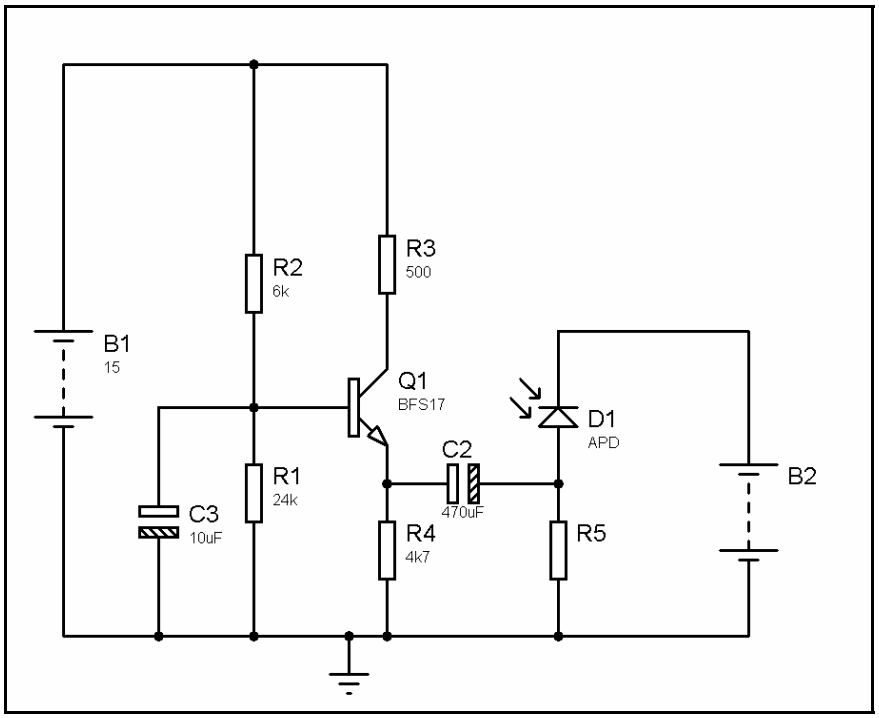


Figure 22: Common Base Amplifier with DC model of APD

[16] C_2 and R_5 are not strictly required. The APD could be DC coupled to the common base stage by connecting its anode to the junction of Q1 and R4. This will not be acceptable when the photocurrent causes significant (e.g. 0.1 x V_{be}) additional voltage across R4. I_C would be lowered, adversely affecting the HF response.

The output suffers a similar problem. A HF op amp will follow the common base stage. It is desirable to AC couple the op amp. This allows levels of gain, within the constraint of the GBP of the op amp, which would not be possible if the op amp was DC coupled. The collector has a DC potential and the supply rails are limited If an inverting connection is used a large capacitance will be required to couple the low frequency signal. R6 in Figure 23 could be made larger at the expense of HF performance. A datasheet for 1206 resistors [51] shows 100Ω as the most suitable value. The resistance could rise to 10kΩ without affecting performance. The output impedance of the common base stage is approximately 500Ω (Appendix 2.1). The loss of gain is still 5%.

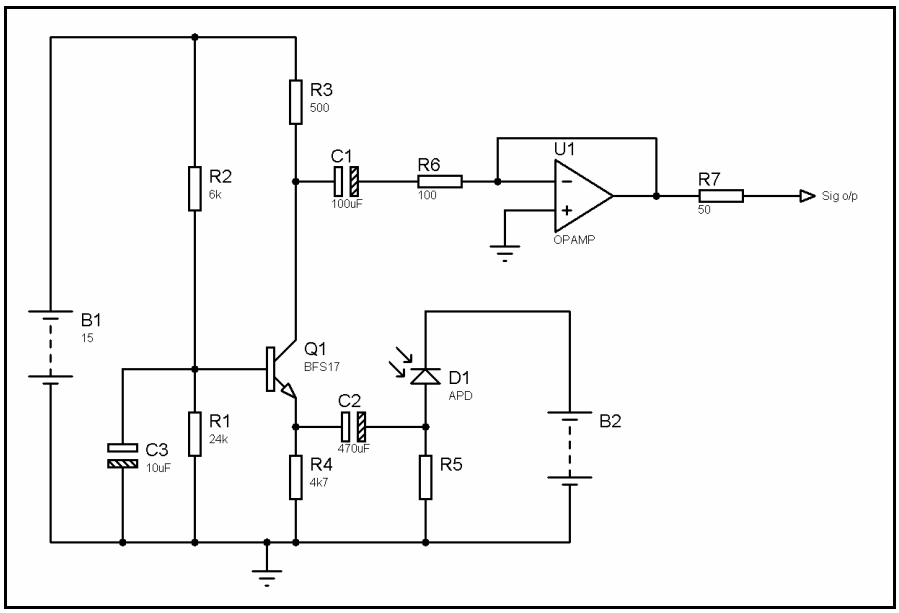


Figure 23: Driving an AC coupled Inverting Op Amp

If the op amp were non-inverting and was AC coupled a large resistance would be required to leak bias current to the input stage. This resistance must be large to avoid loading the transistor. The common base amplifier refers all noise at its output to its input without attenuation. This is a highly undesirable location for a large resistor.

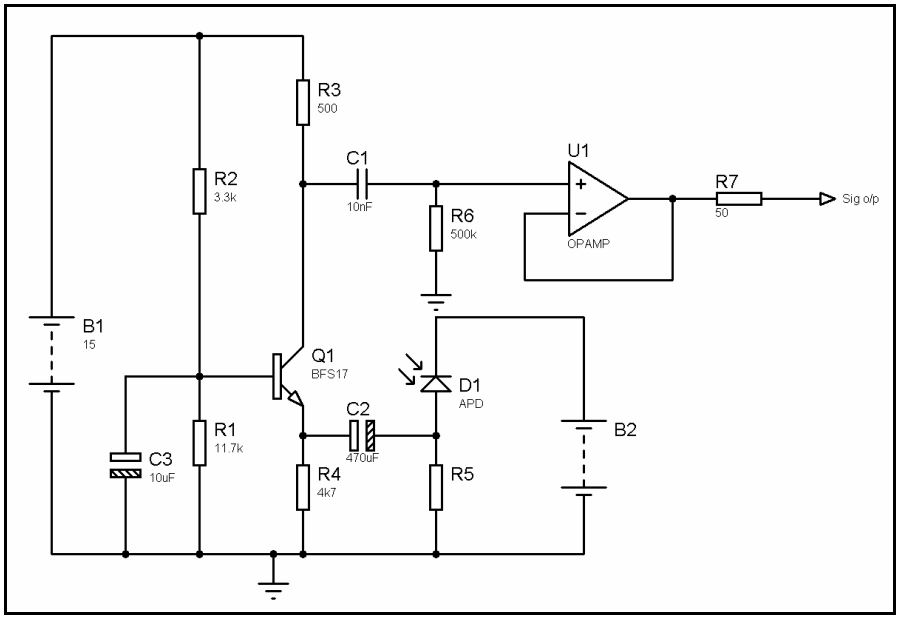


Figure 24: Driving an AC coupled Non Inverting Op Amp

It is preferable to buffer the common base output with a DC coupled op amp and then to attenuate the DC offset.

4.2. DC Output Coupling

Several methods for attenuating the DC are possible. Capacitive coupling is the simplest. The stage that is driven must be inverting and therefore will have low input impedance, necessitating a large capacitance. A 10µF chip (1206) capacitor has been adequate for testing the HF performance. Voltages close to the working voltage result in a considerable reduction in capacitance for this construction [52]; this does not matter for the purpose of HF testing.

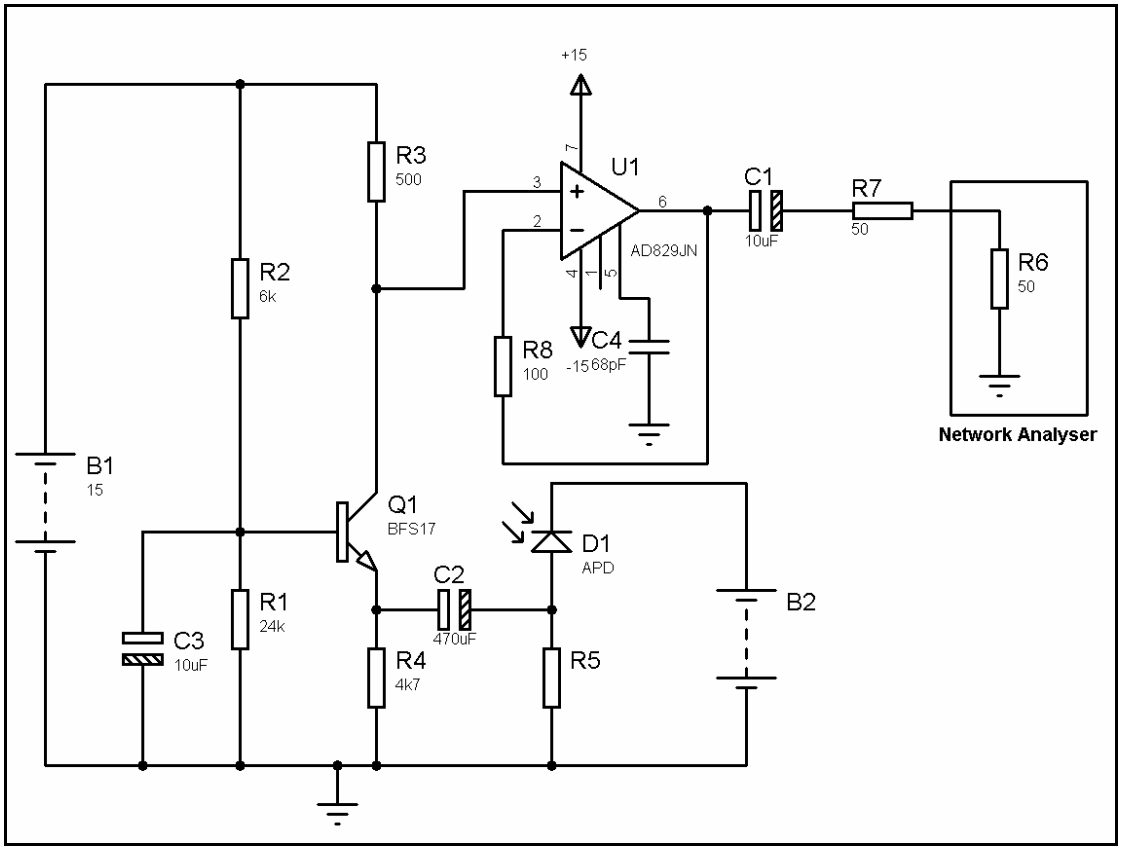


Figure 25: DC Coupled Output Buffer

In later diagrams this method can be used at lower frequencies with a smaller capacitor in place of C1 (Figure 25). There will be more amplification after C1. The stage that follows will have higher input impedance than a 50Ω probe. The use of a very small capacitance is precluded because the following stage must be inverting.

Another method to attenuate the DC is shown in the following circuit.

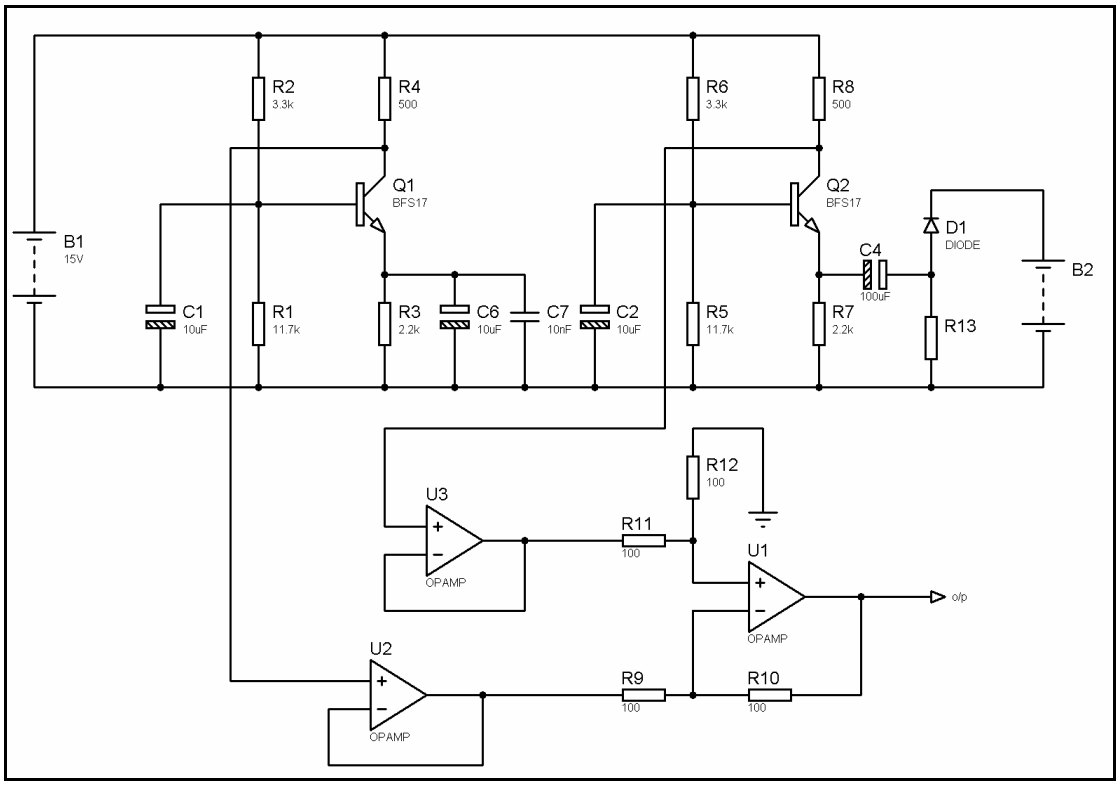


Figure 26: Reduction of DC by differential amplifier

Two common base amplifiers are shown. The input of the first (right) is ground. The second (left) is used to amplify the noise signal. After suitable buffering a differential amplifier (U1) is used to suppress the common mode (DC) signal, and amplify the differential mode (noise) signal. The action of the differential amplifier in this context could also be thought of as a level shifter. The former explanation is preferred as it shows the method of operation. The DC component can not be removed. In this case the CMMR of the differential amplifier would have to be infinite. In the capacitive coupled case the capacitor would require zero leakage current.

4.3. DC Input Coupling

It is preferable to remove the large capacitor coupling the emitter to the resistor chain (or APD). The network analyser in use has a DC coupled source. If the capacitor is removed, a considerable DC current will flow in the resistor chain[17]. One solution which has been tested uses a feedback

[17] 1.6mA for V_E=11V and R_{chain} = 6.6kΩ

mechanism to bring the input to DC ground by controlling the potential of the lower rail of the transistor stage.

The idea is shown schematically in Figure 27. Several designs failed to proceed beyond simulation. Two servo designs were tested one is a refinement of the other.

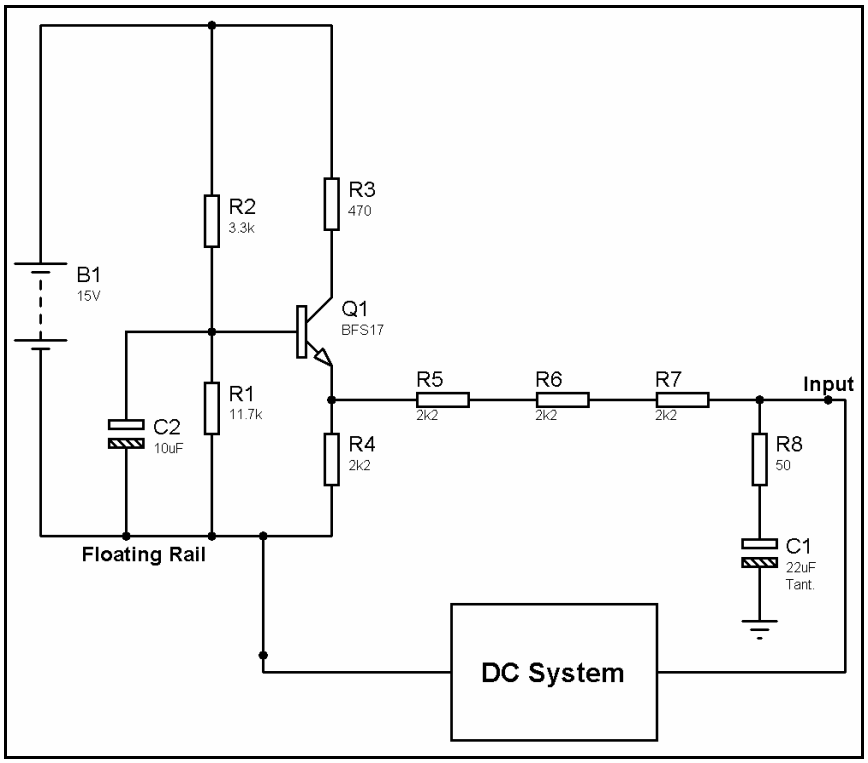


Figure 27: Controlled 'Ground' Rail Diagram

The capacitor C1 was added because there was no return path for the AC current leaving the network analyser. After this addition large phase shifts and troughs in the magnitude response were cleared.

4.3.1. Prototype Servo 1

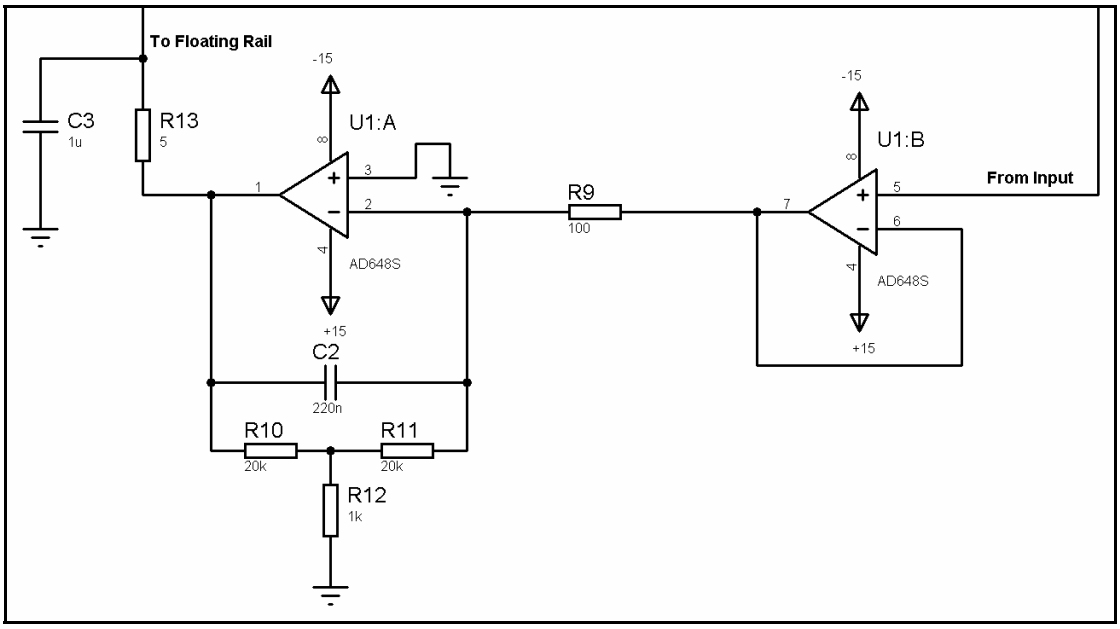


Figure 28: Prototype Servo 1 (extract)

Figure 28 shows the servo[18] section. U1:B has high input impedance. It buffers the input from U1:A. U1:A is an integrator with a current leaking resistor network [53] (R10 R11 R12). The use of this arrangement instead of a single large resistor gives lower output offset voltage. The leaking network is not required. There is a DC path from one terminal of C2 to the other without R10 and R11. This oversight is corrected in prototype servo 2. C3 is used to maintain AC ground at the floating rail of the transistor stage. Driving a large capacitance is known to cause stability problems in some op amps. To avoid this, a 5Ω resistor is included. This resistor is in the feedback loop. It does not produce an error.

This design is likely to suffer instability, although none was observed. The integrator and the RC filter both have significant phase shifts at low frequencies. The buffer will also add significant phase shift as frequency increases. The gain is less than unity before this becomes significant.

The full circuit diagram can be found in Figure 60 Appendix 3.8

[18] The operation of this circuit can also be thought of as bootstrapping R9.

4.3.2. 'Prototype servo 2'

The DC leak resistors have been removed. The integrating capacitor and filter capacitor have been increased to 10μF. These changes move the unity gain point from 200 Hz to 4Hz.

This prototype has two sets of stable DC conditions. One condition is correct. The other has the collector and emitter of Q1 at the same potential (transistor off). The condition reached is determined by the order that the power supplies are turned on.

A significant problem is the substantial loss of gain in these prototypes over the standard common base circuit. The mid-band gain is 263Ω where a gain of 456Ω is expected. This may be due to feed through of the network analyser signal to the floating rail. If an attenuated and inverted version of the input signal current flowed in R4 (Figure 27), the effect would be an attenuation of the input current. The two would partially cancel. A SPICE simulation[19] shows that an anti-phase signal of 250μV on the floating ground halves the gain. It is likely that the DC servo is the means for the signal to appear at the floating rail.

[19] In this simulation the DC loop was removed. A perfect voltage source with an AC and DC component was used in its place. One terminal connected to the floating rail, the other to circuit ground. The DC component reflects the expected DC conditions under normal operation on the floating rail. The AC component was increased in magnitude until the reduction in gain equalled that observed in testing. The AC source on the floating rail was in anti-phase with the source representing the network analyser.

5. Operational Amplifiers

The present system has a gain of around 2000Ω. It is desirable for a transistor front end TIA to have similar gain so one can replace the other in the same measurement setup.

5.1. Voltage amplifiers

The common base amplifier has output impedance approximately equal to R_L (Appendix 2.1). A buffer is necessary to drive the 50Ω termination of the next stage of the measurement system. Also the gain of the common base stage must be quadrupled. Low noise, high input impedance, high frequency op amps designed to drive capacitive 50Ω loads are available. The AD829 is a suitable device. A list of devices that were considered is in (Appendix 2.2).

The gain bandwidth product of 120MHz facilitates a quadrupling of gain in one stage. However two stages are preferable. A design is shown in (Appendix 2.3). It was not possible to manufacture it.

6. Test Circuits and Results

In this section the circuits that were manufactured and the results obtained are discussed. First the test setup used for characterising the circuits is described.

6.1. Test Setup

The test setup uses a network analyser designed to be connected to a circuit using three ports. The source and reference are connected to the input. The receiving channel is connected to the output. All HF connections are made with 50Ω coaxial cable. The cable and other system artefacts are removed by connecting the output probe to the input (and reference) then normalising. This setup is not suitable for HF testing. Artefacts generated by the lack of impedance matching at the input would hide the response of the system. After normalisation the impedance at the input is changed by the removal of the output probe. In high frequency test setups a different method using two probes is common. The source and receiving probe are connected together and the analyser is normalised. Using this method the impedances are always matched.

To circumvent the impedance matching problem a power splitter has been made. It is a three port resistive network. Looking into one port with the other ports terminated the resulting impedance 50Ω. If the two ports were in parallel the impedance would be half of the characteristic impedance. For any port looking into the terminated power splitter the impedance is ((50 + 16.6) // (50 + 16.6) + 16.6) = 49.9Ω. A diagram showing the terminations and grounding of the test setup is given in Appendix 3.1

6.2. Test Designs

The figures in this section and corresponding results can be found in Appendix 3.2 to 3.8

6.2.1. Design 1

The first stage is a series peaked common base transistor. In is AC coupled to an emitter follower. The emitter follower buffers the first stage, enabling a 50Ω termination to be driven. The purpose of this design was to ensure that the

method for common base amplifiers was grasped, secondly to obtain a constant amplification over the bandwidth of interest. Work on series peaked (compensated) loads was discontinued after this design.

This design underwent several modifications. Results were obtained after the 470µF capacitors were changed to 10µF chip types. The LF pole at the input was moved up in frequency accordingly. The input impedance of the second stage is approximately 5kΩ. There is a 10% gain loss due to the loading effect of this stage. The resistor chain (R2, R3 and R4) considerably influences the HF response of the common base stage. This was not recognised until much later. It is likely that the flat response in the region of interest is accidental. Given Appendix 1.3 (a result showing the unsuitability of 10kΩ for chain resistance) it is likely that the amplifier response is rising through the region of interest and peaking near to 25MHz. Also the ground plane closely surrounds the resistor chain. This increases the capacitance to ground, compounding the HF inaccuracy

6.2.2. Design 2

The common base stage is now resistively loaded. Its operating point has been changed. The circuit board layout is substantially different. All the components are closer together. The ground plane is removed around the resistor chain. There is approximately 5mm clearance. The resistor chain was probed between R2 and R3 in order to find its effect on frequency response. The result (Appendix 1.3) is a first order rise in signal amplitude starting at approximately 15 MHz. The estimation of the parasitic capacitance given in section 3.1.2 was produced from this result.

6.2.3. Design 3

In design 3, Q2 is replaced by a darlington pair and the biasing resistor values have been increased. This design was not constructed. An improvement in frequency response was obtained by removing the second and the resistor chain from design 2. A voltage then drove the common base stage. Design 3 was in preparation while these tests were being conducted. By the time design 3 was ready for manufacture it was defunct.

6.2.4. Design 4

The following designs aim to make the common base amplifier useable in the measurement application by removing the necessity for large capacitors on the input and output. Design 4 is uses pair of common base circuits one has the input grounded, the other amplifies the noise signal. A differential amplifier attenuates the DC. U1 must have high value gain determining resistors. If low, less noisy values were used, the differential amplifier would load the common base circuits. This is the first design to include a DC servo. In this design, R6 is sufficiently small that the current flowing to ground through R20 R21 R22 and R23 can be neglected. There are several problems with this circuit which would stop it performing as intended.

The shield of the network analyser source is connected to the floating rail. The 47kΩ resistors that set the gain of the buffer, U5, would be noisy. Use of a low value resistor would cause current to flow into the buffer instead of the transistor. This stage would be more suited to a non inverting structure which is used later. The capacitors C4, C5 and C6 are poorly positioned. To ensure that the large capacitance doesn't affect the stability of the U4 a series resistor should be included. The op amp used for the differential amplifier and the following stages (having a gain of 1.5) has a maximum supply voltage of +/- 12 Volts. 15 Volts was used in the design of the common base stage, necessitating two supplies. There will be a small offset around the DC loop due to the finite GBP of U4. Design 4 was not manufactured.

6.2.5. Design 5

This design was also not manufactured. The common base stage was redesigned again, with half the gain of design 4 to improve bandwidth. Considering the probes marked on the design (Appendix 3.6) most of the current meant to flow in R1 flows into the DC servo. The input resistance of the buffer is 100Ω. The two op amp DC servo of design 4 was changed to one op amp to lessen the likelihood of instability in the loop. This is the first design where the DC loop had integral action.

6.2.6. Design 6

Design 6 was used to investigate a method of correcting the rise in the HF response of the resistor chain. The rise in gain at HF due to the parallel parasitic capacitors can be corrected by the addition of a capacitance to ground. This is permissible because the APD will replace the resistor chain. The required capacitance to ground is approximately 2nF. More than 200pF will adversely affect the TIA HF response. The board was manufactured, however no data was recorded. A first order roll off started at 10 kHz! The circuit is simple enough that the solution should be obvious. Nothing that was attempted affected the result. It was abandoned.

6.2.7. Design 7

Design 7 is the first manufactured design with a DC coupling into, and out of, the common base stage. The DC servo part of this design is the subject of section 4.3. In brief a low frequency op amp (AD648, GBP = 1MHz) is used, first in a non inverting unity gain buffer circuit followed by an integrator with a DC leak network. The output of the integrator is connected to a capacitance to ground via a 5Ω resistor to avoid stability problems. The transistor stage is a common base circuit. This is followed by a DC coupled, non-inverting, unity gain buffer. The op amp is a Texas Instruments THS4011 high frequency *high noise* op amp (c.f. AD829).

6.2.8. Design 8

This design is a modification of Design 7[20]. The DC servo is modified to that of section 4.3.2. The changes, in brief, are: the removal of the leaking resistor across the integrating capacitor, the changing of the time constants in the DC servo loop to ensure stability. The disconnection of the network analyser ground from the floating rail and the addition of a 22µF capacitor to ground from the network analyser shield. The common base output buffer op amp was changed to an AD829 this offers equivalent bandwidth performance when used in low gain amplifiers. The noise performance of this op amp is improved over the THS4011.

[20] In the authors hand written notes and results it is referred to as Design 7 II

An interesting problem occurred in the DC servo of this design after the AD648 was inadvertently connected with its power pins reversed (see Figure 28). The supply limited the fault current to around 100mA. The fault caused a deep notch in the frequency response at 127 kHz[21]. A new test arrangement was made to find the problem. The op amp was disconnected from the surrounding circuitry. A signal generator and an oscilloscope revealed the nature of the problem. As the frequency is increased towards 127 kHz the gain reduced slowly until the waveform appeared absent. Further slight increases in frequency cause the signal to reappear in anti-phase. Within 1 kHz the signal was at its previous amplitude. It appeared to jump suddenly instead of a linear rise with frequency. When 127 kHz is approached from a higher frequency the gain reduction is slow (as it was when approaching from less than 127 kHz) passing through 127 kHz has the same effect. After this the gain appears to return instantly to around the expected value. The gain difference in the flat regions either side of the anomaly was approximately 2 dB. The op amp was replaced. The problem almost disappeared manifesting itself as a 2dB drop in gain of similar nature at the same frequency. The 100nF chip decoupling capacitors were changed to orange drop types. This cured the problem. One of the plots of this problem is located in Appendix 3.8

When a capacitor (C7 in Figure 61) was added from R11 to circuit ground the SPICE response at the floating rail changed from Figure 66 to Figure 67 (Appendix 3.8). SPICE does not model the network analysers' internal connections. Neither end of the voltage source that acts as the network analyser source is connected to DC ground (unless it is shown on the schematic). However inside the network analyser the shield of the source connection may be connected to ground. If so the capacitance that has been added is redundant. This is not consistent with what is observed in testing (Section 4.3). The addition of the capacitance appears not to affect the DC servo operation. A solution to this inconsistency has not been sought.

[21] The frequency of the notch was dependant on capacitances in the servo loop. These were changed more than once. 127 kHz is the first frequency where the notch was observed. Later the notch moved to 132 kHz and 144 kHz when C3 C2 and C5 in Figure 61 were increased in value between design 7 and design 8

Results and circuit diagrams for designs 1 to 8 are given in the Appendix beginning at Appendix 3.2

7. Conclusion and Further Work

7.1. Summery of work

A brief survey of the measurement system in use at Sheffield has been completed. A common base amplifier has been used with a circuit representation of an APD. A non peaking transimpedance front end, irrespective of APD capacitance, has been investigated. Methods of coupling the signals into and out of the front end have been tested. A noise analysis has been performed which can be modified or extended for use on new common base circuits. New noise sources can be added at the input or output of the common base amplifier without restarting the analysis, only extending it.

7.2. Objectives

The primary objective of this project is given in its title. A critical evaluation may conclude that since the primary objective has not been achieved, the project is unsuccessful.

The development of APD noise measurement systems at Sheffield has focused on front ends using op amps. Considerable time and ingenuity have been applied to develop the present measurement system. A transistor front end is not yet developed. Although no devices have been characterised two achievements are worthy of note.

The common base transistor stage acts sufficiently as a buffer between the APD capacitance and the next stage of the measurement system. The response is invariant (for practical purposes) with junction capacitances up to 200pF (Figure 64). The interaction between the device capacitance and op amp compensation capacitance has caused a peak in response of the measurement system [10] and [11].

The calculated noise performance (Section 3.3.3 and Appendix 1.6) of the most recent design presented here is similar to those published previously [50].

The results presented warrant further investigation of discrete transistor TIAs

7.3. Further work

The loss in gain, possibly due to feed through, in design 8 must be resolved. The use of a servo to DC couple the input may not be practical. If this is the case another method involving a bias tee which, regrettably, did not receive any attention after its suggestion may be investigated. If this should also prove impractical it may be possible to use two amplifiers. One amplifier will amplify the noise signal using a small value (non polarised polytetrafluroethene, polyester etc.) capacitor. The other would be used to amplify the low frequency chopper signal (using an electrolytic capacitor). If the phase shift introduced by the amplifiers can be kept (or made) equal to each other at 200 Hz and between 8MHz and 12 MHz, this method may provide acceptable results.

Considering the output of the common base stage, if the required LF response can not be obtained using buffered capacitive coupling, the attenuation of the DC component using a differential amplifier is a logical way forward.

This project (apart from some early design work) has only used one transistor (BFS17W). No reason was found to change it. At the operating point eventually selected f_T is 900MHz (from SPICE). If this transistor should prove inadequate another may be substituted[22]. All transistors of sufficient f_T will provide the same bandwidth (using the same operating conditions). The limiting factor on HF performance is the pole formed between the APD capacitance and the resistance looking into the emitter of the transistor (re'). A logical progression may be to look for a device that has higher β and lower noise. High β is desirable for two reasons. Firstly for a given r_{be}, transconductance is increased so re' is lowered. Secondly the output noise is divided by α to obtain the input noise. Increasing β makes α closer to one which is the optimum condition. If a device fitting these criteria is found then it should be possible to obtain the same noise performance as calculated earlier while having a higher quiescent collector current. This increases

[22] It is not generally considered good design practice to rely on the device characteristics to make a circuit *function*

transconductance (reduces re') and increases HF response. An alternative view would be that the HF response will be the same as present for a larger device capacitance.

Leach [54] describes a noise optimisation for a number of parallel transistors. Where thermal noise at the input is not dominant, increasing the number of parallel transistors increases SNR without limit. In the case where the thermal noise is dominant there is a finite optimum. If the SNR can be improved by this method gain may be decreased (by decreasing R_L). This is desirable because it extends bandwidth. Bandwidth may be also be extended by increasing IC while maintaining the present NSNR. This is desirable as it reduces re' permitting larger APD capacitances. (It also extends bandwidth for a given APD capacitance).

8. References

[1] Streetman B G & Banerjee S, “Solid State Electronic Devices”, Fifth Edition, Prentice Hall, 2000, Pages 384 - 385

[2] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 1

[3] Jarron P et.al, ”A transimpedance amplifier using a novel current mode feedback loop”, Nuclear Instruments and Methods in Physics Research A 377 (1996) 435 439

[4] Knorr J and Zimmermann H, ”A Transmission-Line Approach for Modelling Feedback Resistors in Integrated Transimpedance Amplifiers”, IEEE Transactions On Circuits And Systems-I: Fundamental Theory And Applications, Vol. 50, No. 9, September 2003

[5] Chien F and Chan Y, ”Bandwidth Enhancement of Transimpedance Amplifier by a Capacitive-Peaking Design”, IEEE Journal Of Solid-State Circuits, Vol. 34, No. 8, August 1999

[6] S. Moustakas et al. ”Comparison of BJT and MESFET front ends in broadband optical transimpedance preamplifiers”, Optical and Quantum Electronics 14 (1982) 57-60

[7] K F Li , “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 4 Fig 1.2

[8] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Pages 12 & 16

[9] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 51 Fig 4.3

[10] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 59

[11] Lau K S, “Multiple Transit Region Gunn Diode”, A PhD Thesis Submitted to the University of Sheffield, October 2006, Page 77 -81

[12] Lau K S et al, “Excess Noise Measurement in Avalanche Photodiodes Using A Transimpedance Amplifier Front End”, Institute of Physics Publishing, Meas. Sci. Technol. 17, 2006, 1941-1946

[13] Leach W M, “Fundamentals of Low-Noise Analog Circuit Design”, Proc. IEEE, Vol. 82, No. 10 Oct 1994 Page 1517

[14] Lau K S, “Multiple Transit Region Gunn Diode”, A PhD Thesis Submitted to the University of Sheffield, October 2006, Page 17

[15] Gray et al, “Analysis and Design of Analog Integrated Circuits”, Wiley, 2001, Page 755

[16] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 17 -18

[17] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 21 - 27

[18] Leach W M, “Fundamentals of Low-Noise Analog Circuit Design”, Proc. IEEE, Vol. 82, No. 10 Oct 1994 Page 1514

[19] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 70 - 74

[20] Lau K S, “Multiple Transit Region Gunn Diode”, A PhD Thesis Submitted to the University of Sheffield, October 2006, Page 76

[21] van der Ziel A, “Noise in Solid State Devices and Circuits”, John Wiley & Sons, 1986, pages 145 - 162

[22] Ng J S, “EEE6009: Photoluminescence Measurements”, The University of Sheffield. Pages 6 - 7

[23] Lau K S, “Multiple Transit Region Gunn Diode”, A PhD Thesis Submitted to the University of Sheffield, October 2006, Page 77, (Eq^{n} 6.1)

[24] Yong-Hun Oh and Sang-Gug Lee “An Inductance Enhancement Technique and Its Application to a Shunt-Peaked 2.5 Gb/s Transimpedance Amplifier Design”, IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 51, No. 11, November 2004

[25] Feng-T and Chan Y, “Bandwidth Enhancement of Transimpedance Amplifier by a Capacitive-Peaking Design“, IEEE Journal of Solid- State Circuits, Vol. 34, No. 8, August 1999

[26] Terman F E, “Electronic and Radio Engineering”, McGraw Hill, Fourth Edition, 1955, Pages 400 - 448.

[27] Williams E, “Thermionic Valve Circuits”, Isaac Pittman & Sons, Fourth Ed. 1961, Pages 84 -100

[28] Langford-Smith F, “Radiotron Designers Handbook”, RCA, Fourth Ed. 1952, Pages 912 -945 & 1020 - 1055

[29] Krugman L, “Fundamentals of Transistors”, John F Rider, 1954, Pages 122 - 126

[30]Simpson & Richards, “Junction Transistors”, Oxford, 1962, Pages 328 - 357

[31] Barden W S, “Amplifying Device”, US Patent No. 2085407, Applied 31 Dec. 1934, Granted 29 June 1937

[32] Terman F E, “Electronic and Radio Engineering”, McGraw Hill, Fourth Edition, 1955, Page 416.

[33] Analui B and Hajimiri A, “Bandwidth Enhancement for Transimpedance Amplifiers”, IEEW Journal of Solid-State Circuits, Vol. 39, No 8, August 2004 Pages 1263 – 1270

[34] Motchenbacher C D & Connelly J A, “Low Noise Electronic System Design”, John Wiley & Sons, 1993

[35] Motchenbacher C D & Connelly J A, “Low Noise Electronic System Design”, John Wiley & Sons, 1993, Page 39 - 41

[36] NXP (formally Phillips Semiconductor), “BFS17W Datasheet”, See http://www.nxp.com

[37] Motchenbacher C D & Connelly J A, “Low Noise Electronic System Design”, John Wiley & Sons, 1993, Page 113

[38] Motchenbacher C D & Connelly J A, “Low Noise Electronic System Design”, John Wiley & Sons, 1993 Page 112 – 118

[39] Cowles L G, “Analysis and Design of Transistor Circuits”, Van Nostrand, 1966 pgs 31 - 38

[40] Grey et al. “Analysis and Design of Analog Integrated Circuits”, John Wiley & Sons, Fourth Edition, Page 183

[41] Gray et al. “Analysis and Design of Analog Integrated Circuits”, Wiley, 2001, Page 34 - 37

[42] Streetman B G & Banerjee S, “Solid State Electronic Devices”, Fifth Edition, Prentice Hall, 2000, Pages 363 - 365

[43] NXP (formally Phillips Semiconductor), “BFS17W Datasheet”, See http://www.nxp.com

[44] Bibby M, “Non Op-amp Based Transimpedance Amplifier” a third year project report submitted to the University of Sheffield, 2007

[45] Williams E, “Thermionic Valve Circuits” Pitman, 1961, page 98

[46] Terman F E, “Electronic and Radio Engineering”, McGraw Hill, Fourth Edition, 1955, page 428

[47] SIMetrix is a simulator based on Berkley SPICE 3F5. It is produced by Catena Software. A free limited node version is available from http://www.catena.uk.com/

[48] Grey et al. “Analysis and Design of Analog Integrated Circuits”, John Wiley & Sons, Fourth Edition, Page 783

[49] Leach W M, “Fundamentals of Low-Noise Analog Circuit Design”, Proc. IEEE, Vol. 82, No. 10 Oct 1994 Page 1524

[50] K F Li, “Avalanche Noise in Submicron GaAs and InP Structures”, A PhD Thesis Submitted to the University of Sheffield, March 1999, Page 58

[51] Yageo Datasheet “Chip Resistor Surface Mount Introduction” www.yageo.com

[52] Dimler S, Private Correspondence, March 2007

[53] Horowitz P & Hill W, “The Art of Electronics”, Cambridge, 1989, page 223

[54] Leach W M, “Noise Relations for Parallel Connected Transistors”, J. Audio. Eng. Soc. No. 47 Vol. 3 March 1999

1. Appendix for Section 3

1.1. Analysis of Common Base Connection for re'

Resistance looking into the emitter of a common base amplifier

A test current is injected into the emitter in order to find the impedance looking into the emitter.

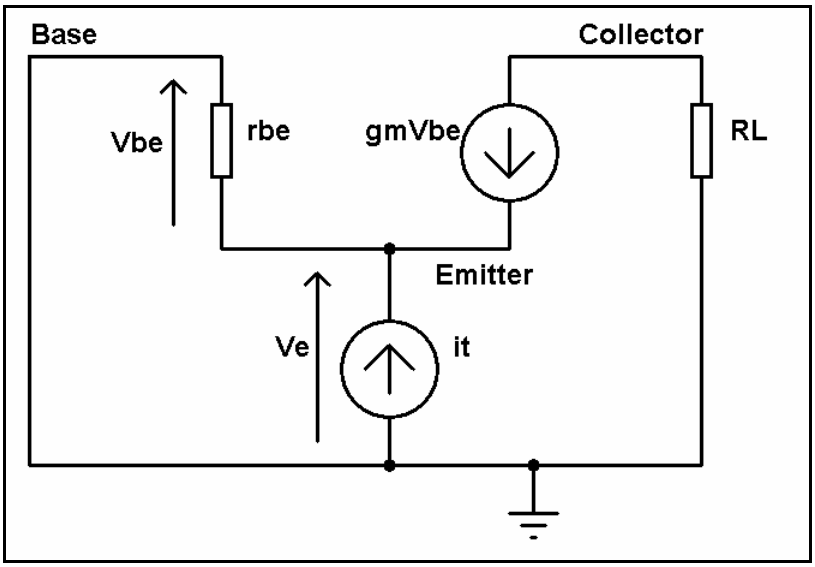


Figure 29: Simplified Low Frequency Small Signal Model of Common Base Circuit

At the emitter node:

$$\frac{V_{be}}{r_{be}} + i_T + gmV_{be} = 0$$

$$V_e = -V_{be}$$

$$V_{be}\left(\frac{1}{r_{be}} + gm\right) + i_T = 0$$

$$-V_e\left(\frac{1}{r_{be}} + gm\right) = -i_T$$

$$r_e' = \frac{V_e}{i_T}$$

$$r_e' = \frac{1}{1/r_{be} + gm} \approx \frac{1}{gm}$$

1.2. Transimpedance Gain of Common Base Topology

The resistor modelling the early voltage has been ignored as has the collector – emitter capacitance. The input signal is small enough that the slight slope of the collector characteristics is unlikely to have significant effect. In this connection the collector – emitter capacitance represents a feedback method from output to input. The value of c_{ce} is in the order of 0.5pF for a BFS17W. At 20MHz this represents an impedance of approximately 16kΩ and can be ignored.

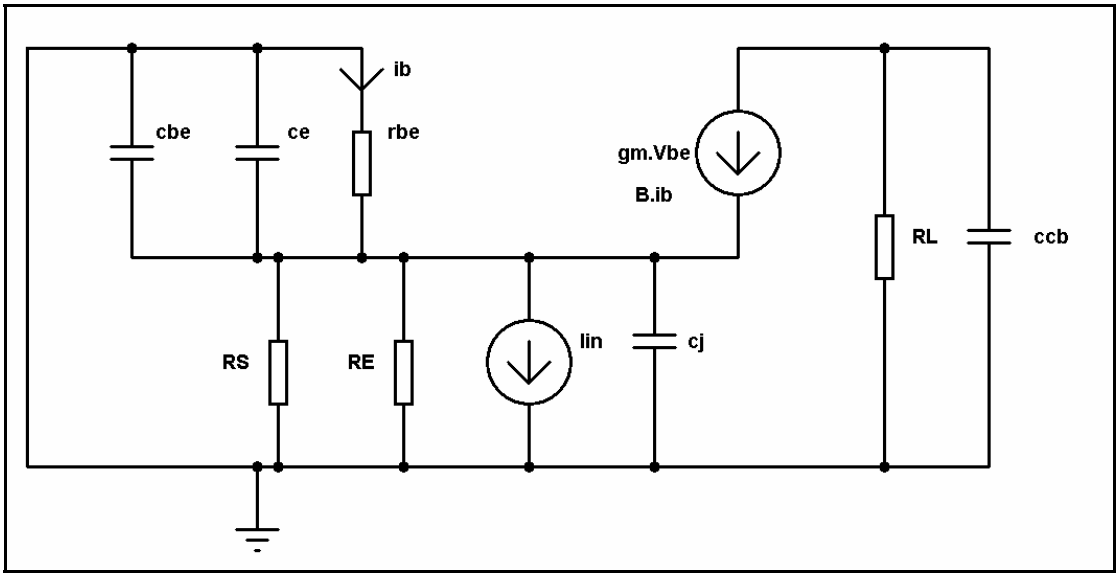


Figure 30: Small Signal Model of CB Amplifier

For the input network:

$$z_i = \frac{R_E \,//\, r_{be}}{1 + s\left(R_E \,//\, r_{be}\right)\left(c_j + c_{be} + c_e\right)}$$

Equation 1

For the output network

$$z_L = \frac{R_L}{1 + s\left(c_{cb} R_L\right)}$$

Equation 2

From the network simplification:

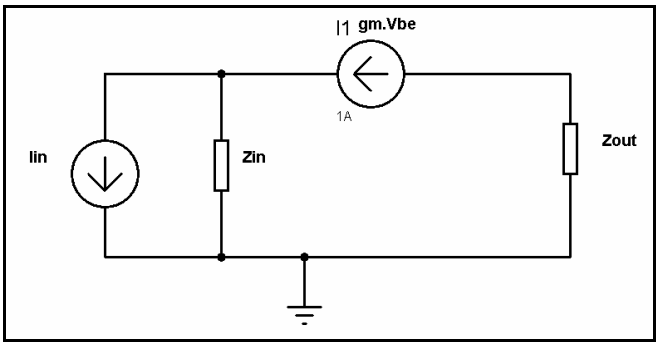


Figure 31: Simplified CB Amplifier

$$i_{ph} = gm \cdot v_{be} + \frac{v_{be}}{z_i}$$

Equation 3

$$\frac{V_o}{z_L} = gm \cdot v_{be}$$

Equation 4

From Equation 3 & Equation 4:

$$i_{ph} z_i = v_{be} + gm \cdot v_{be} z_i$$

$$i_{ph} z_i = v_{be} \left(1 + gm \cdot z_i\right)$$

$$i_{ph} z_i = \frac{V_o}{gm \cdot z_{out}} \left(1 + gm \cdot z_i\right)$$

$$\frac{V_o}{i_{ph}} = \frac{gm \cdot z_{out} \cdot z_i}{1 + gm \cdot z_i}$$

Equation 5

Substituting Equation 1 & Equation 2 into Equation 5:

$$\frac{V_o}{i_{ph}} = \frac{gm\left(\frac{R_L}{1 + s\left(c_{cb} R_L\right)}\right)\left(\frac{R_E \,//\, r_{be}}{1 + s\left(R_E \,//\, r_{be}\right)\left(c_j + c_{be} + c_e\right)}\right)}{1 + gm\left(\frac{R_E \,//\, r_{be}}{1 + s\left(R_E \,//\, r_{be}\right)\left(c_j + c_{be} + c_e\right)}\right)}$$

Equation 6

1.3. Parasitic Capacitance for a 1206 Resistor

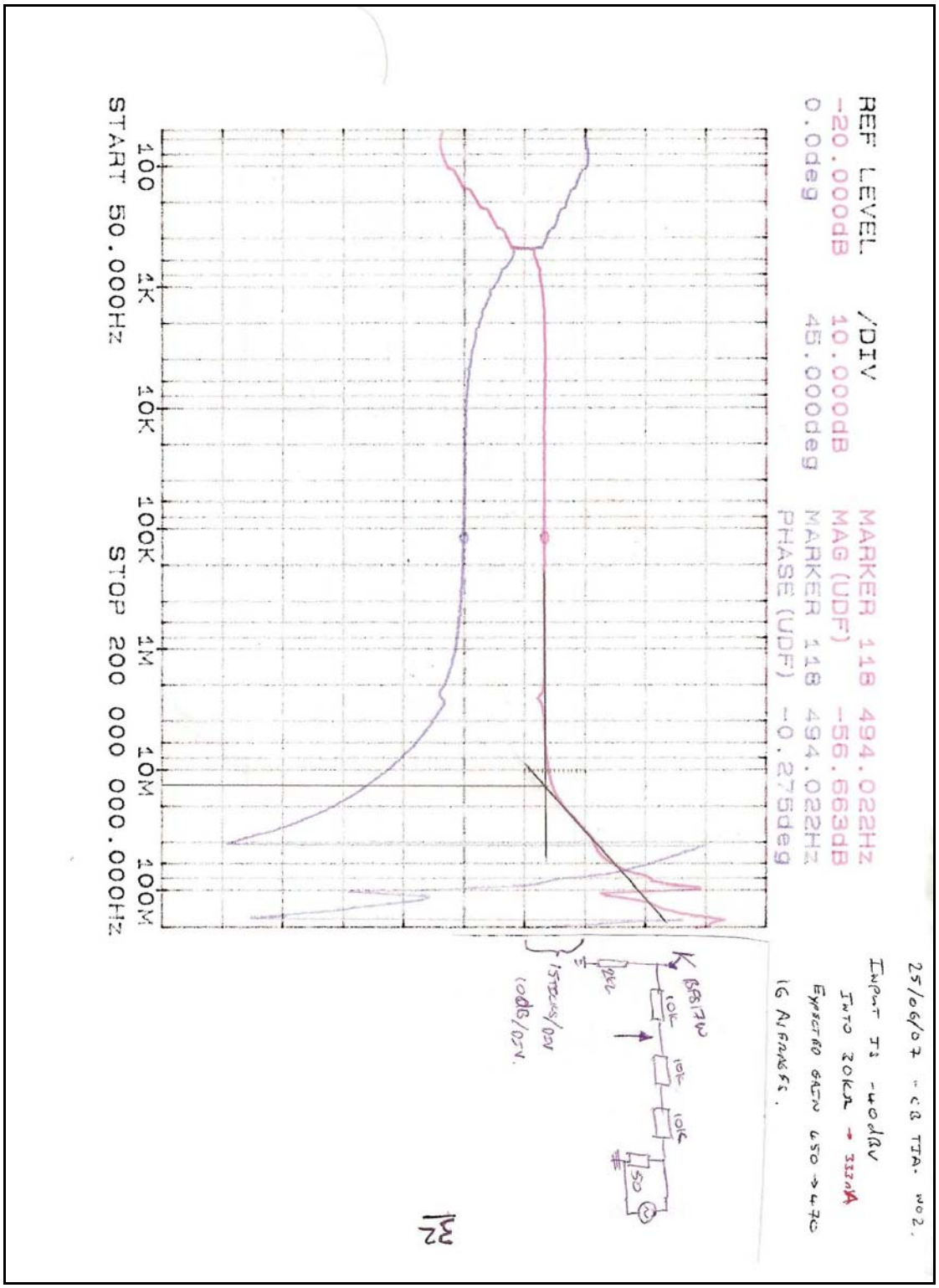


Figure 32: Plot from between second and third resistors in chain.

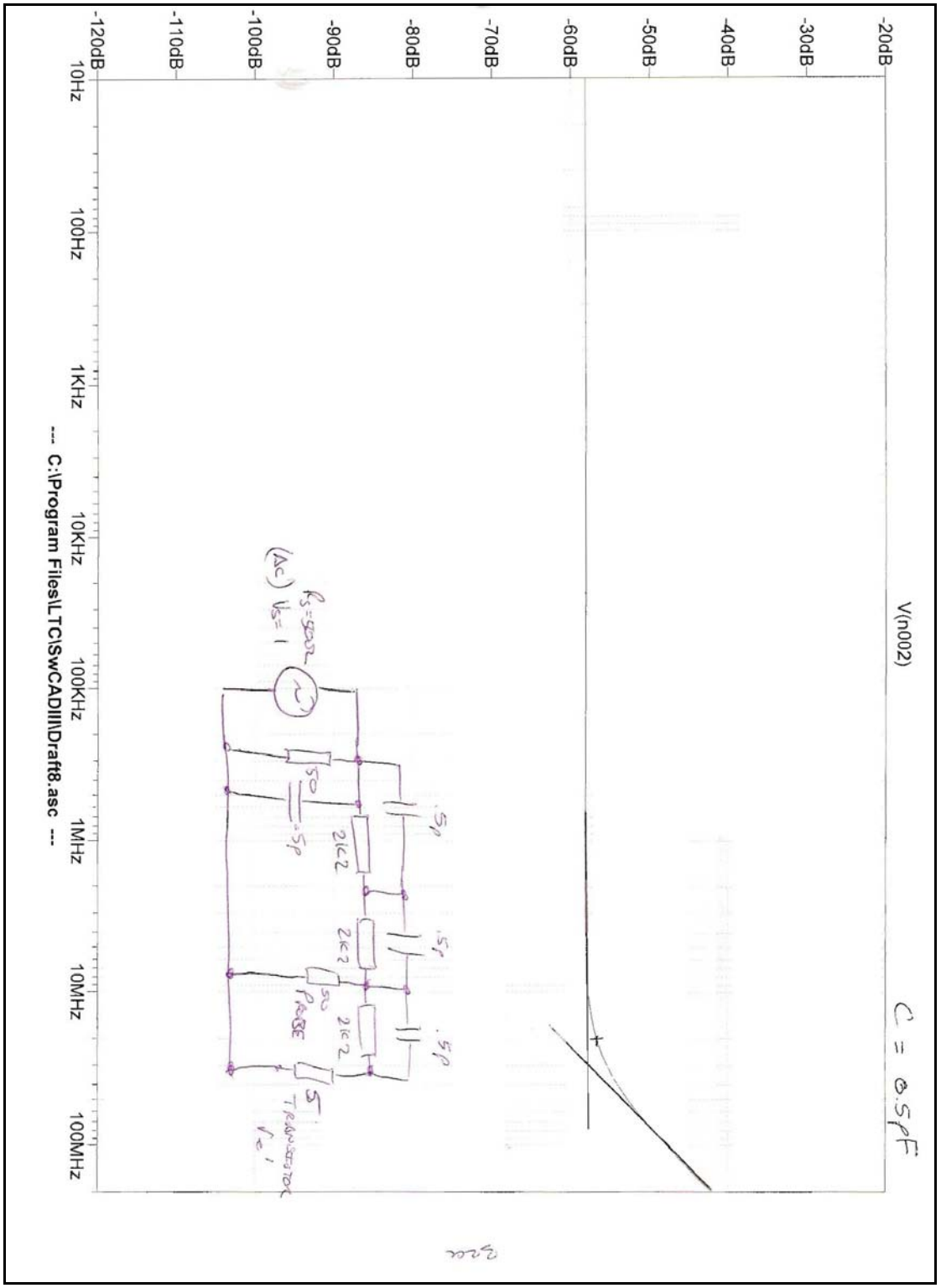


Figure 33: Spice simulation of resistor chain with parasitics and re' for Cp = 0.5pF

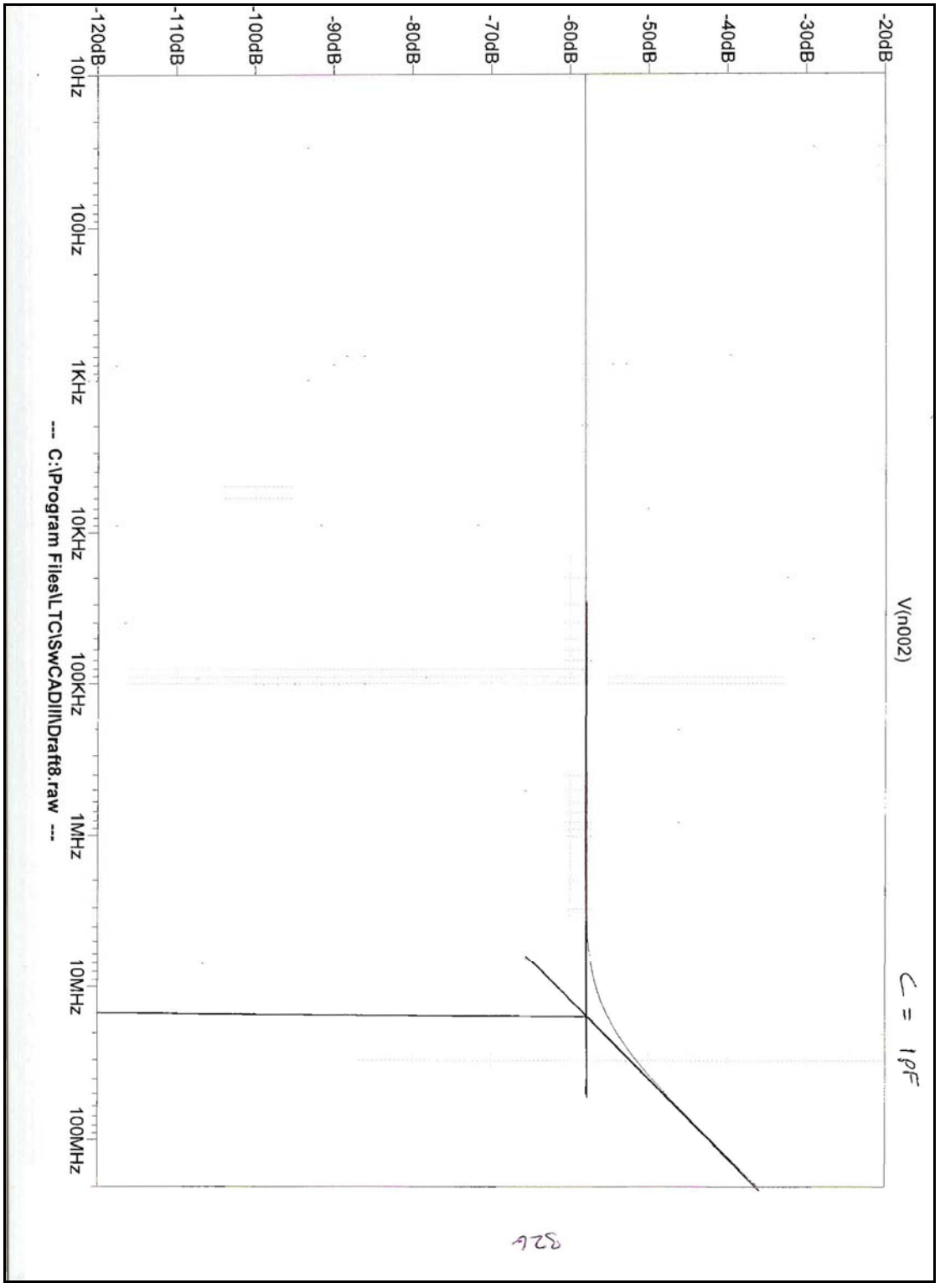


Figure 34: Spice simulation of resistor chain with parasitics and re' for Cp = 1pF

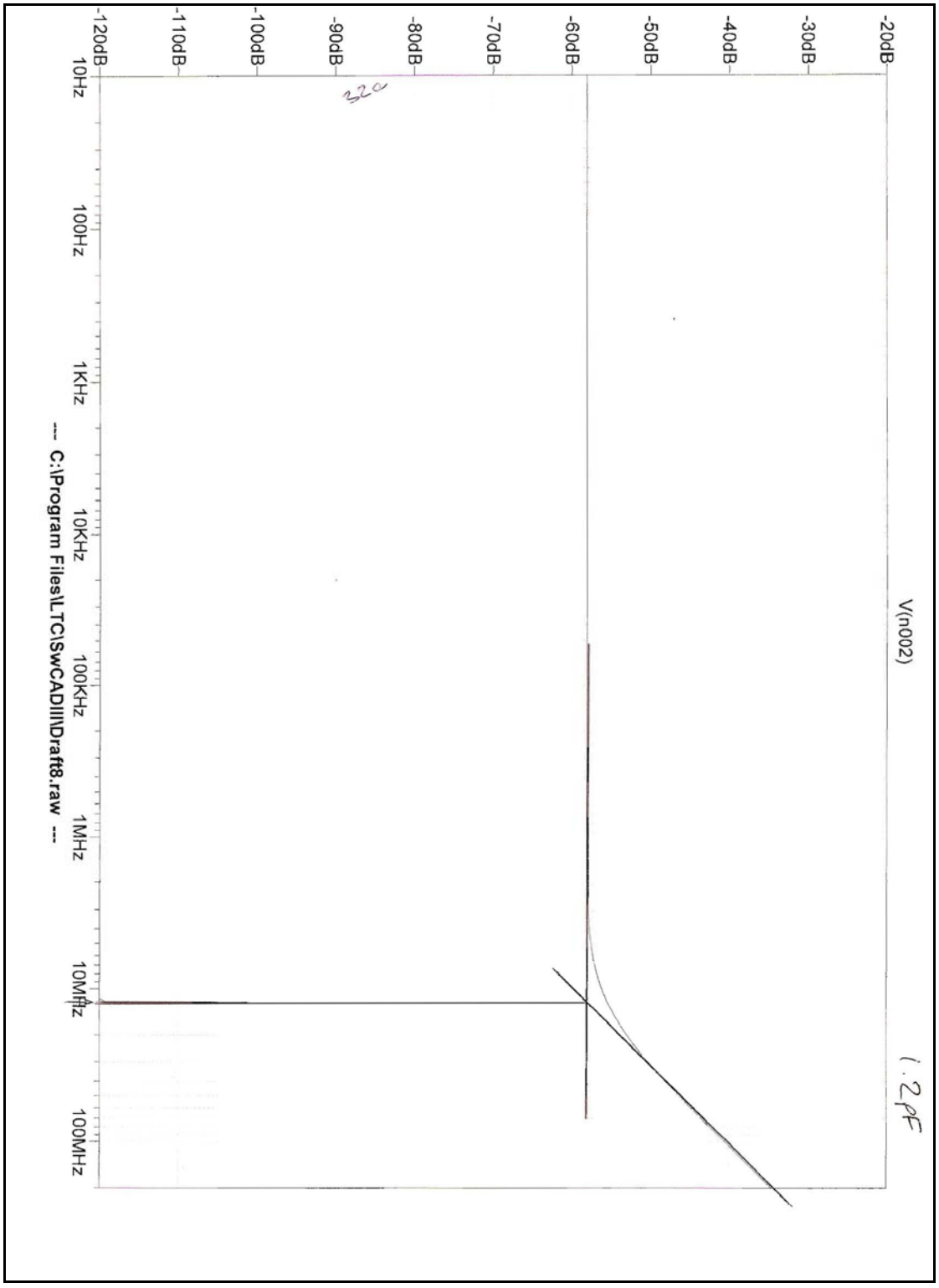


Figure 35: Spice simulation of resistor chain with parasitics and re' for Cp = 1.2pF

1.4. Graph Showing Gain - Bandwidth Relationship

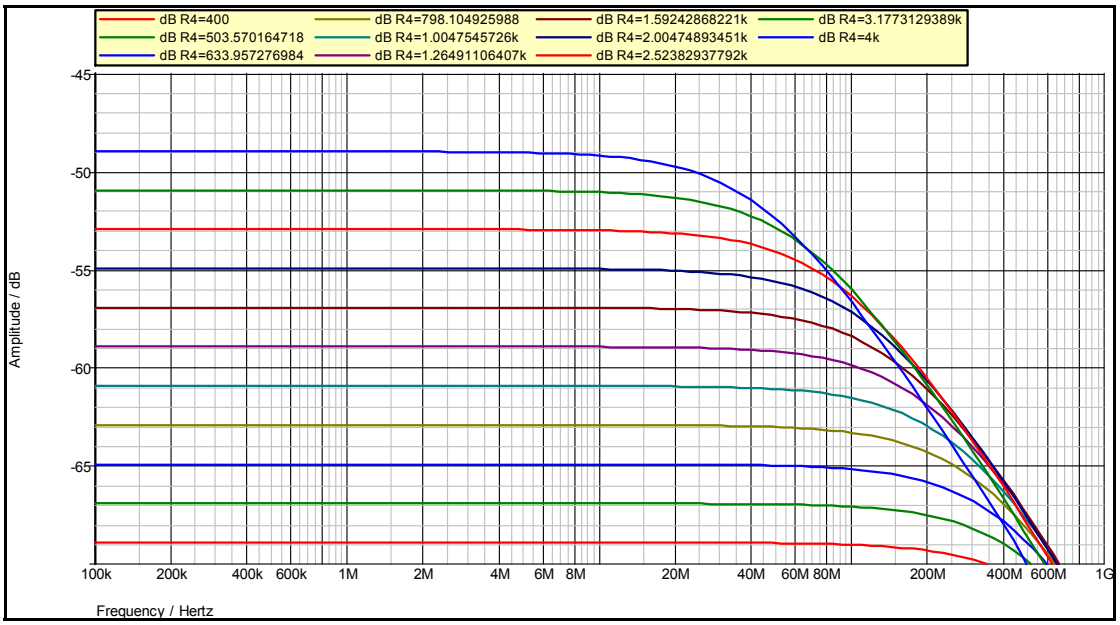


Figure 36: SPICE graph showing gain/bandwidth trade off

1.5. Noise Simulation Circuit

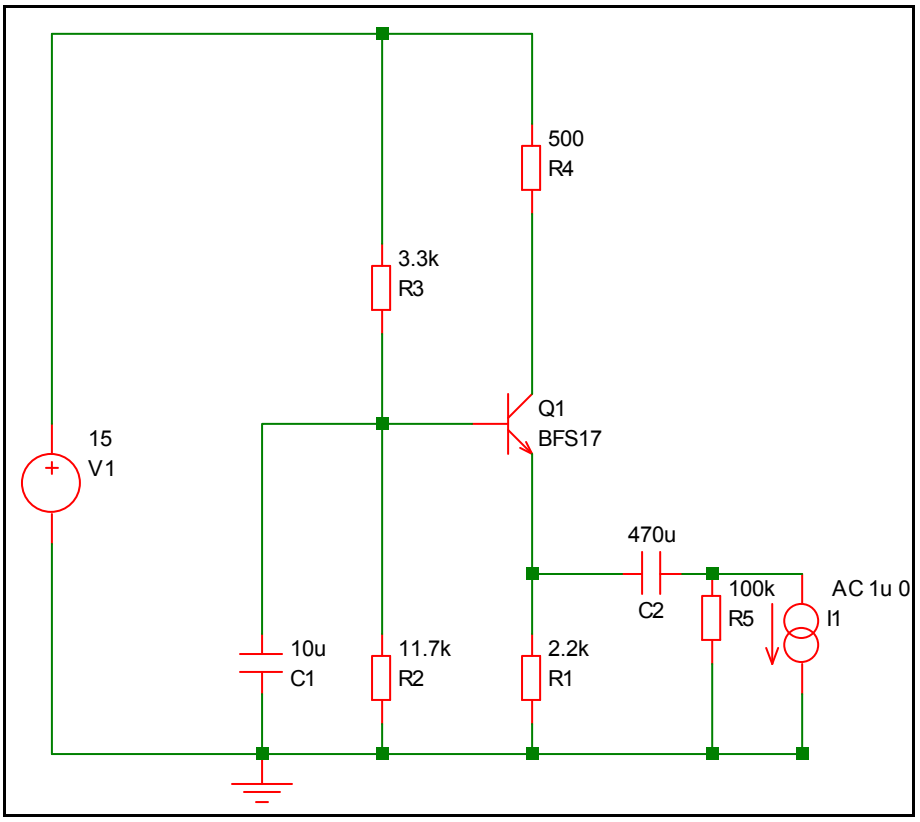


Figure 37: Noise Simulation Circuit

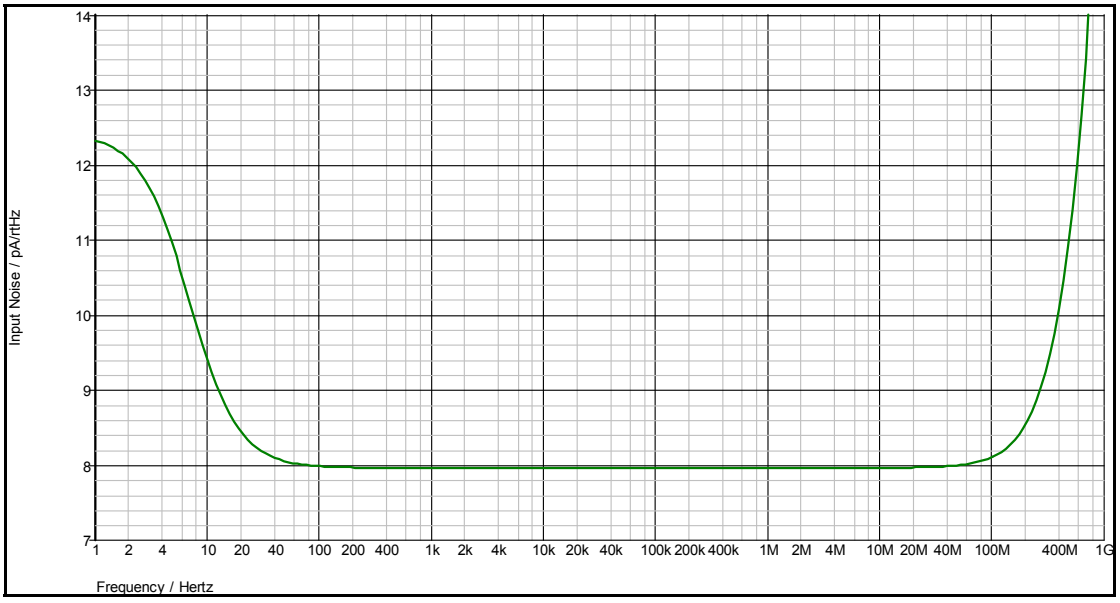


Figure 38: SPICE graph of input noise. The increased noise in the LF region is flicker noise. The HF region is due to an increase in collector shot noise [37].

1.6. Noise Analysis

The noise analysis begins with the combination of all the noise sources of interest in the transistor. This is combined with the noise of the load resistor. The combination of the load and transistor noise is referred to the emitter. This is done by dividing by the current gain of the transistor. The noise of the emitter resistor could be combined after the output noise is divided by the current gain if desired. This has little effect on the overall result.

Note that the results given here must be modified to be used in the noise analysis. The values of the noise voltages (and currents) are squared terms (e.g. $Ez_b{}^2 = 4 \cdot k \cdot T \cdot z_b$) and so the solutions below must be modified accordingly as in section 2.4.3.

For example from the analysis that follows:

$$I_o = \frac{I_{nb}\beta(R_s - z_b)}{r_{be} + z_b - R_s(1+\beta)}$$

Equation 7

Must become

$$I_o = \frac{I_{nb}^2 \beta (R_s - z_b)}{r_{be} + z_b - R_s(1+\beta)}$$

Equation 8

In order to be used in the noise analysis in the main body of this report. Mathematically, the two are identical. The change is purely in notation. The analysis was done with the symbol I_{nb} representing the base – emitter shot noise *squared.* Later in the (main body) analysis it is necessary to denote explicitly the squaring of the term.

The transistor showing all noise sources on the same diagram is given below. When the analysis was first attempted the result was found in the form of the input noise voltage per root Hz. Later, when the noise *current*[23] was required the *later* part of the analysis was modified to have i_{ph} instead of V_s. This is permissible *without* changing the value of R_s[24] as V_s = 0.1V develops 1μA (the photocurrent) in R_s = 100KΩ and the output noise current is found accordingly (from the voltage diagram). This current is referred to the input on the second diagram. Because the noise due to all the sources is found as a current at the output, a new diagram can be drawn consisting of a noiseless transistor and an input current (i_{ph}) and an input noise current (I_{ni}^2) The voltage source that would previously have got in the way (E_s^2) is not necessary in the new diagram (its effect is included in the total output noise current). The input noise current is found by dividing the output noise current by the current gain (α) instead of the transconductance gain (to get input noise voltage).

[23] The input noise current is required because the signal of interest is a current and the signal to noise ratio (at the input) is the objective of the analysis

[24] If a source transformation were performed in the usual way then R_s would have to be changed (changing its noise voltage (or current)). But in this case there is no source transformation.

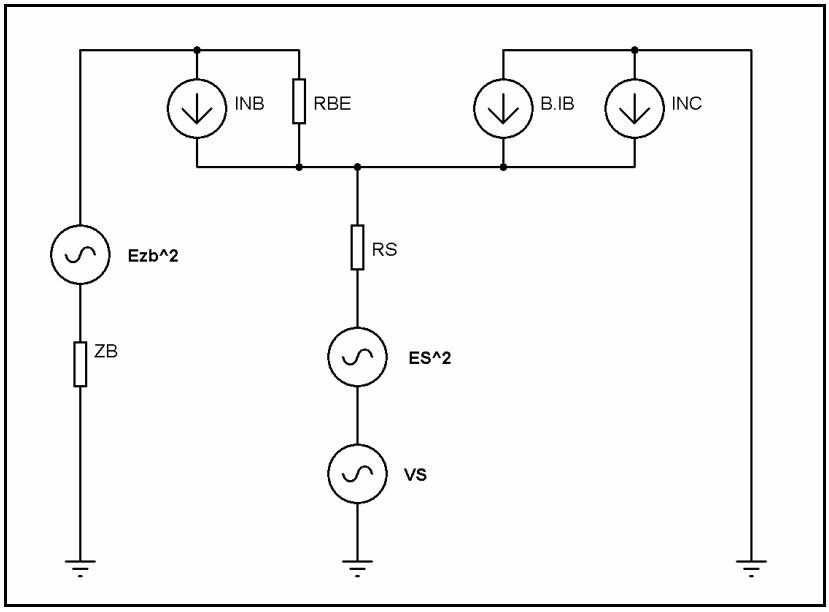


Figure 39: Transistor SSM with Noise Sources (Voltage Input Version)

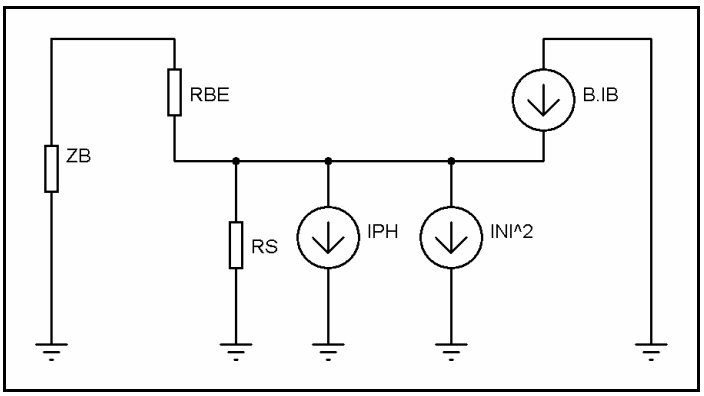


Figure 40: Transistor SSM with Referred Input Noise Current and Photocurrent Sources (Current Input Version)

1.6.1. Transfer Function (I_o/V_s) & Output Noise Current due to Thermal Noise of Source Resistance

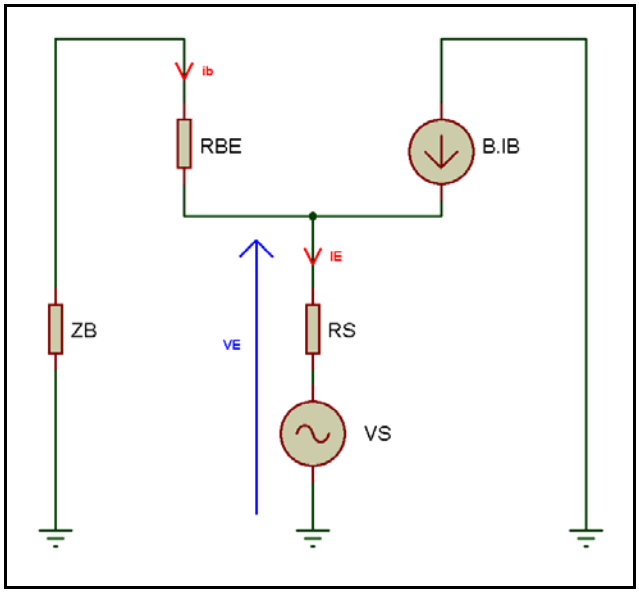


Figure 41: Transconductance gain

$$V_E = I_E R_s + V_s$$
$$V_E = (i_b + \beta \cdot i_b) R_s + V_s$$
$$v_{be} + v_{zb} = V_E$$
$$i_b (r_{be} + z_b) = (i_b + \beta \cdot i_b) R_s + V_s$$
$$i_b (r_{be} + z_b - R_s - \beta \cdot R_s) = V_s$$
$$i_b = \frac{I_o}{\beta}$$
$$\frac{I_o}{V_s} = \frac{\beta}{r_{be} + z_b - R_s(1+\beta)}$$

1.6.2. Output Noise Current Due to i_{nb} (Base Emitter Shot Noise)

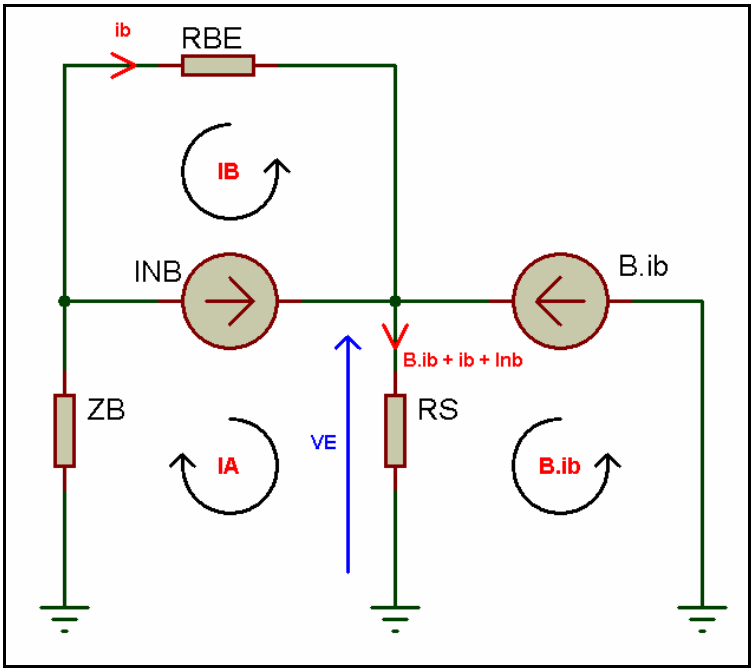


Figure 42: Model for Base - Emitter Shot Noise

$$I_A + I_B = I_{nb}$$
$$I_B = -i_b$$
$$V_E + v_{zb} = I_A(r_s + z_b) + \beta \cdot i_b \cdot R_s$$
$$v_{be} = I_B r_{be} = -i_b r_{be}$$
$$I_A - i_b = I_{nb}$$
$$V_E = (I_{nb} + i_b)(R_s + z_b) - (I_{nb} + i_b)z_b + \beta \cdot i_b \cdot R_s$$

$$V_E = I_{nb}R_s + i_b R_s + \beta \cdot i_b \cdot R_s$$

Equation 9

$$V_E = v_{be} + v_{zb}$$
$$V_E = i_b r_{be} + I_A z_b$$

$$V_E = i_b r_{be} + I_{nb} z_b + i_b z_b$$

Equation 10

Substituting Equation 9 into Equation 10

$$i_b r_{be} + I_{nb} z_b + i_b z_b = I_{nb} R_s + i_b R_s + \beta \cdot i_b R_s$$

$$i_b \left(r_{be} + z_b - R_s - \beta \cdot R_s\right) = I_{nb}\left(R_s - z_b\right)$$

$$i_b = \frac{I_o}{\beta}$$

$$\frac{I_o}{\beta}\left(r_{be} + z_b - R_s - \beta \cdot R_s\right) = I_{nb}\left(R_s - z_b\right)$$

$$I_o = \frac{I_{nb}\beta\left(R_s - z_b\right)}{r_{be} + z_b - R_s\left(1+\beta\right)}$$

1.6.3. Output noise current due to base spreading resistance z_b

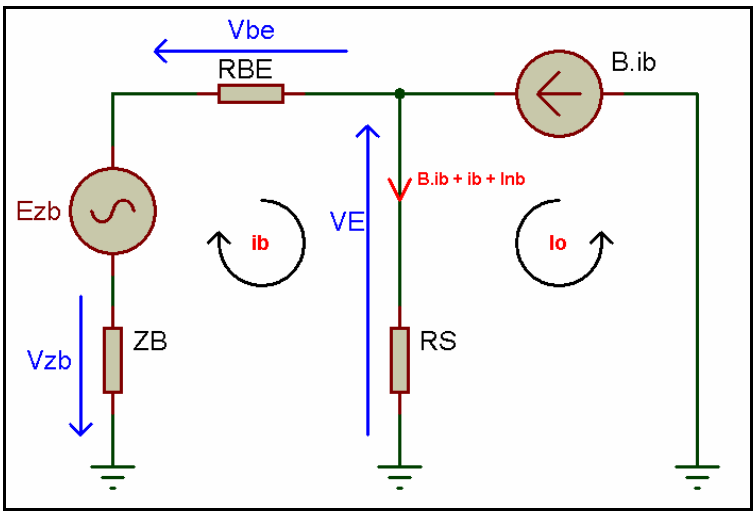


Figure 43: Model for Base Spreading Resistance z_b Thermal Noise

$$I_B\left(r_{be} + R_s + z_b\right) - E_{zb} + I_o R_s = 0$$

$$\frac{I_o}{\beta}\left(r_{be} + R_s + z_b\right) + I_o R_s = Ez_b$$

$$I_o\left(r_{be} + R_s + z_b + \beta \cdot R_s\right) = \beta \cdot Ez_b$$

$$I_o = \frac{\beta \cdot E_{zb}}{r_{be} + z_b + R_s\left(1+\beta\right)}$$

1.6.4. Output Noise Current due to Collector Base Shot Noise

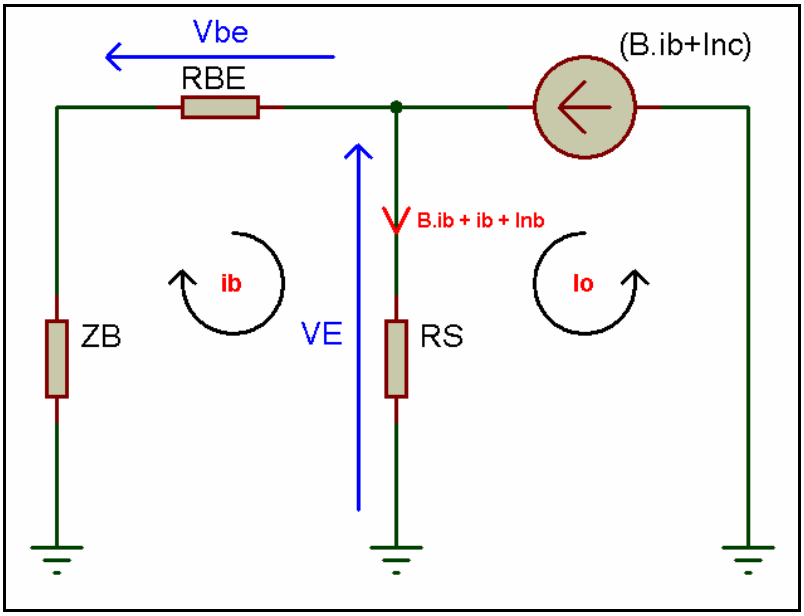


Figure 44: Collector Shot Noise Model

$$I_o = \beta \cdot ib + I_{nc}$$
$$i_b\left(R_s + z_b + r_{be}\right) + I_o R_s = 0$$
$$i_b\left(R_s + z_b + r_{be}\right) + \left(\beta i_b + I_{nc}\right)R_s = 0$$
$$i_b = \frac{I_o - I_{nc}}{\beta}$$
$$\frac{I_o - I_{nc}}{\beta}\left(R_s + z_b + r_{be}\right) + R_s\beta\left(\frac{I_o - I_{nc}}{\beta}\right) + I_{nc}R_s = 0$$
$$\frac{I_o R_s - I_{nc}R_s}{\beta} + \frac{I_o z_b - I_{nc}z_b}{\beta} + \frac{I_o r_{be} - I_{nc}r_{be}}{\beta} + R_s\left(I_o - I_{nc}\right) + I_{nc}R_s = 0$$
$$I_o\left(R_s + z_b + r_{be}\right) + \beta I_o R_s + I_{nc}\left(-R_s - z_b - r_{be} - R_s\beta + R_s\beta\right) = 0$$
$$I_o\left(R_s + z_b + r_{be} + \beta R_s\right) = -I_{nc}\left(-R_s - z_b - r_{be}\right)$$
$$I_o = \frac{I_{nc}\left(R_s + z_b + r_{be}\right)}{R_s + z_b + r_{be} + \beta R_s}$$

1.6.5. Operating Conditions for Noise Analysis

Constants:

$$k = 1.38 \times 10^{-23}$$
$$q = 1.6 \times 10^{-19}$$
$$T = 300.15$$

Transistor Parameters:

$R_s = 100000$

$r_{be} = 227.55$

$z_b = 10$

$E_s^{\,2} = 4 \cdot k \cdot T \cdot R_s$

$\beta = 41.4$

$I_{nb}^{\,2} = 2 \cdot q \cdot I_b$

$Ez_b^{\,2} = 4 \cdot k \cdot T \cdot z_b$

$I_{nc}^{\,2} = 2 \cdot q \cdot I_c$

The value of β is obtained from the manufactures curves as 45 for I_c = 5mA. From SPICE the operating point above leads to the value of β used.

DC Parameters:

$I_c = 4.71009 \times 10^{-3}$

$I_b = 1.138 \times 10^{-4}$

$vs = 0.1$

Circuit Parameters:

$R_L = 500$

2. Appendix for Section 5

2.1. Output impedance of a Common Base Amplifier

A test voltage is applied to the output and the current that flows is found. The impedance is found from these by ohms law.

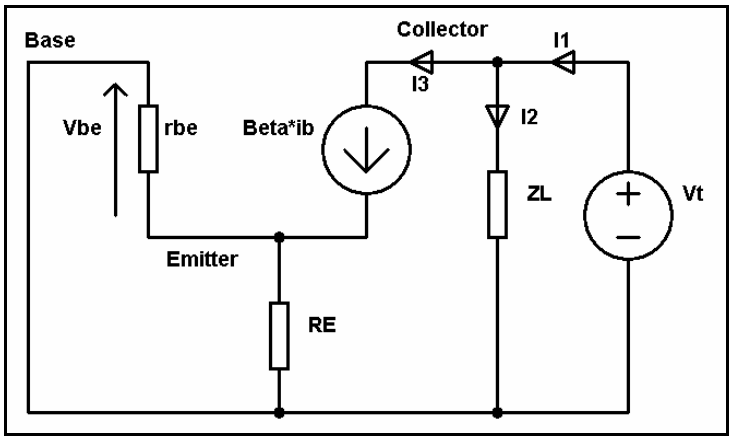


Figure 45: Simplified Common Base Signal Model

Figure 45 reduces to:

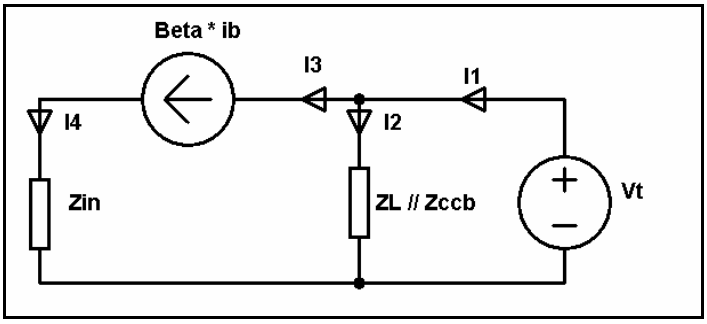


Figure 46: Signal Model with Components Lumped

At the collector node:

$$z_{out} = \frac{V_T}{I_1}$$

$$I_1 = I_2 + I_3$$

$$I_1 = \frac{V_T}{Z_L // Z_{ccb}} + \beta \times i_b$$

$$I_4 = i_b = I_3 = \beta \times i_b$$

$$i_b = \beta \times i_b$$

$$\therefore i_b = 0$$

And the equation for I_1 reduces to:

$$I_1 = \frac{V_T}{Z_L // Z_{ccb}}$$

$$\frac{V_T}{I_1} = Z_L // Z_{ccb}$$

Z_L // Z_{ccb} is:

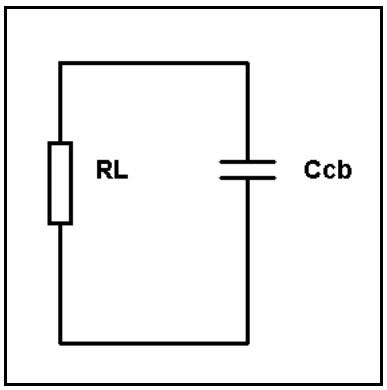


Figure 47: Output Network of Common Base Stage

$$Z_{out} = \frac{R_L}{1 + s \cdot C_{cb} \cdot R_L}$$

For the frequency range of interest the magnitude of the output resistance is approximately equal to R_L.

2.2. List of Operational Amplifiers Considered

LM7121

THS4001

THS4601

THS4082

THS3061

THS4601

LMH6640

OPA37GP

LM101

THS3120

CLC430

THS3201

THS4221

THS3201

THS3202

ADEL2020

LT1363

THS4222

THS4082

LM7121

THS3212

LM7171

OPA637

THS4081

THS4211

THS4275

2.3. Possible Design with Additional Gain Using Op Amps

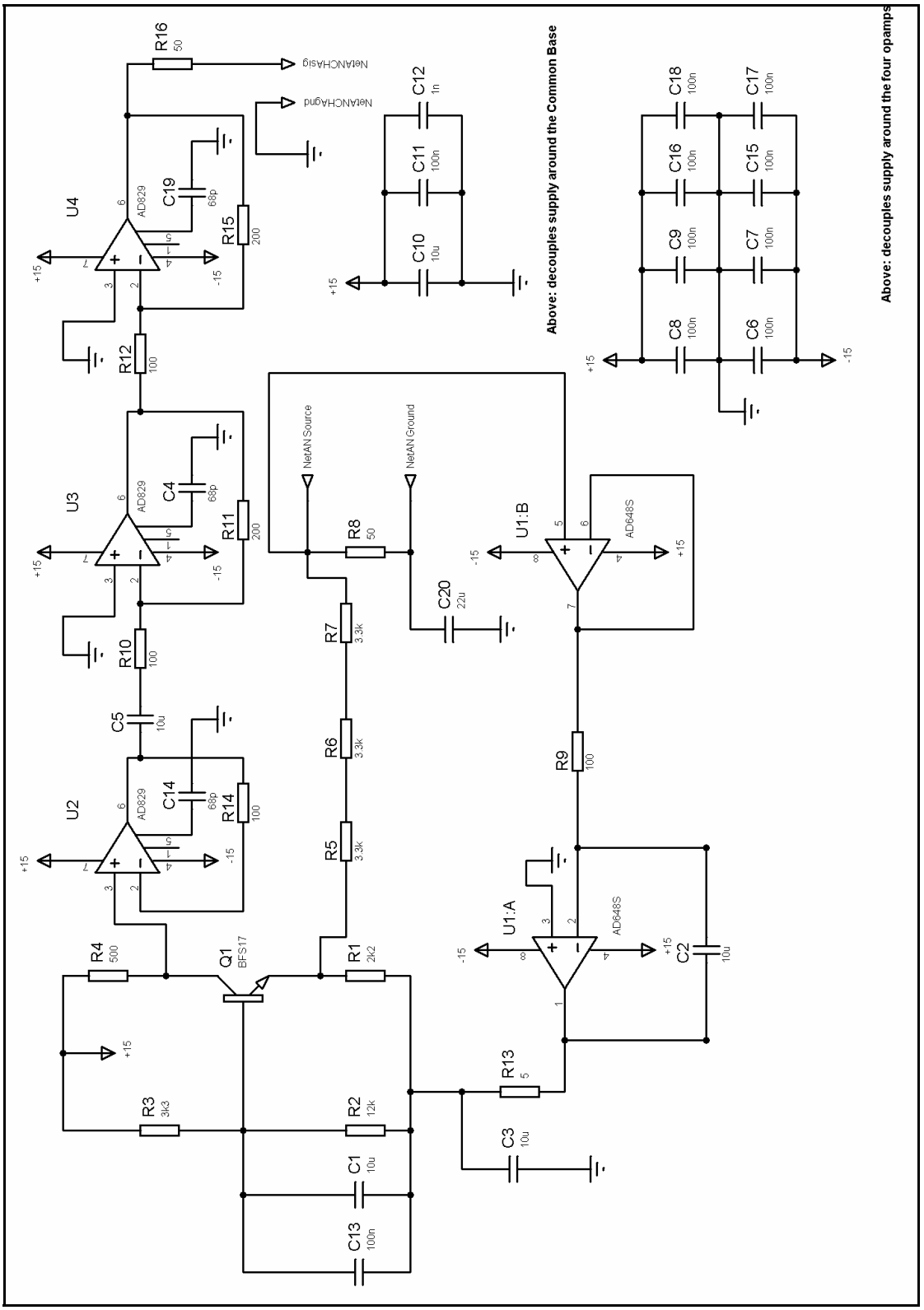


Figure 48: Design with additional gain using opamps

3. Appendix for Section 6

3.1. System Termination Layout for Characterisation of TIA

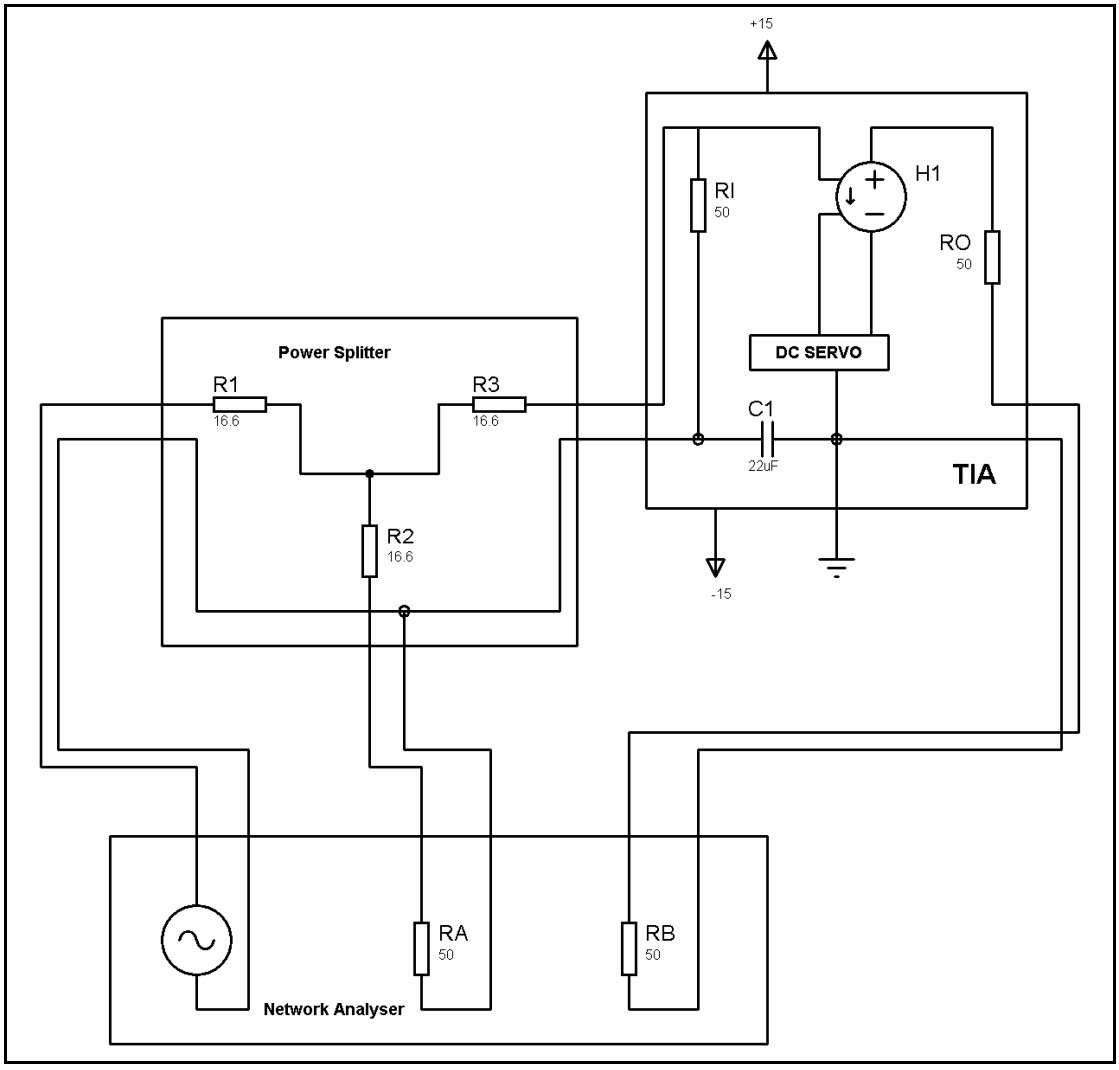


Figure 49: System Termination layout for characterisation of TIA

3.2. First Design Schematic and Results

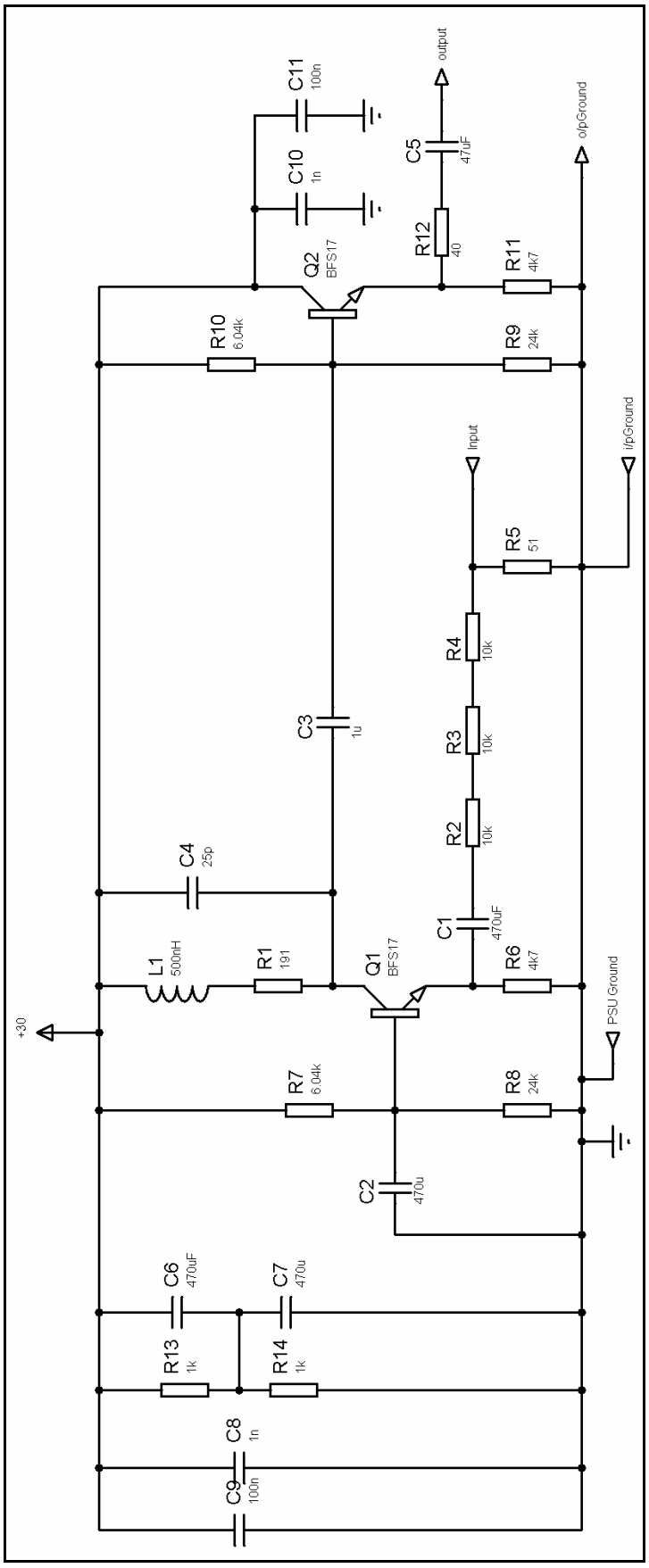


Figure 50: Design 1

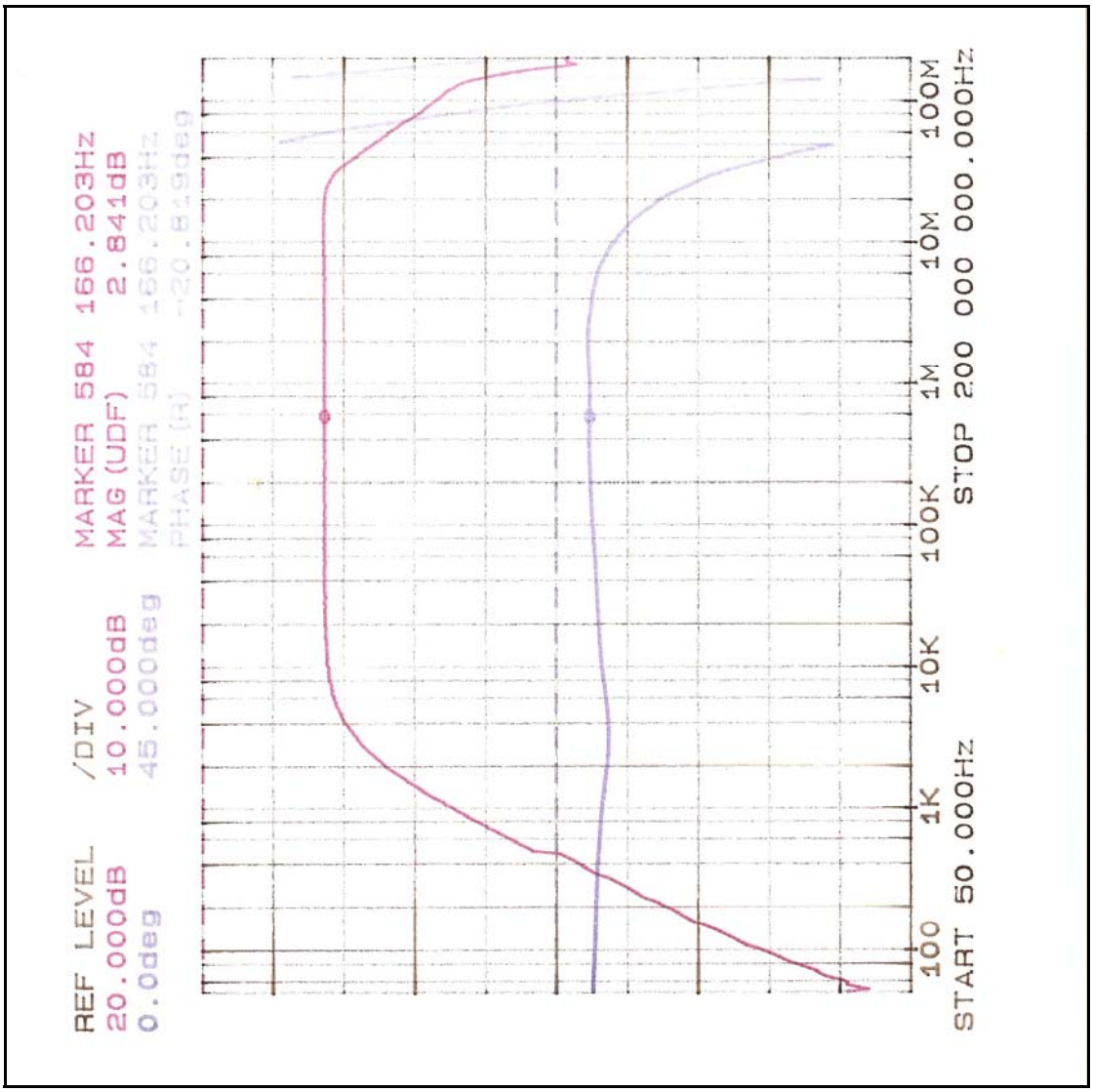


Figure 51: Series Peak Compensated Common Base Stage followed by an EF buffer.

3.3. Second Design Schematic and Results

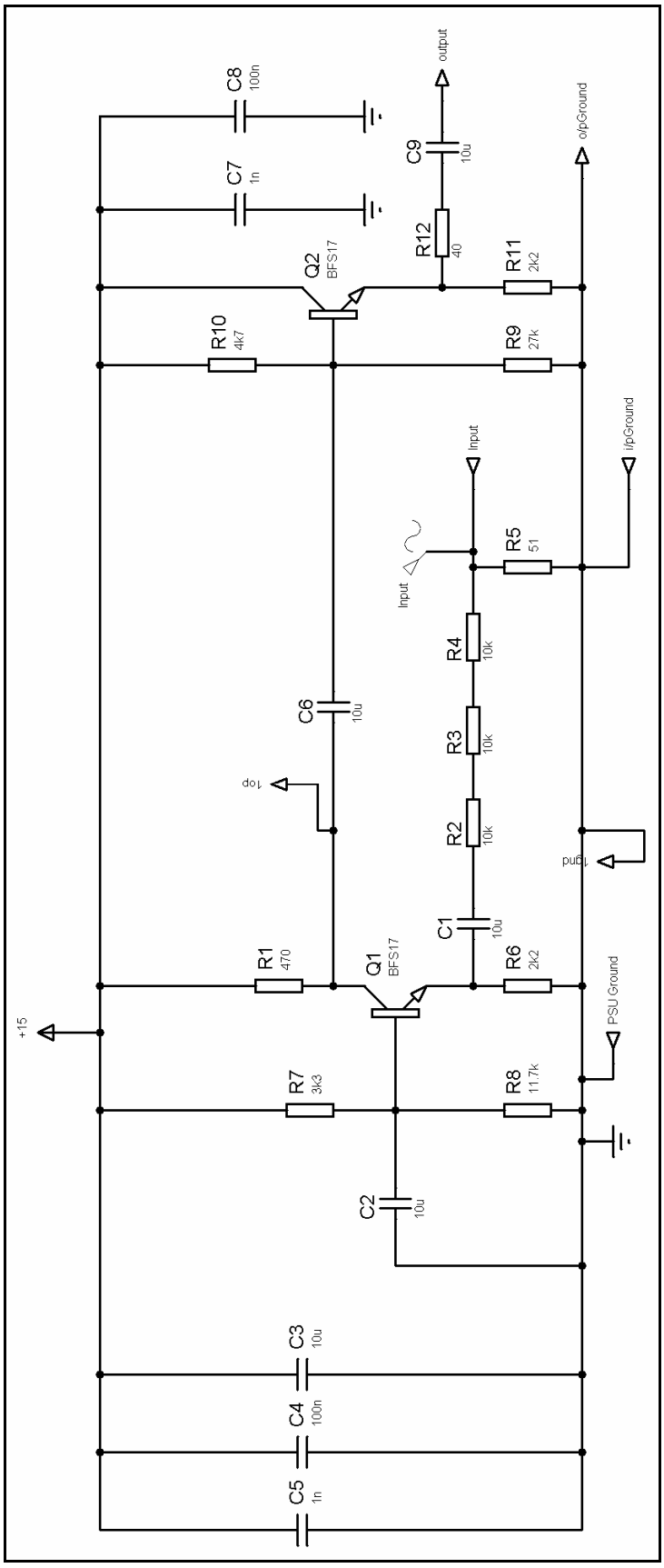


Figure 52: Design 2

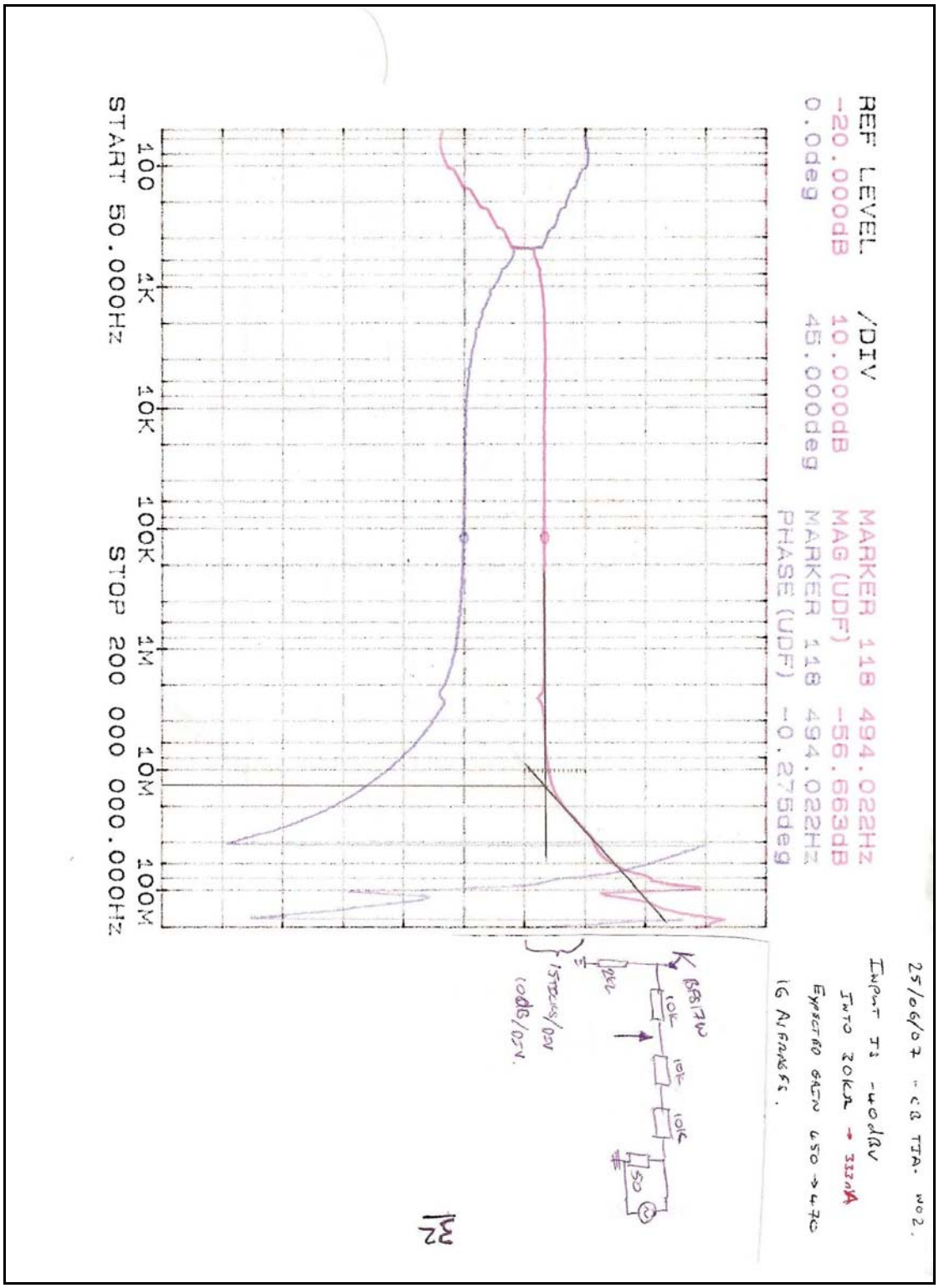


Figure 53: Plot showing effect of parasitic capacitance across the resistor chain

3.4. Third Design Schematic

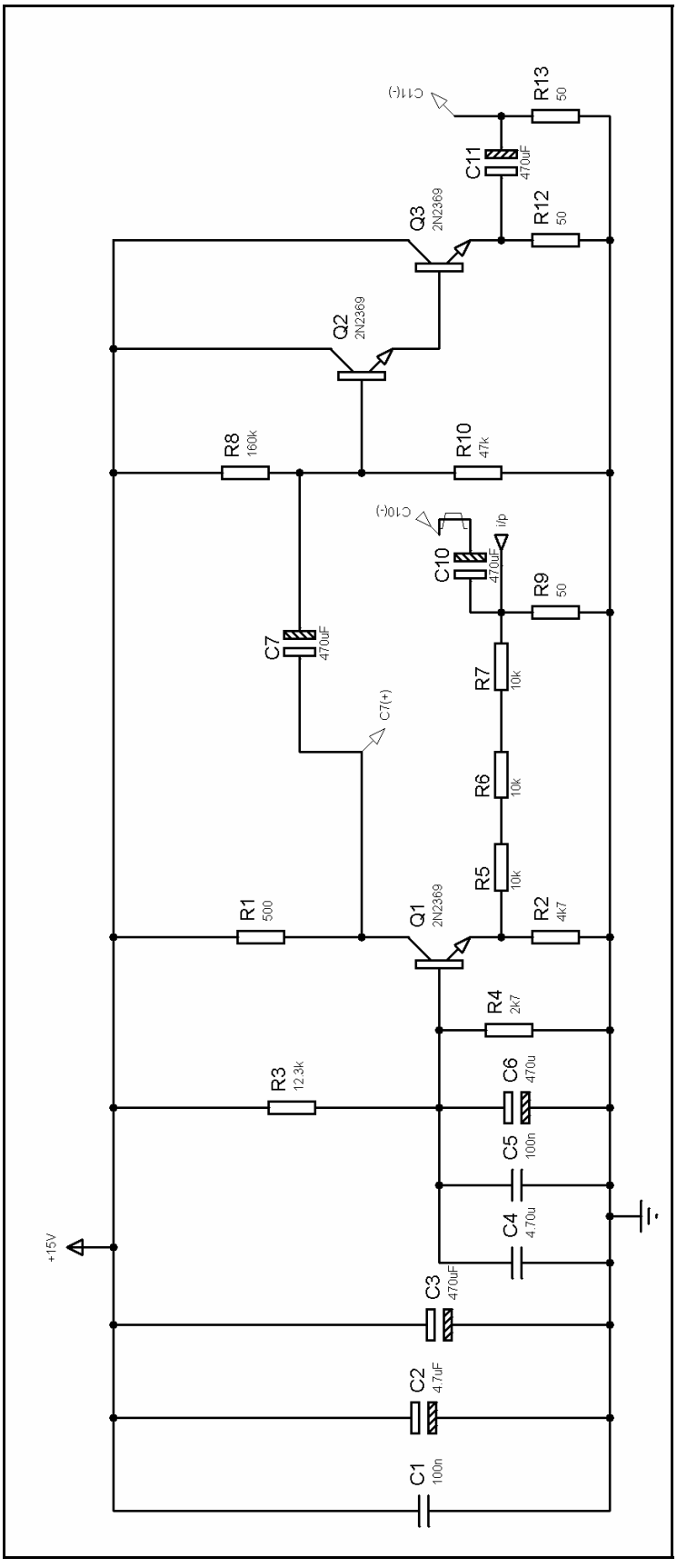


Figure 54: Design 3

3.5. Fourth Design Schematic and Results

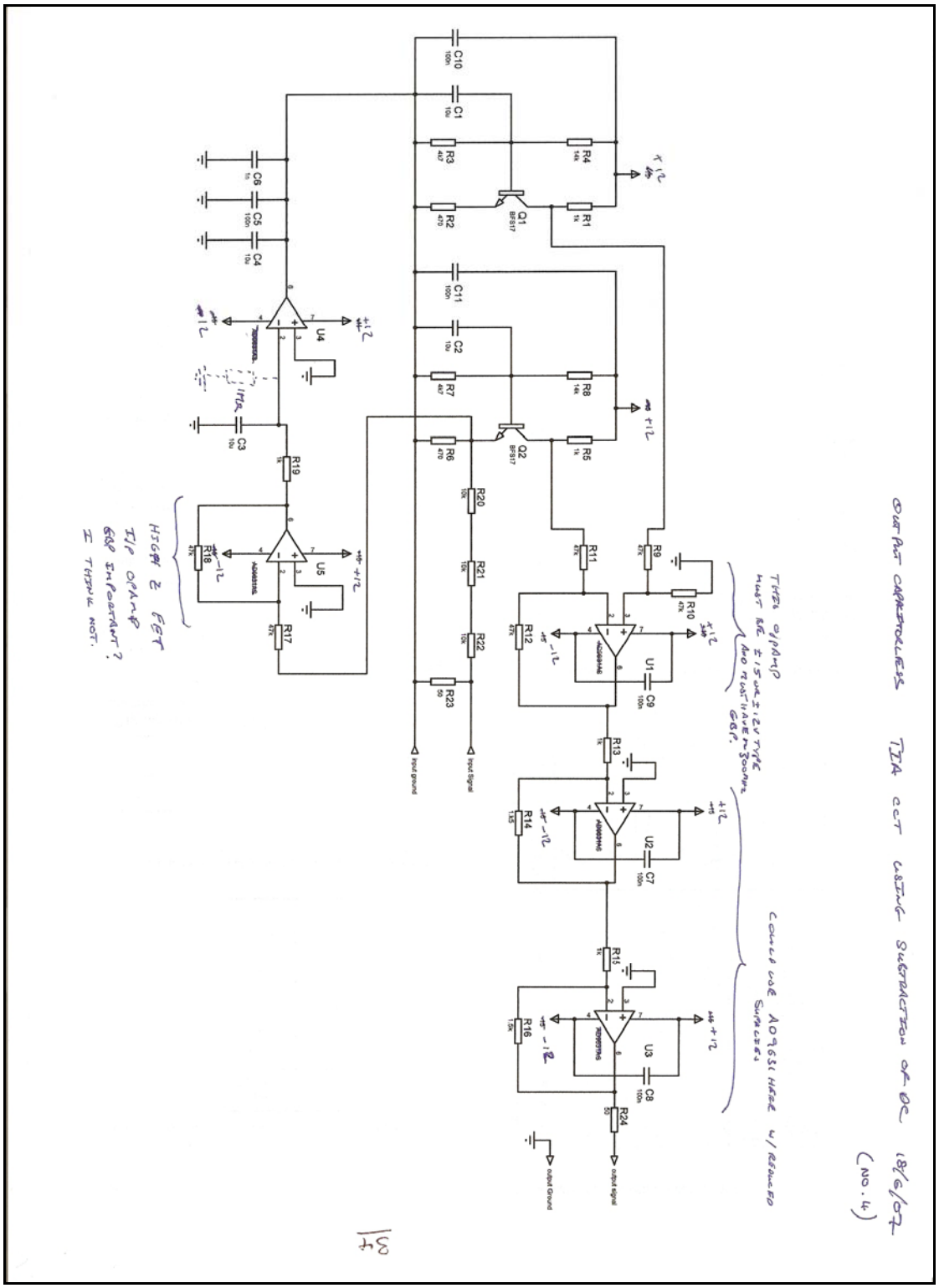


Figure 55: Design 4

3.6. Fifth Design Schematic and Spice Data

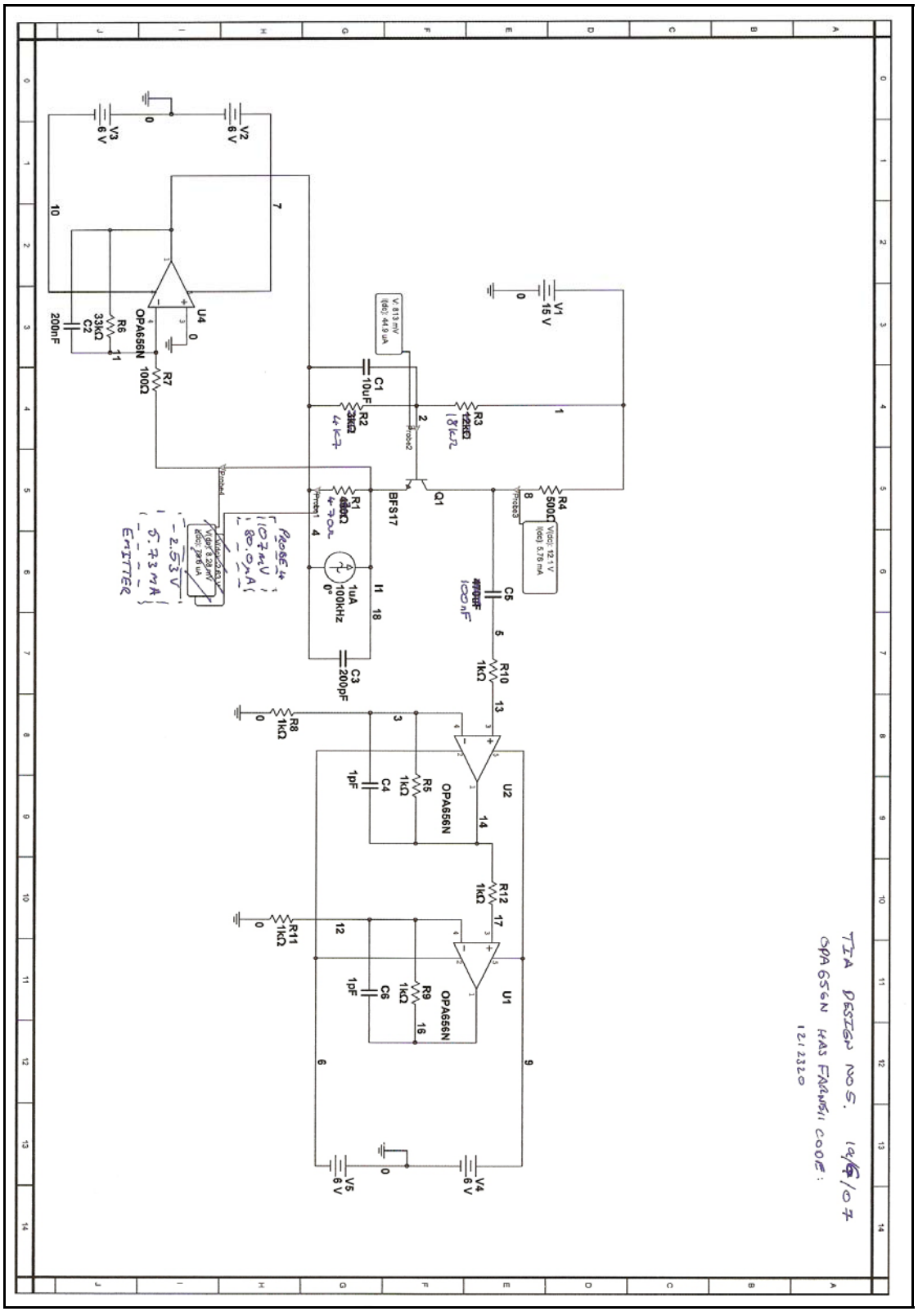


Figure 56: Design 5

In this simulation it does not matter that I1 shares a common connection with the floating rail because the source isn't grounded at its lower terminal.

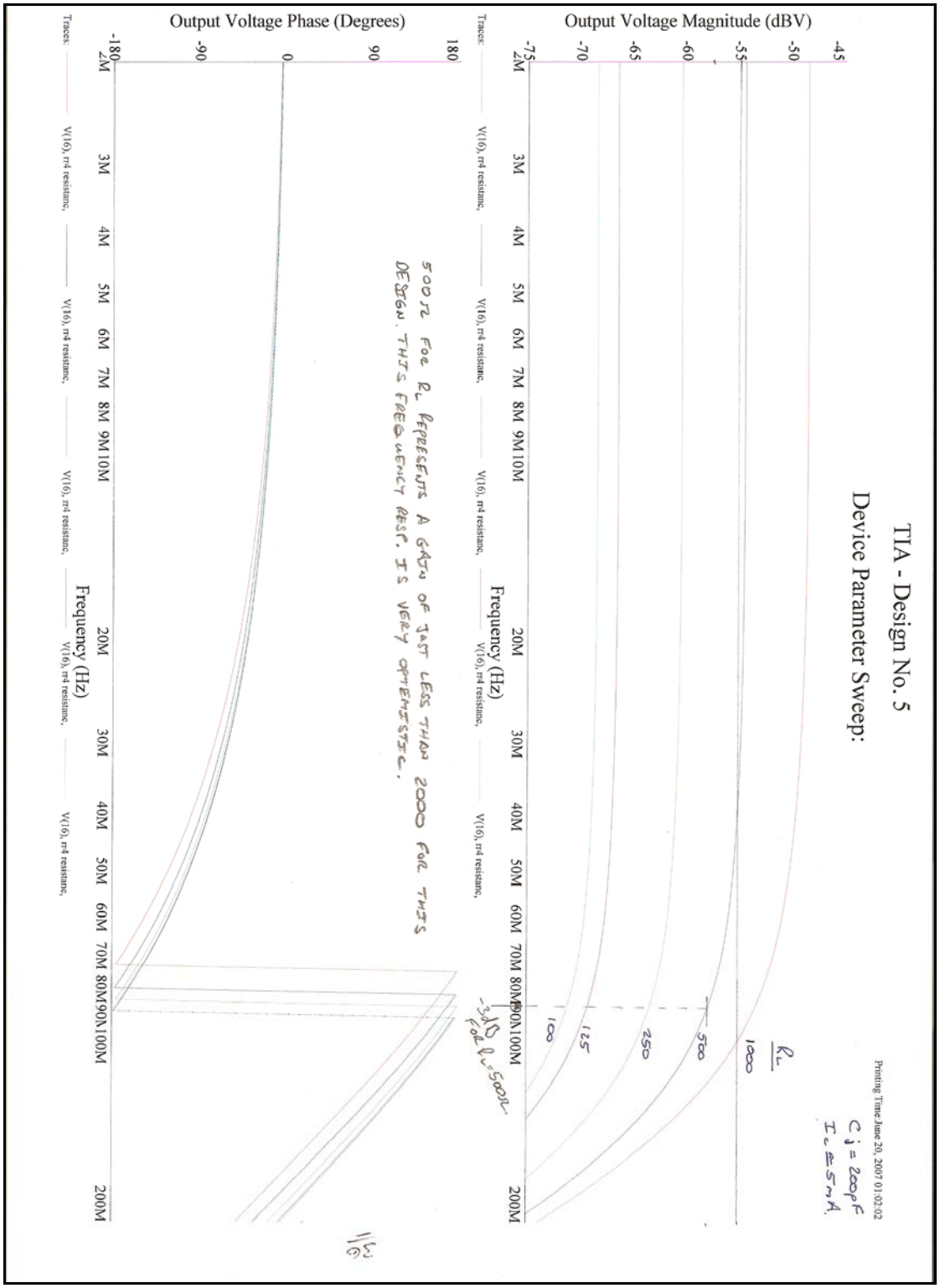


Figure 57: Design 5 SPICE Frequency Response (optemistic)

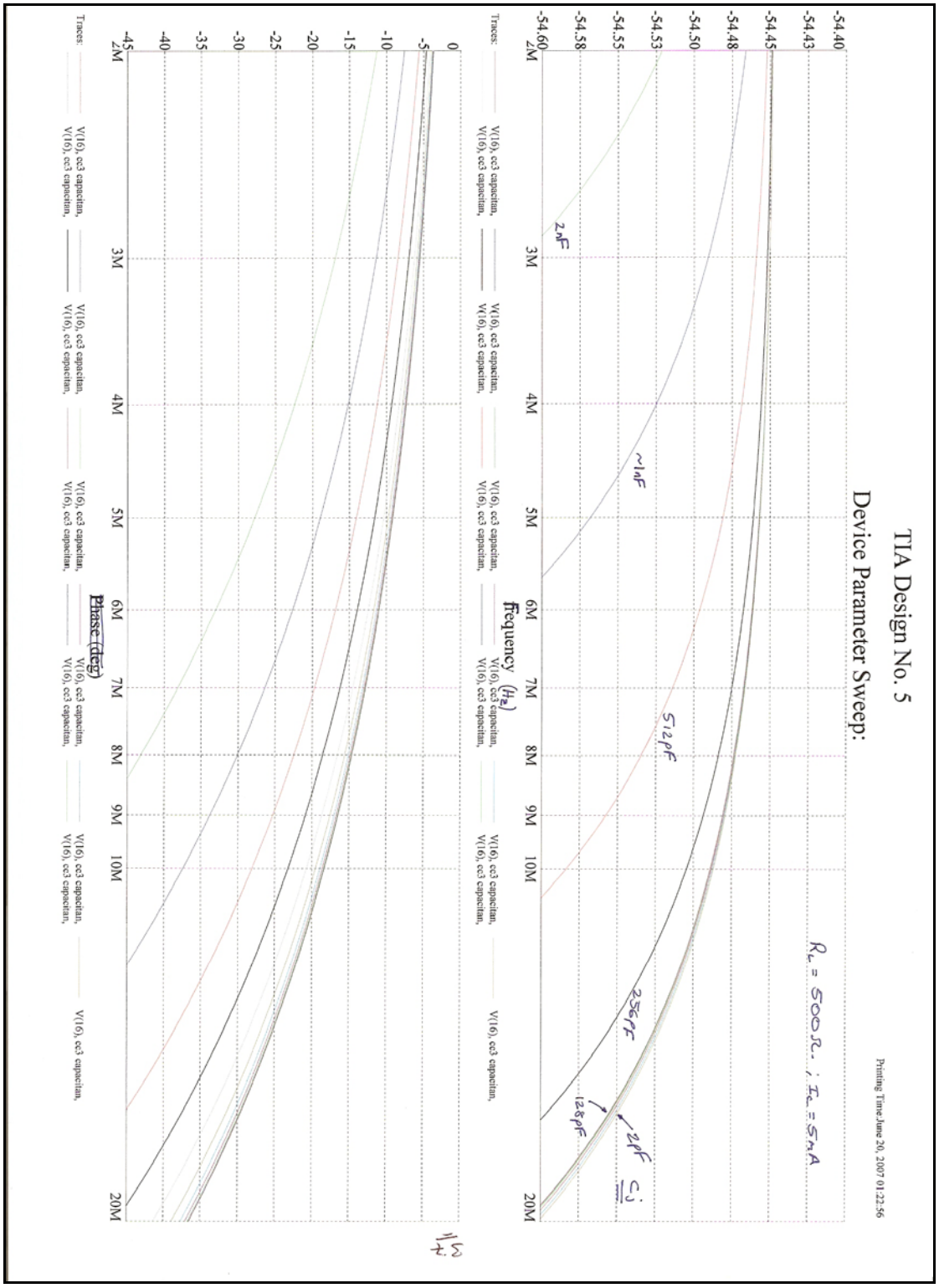


Figure 58: Design 5 Frequency Response for c_j = 2pF to c_j = 2nF R_L=500Ω

3.7. Sixth Design Schematic

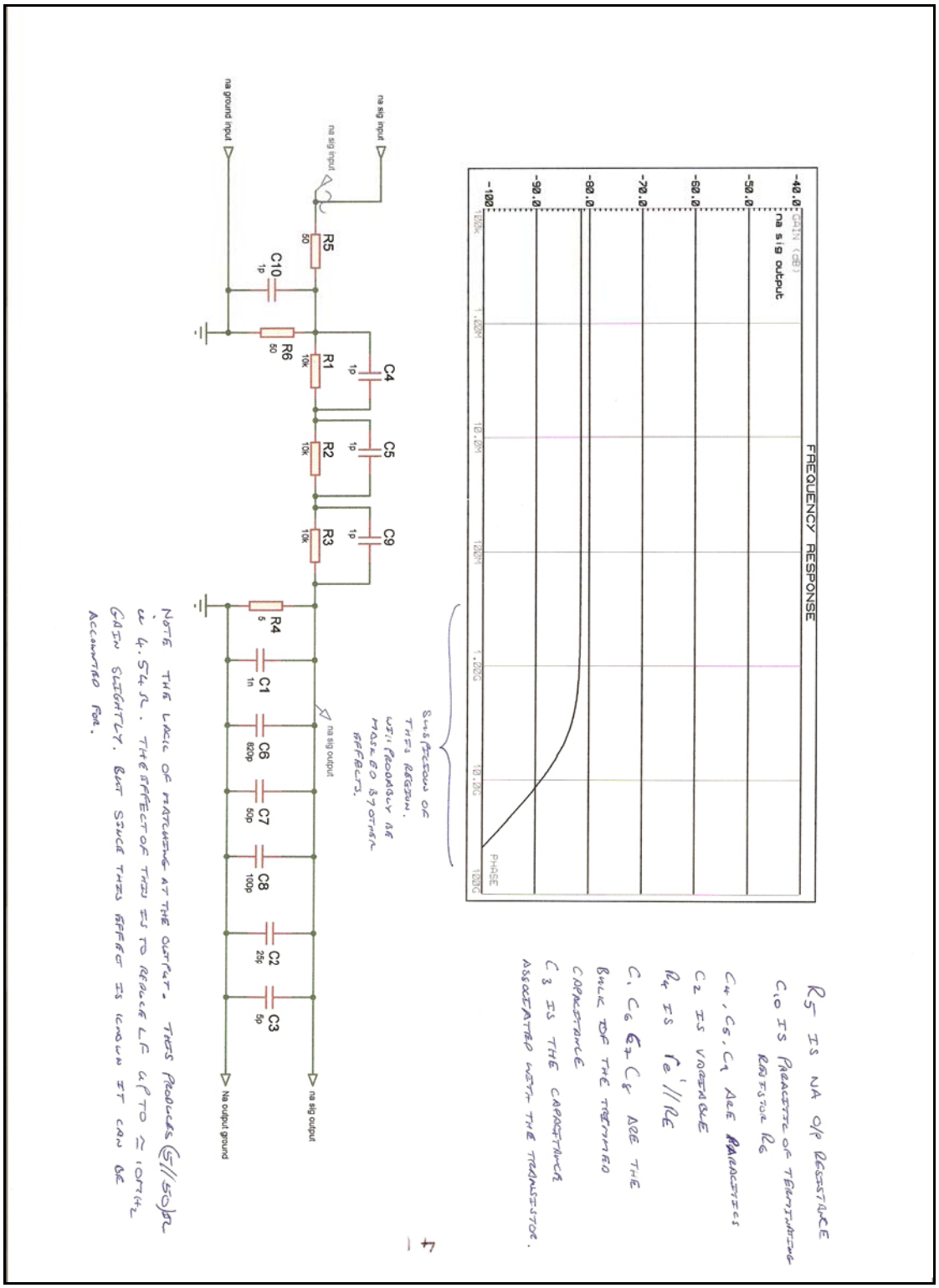


Figure 59: Design 6 - A test board to examine the possibility of correcting for the loss in HF response due to the parasitic capacitance across the resistor chain

3.8. Seventh and Eighth Schematics, Results and Simulation Data

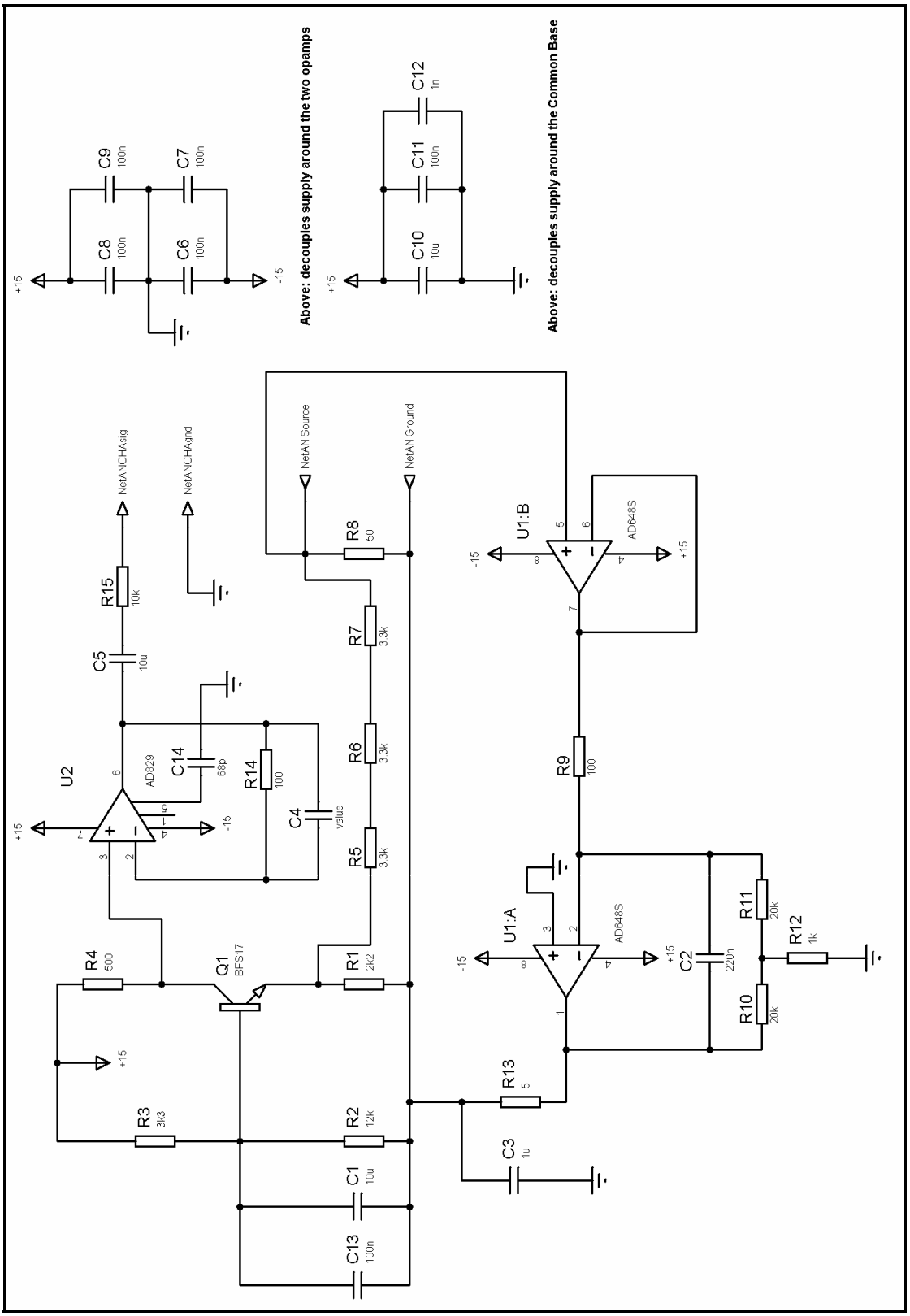


Figure 60: Design 7

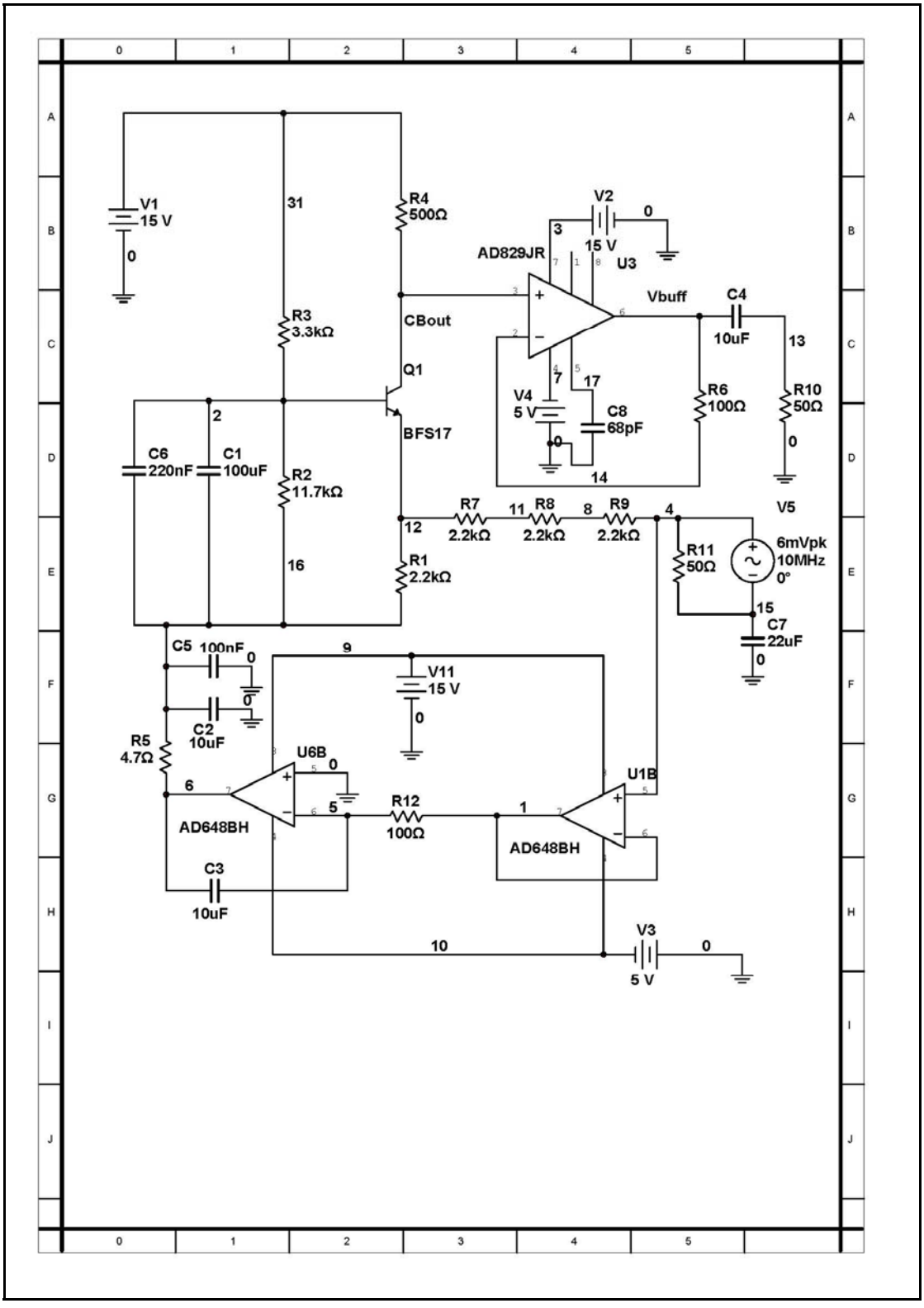


Figure 61: Design 8

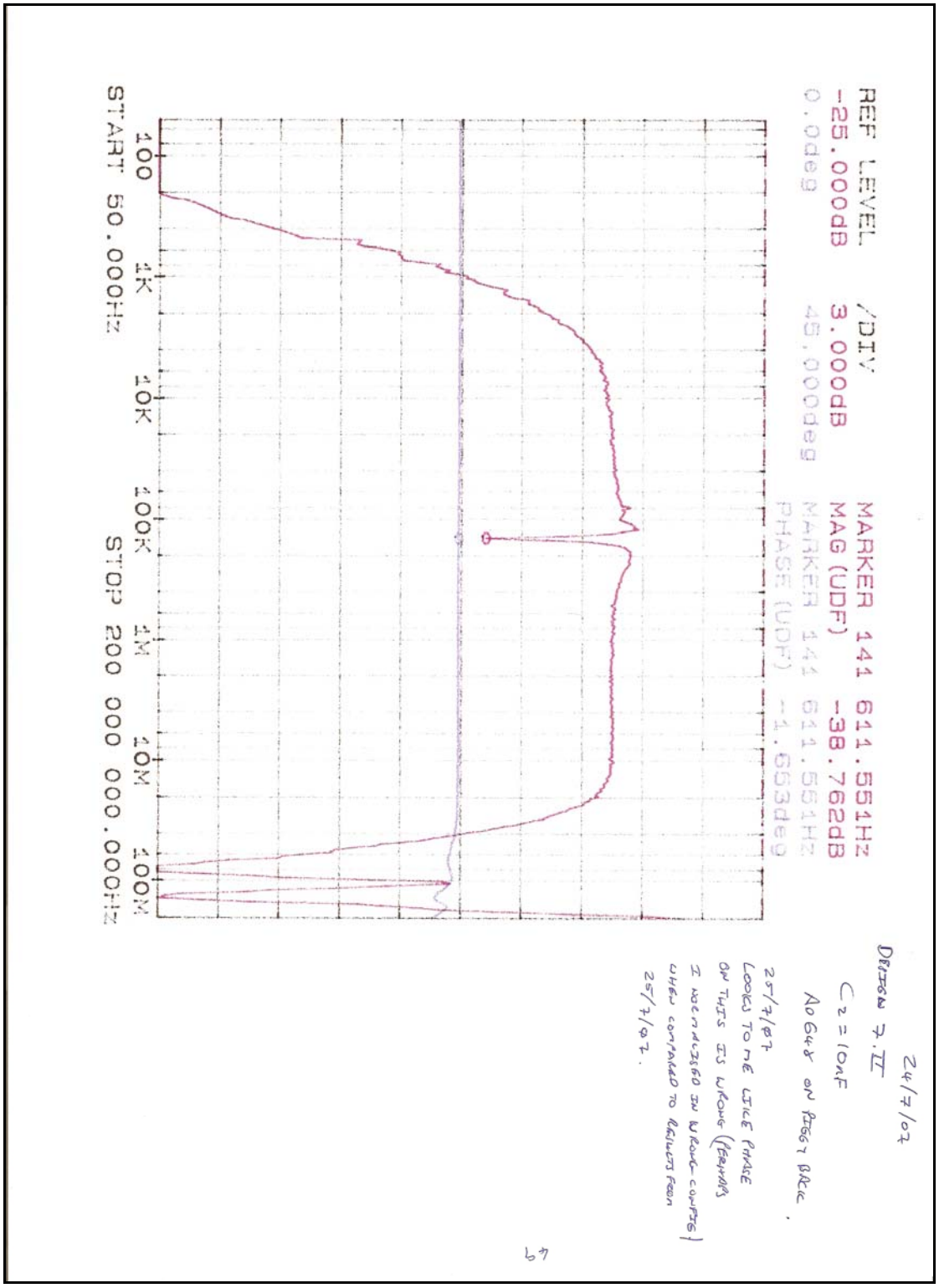


Figure 62: Result showing the Notch in the Frequency Response

Notice the phase (blue) is almost unchanging. This is wrong, it is likely that the phase trace was accidentally normalised at the wrong time.

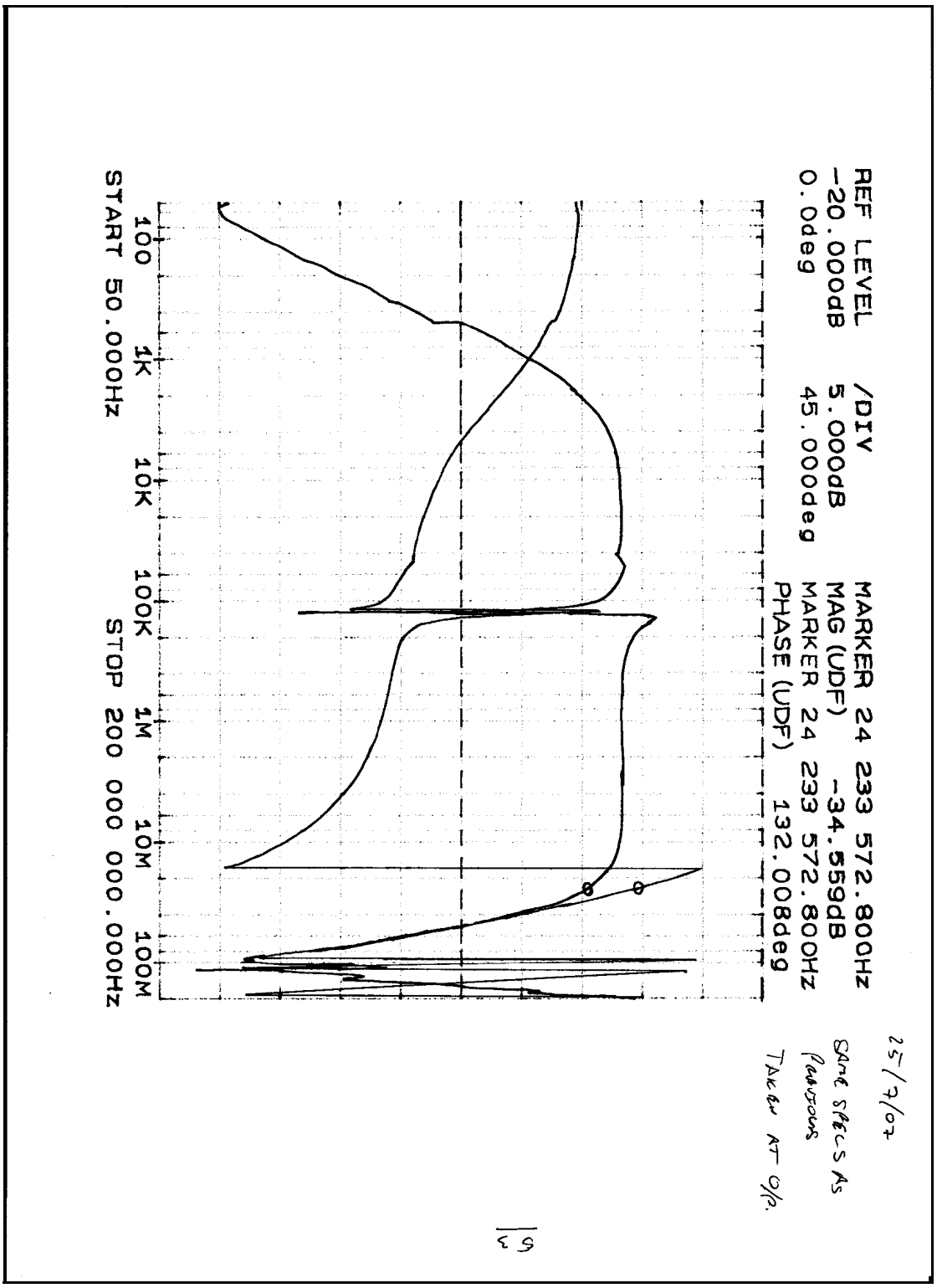


Figure 63: Result taken at the floating rail. It shows the notch in the frequency response with plausible phase. This plot has been inked (except the graticule) to aid clarity

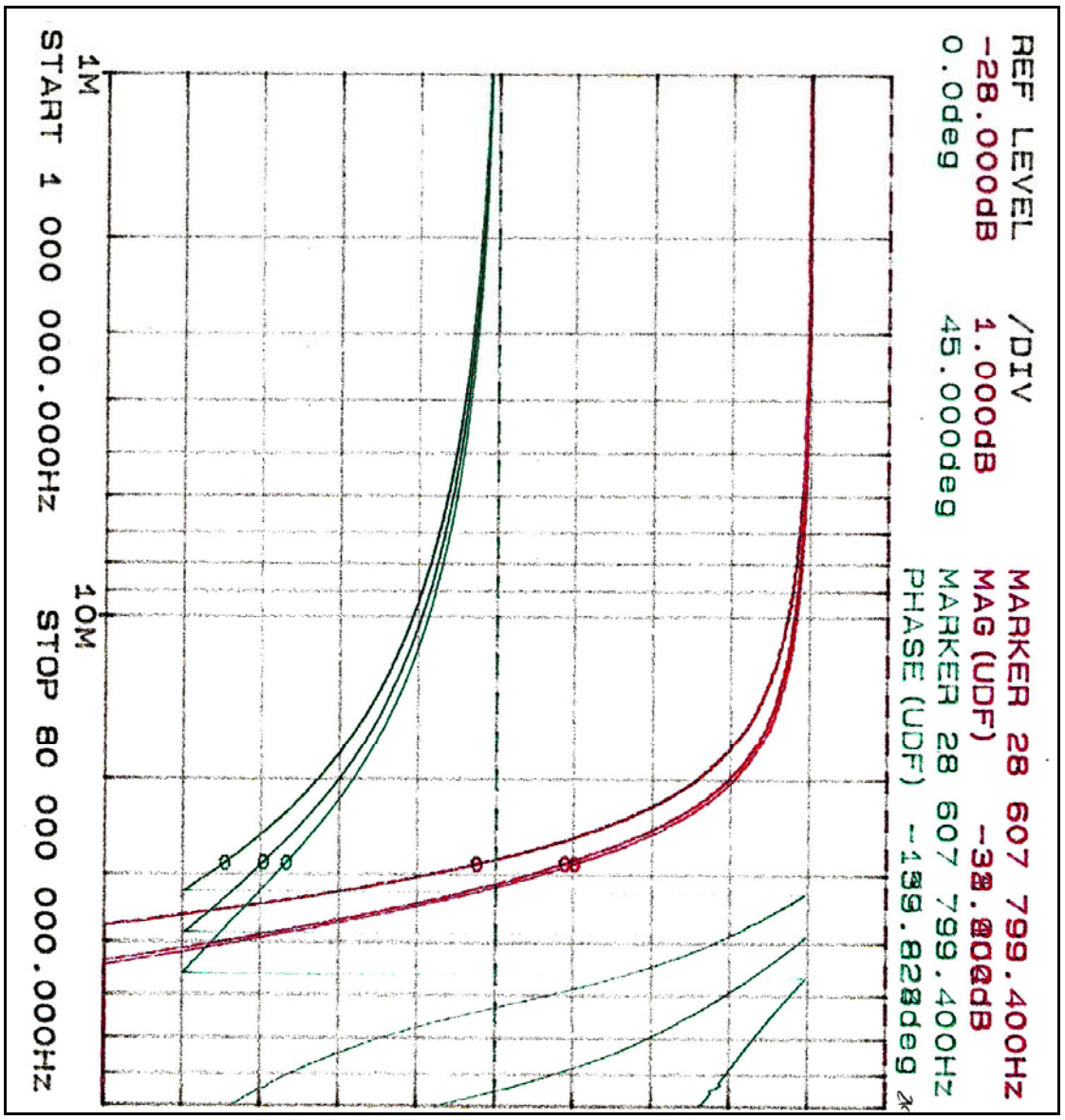


Figure 64: Three plots overlaid on a common frequency axis (using Adobe Photoshop) representing parasitic capacitance at the input, 200pF and 470pF. The mid-band gain is 262Ω. The early roll off is the only effect of added capacitance.

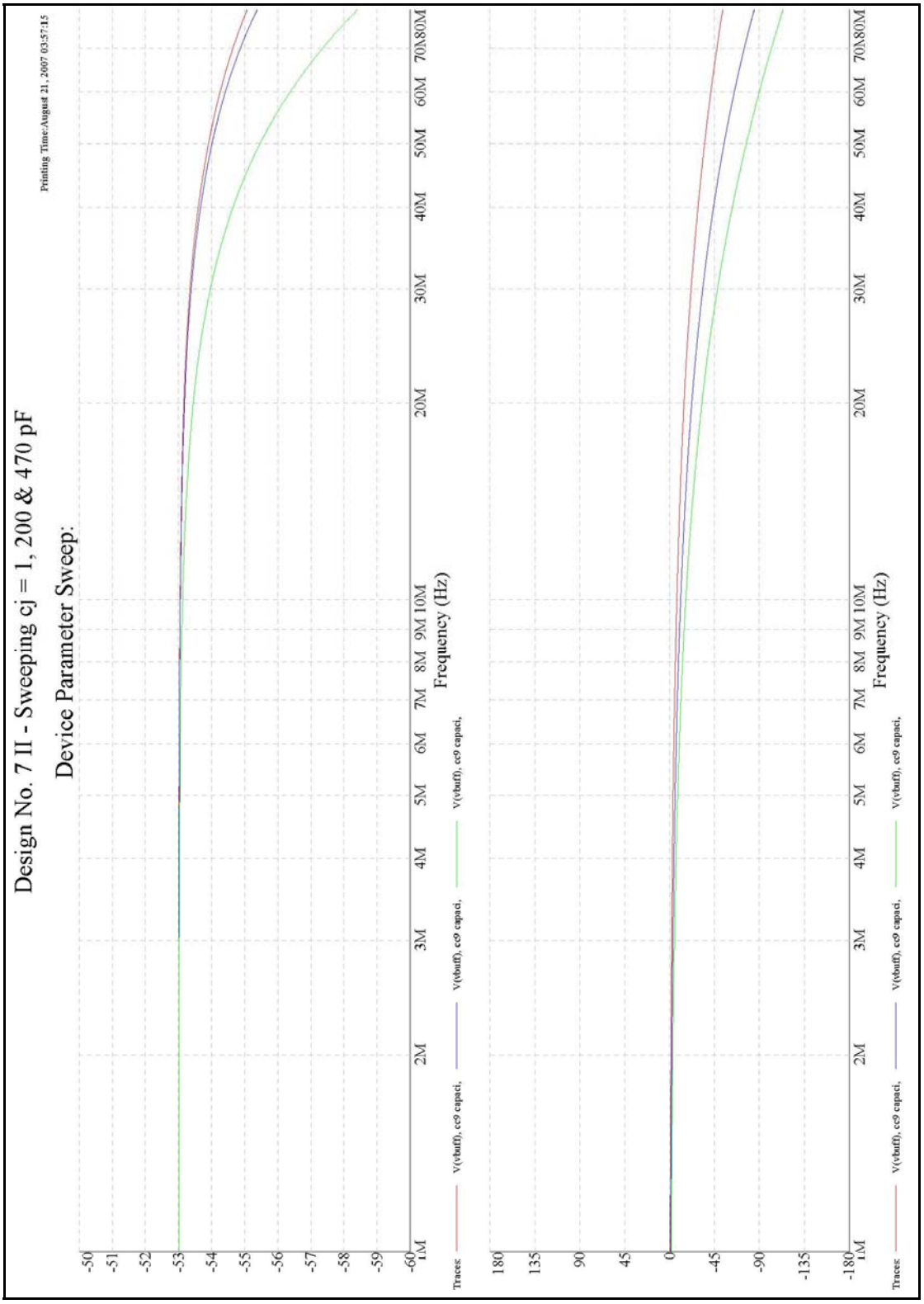


Figure 65: SPICE data generated when simulating a circuit equivalent (without parasitics) to the circuit used to generate Figure 64

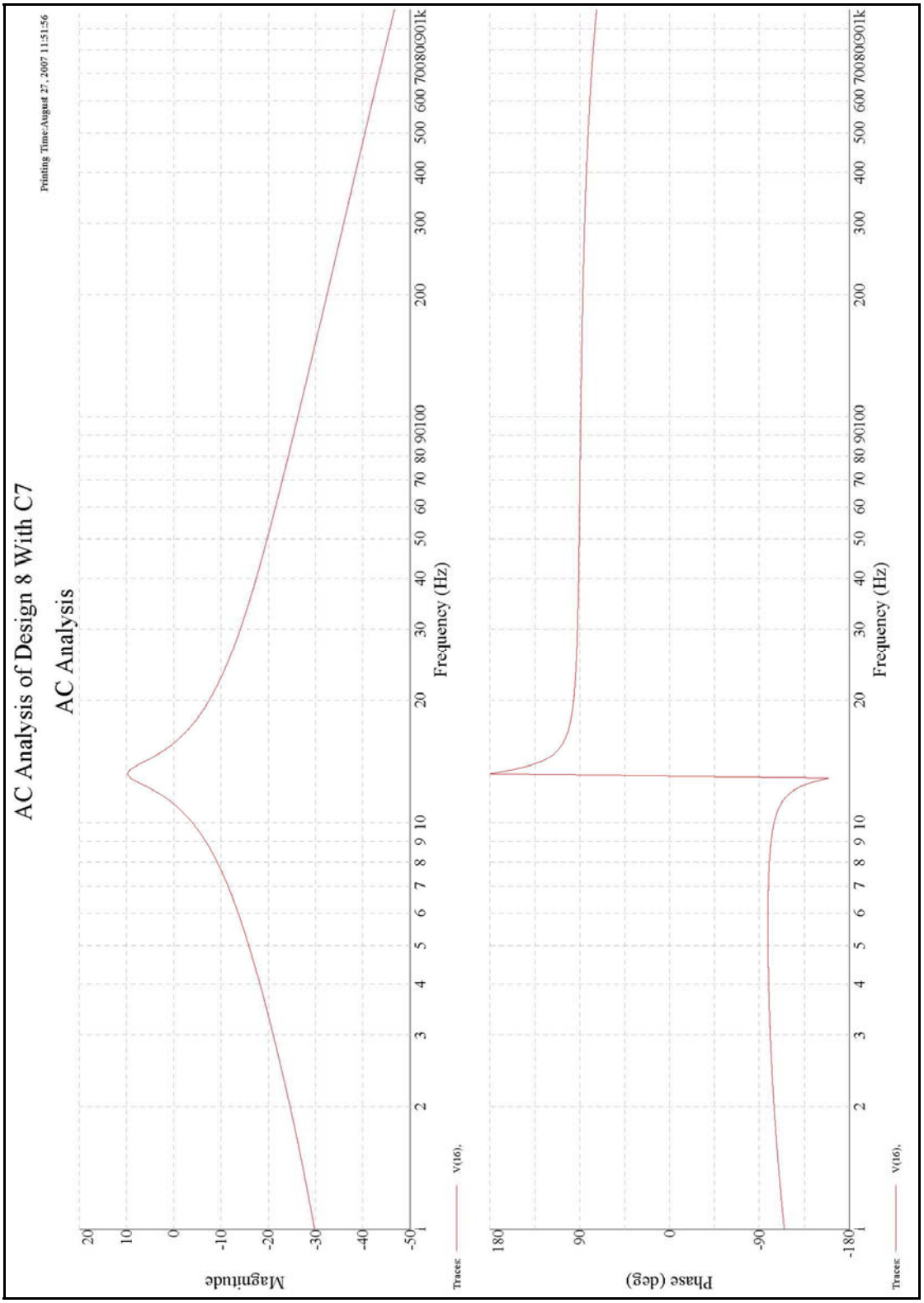


Figure 66: Response of design 8 with C7 plotted at the floating rail for a small signal at the input

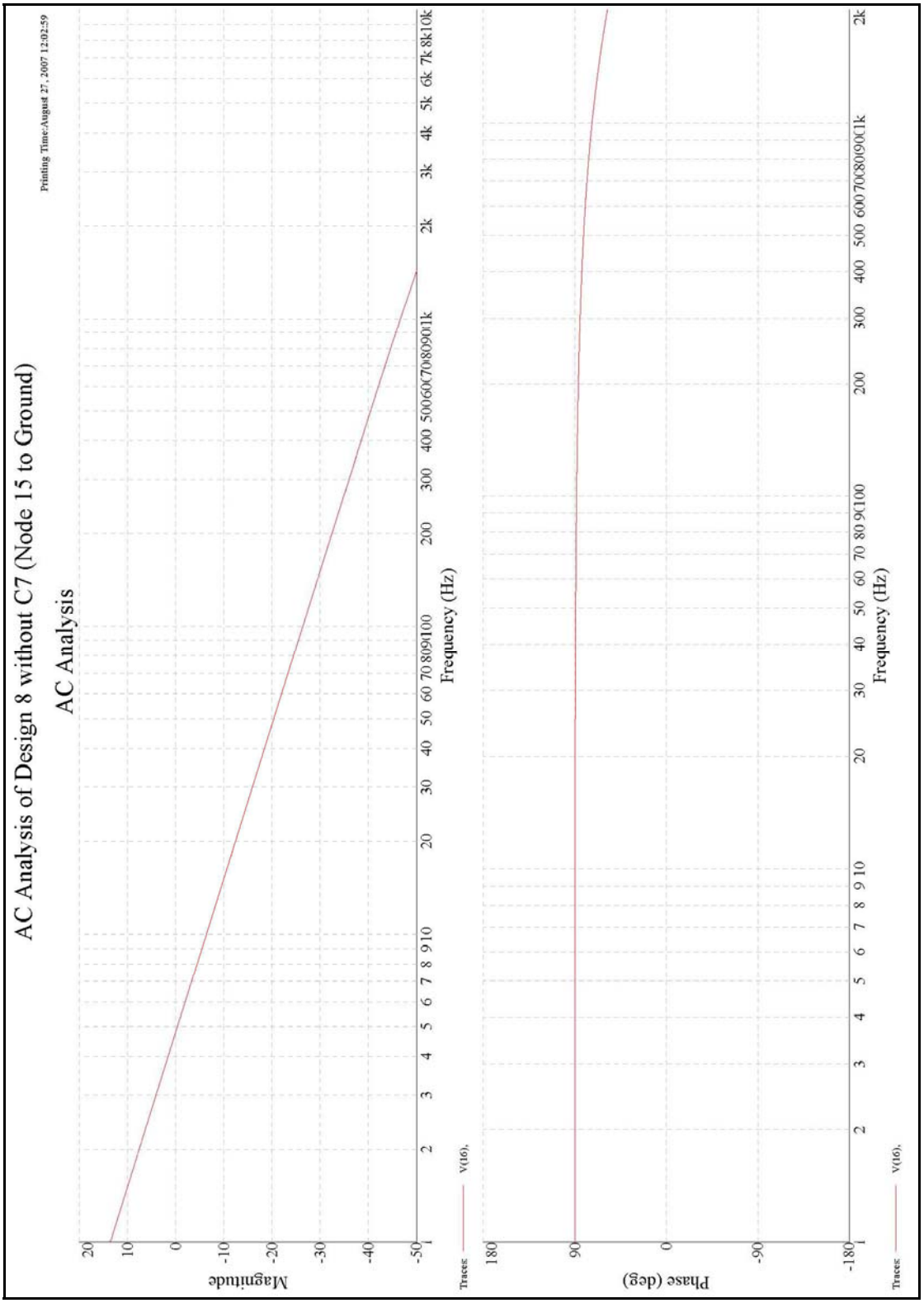


Figure 67: Design 8 without C7 Node 15 to ground graph taken at the floating rail for a small signal at the input