Why does my FET OPS Oscillate?

The following circuit is an output stage for a standard audio amplifier. The current source I1 and R5 are a transistor current source and early effect modelling resistor. V4 is a biasing circuit.V3 is the rest of the amplifier. The DC offset of V3 is just right to give plausible quiescent current conditions in the stage. L1 and L4 are the inductances of the gate connecting wires. L3 L2 R1 and R4 model the wires connecting the power supply to the amplifier. The position of R1 and L3 (and L2 and R4) can be exchanged without affecting the results. I have assumed a wire inductance of 1nH/cm. R7 and R8 are gate stopper resistors. Increasing their value may, in some cases, cause oscillation to cease. C1 and C2 are capacitances that bypass the drain of each FET to signal ground. In this case they mitigate the effects of the power supply wiring. It is often found that only the high side driver (M1) oscillates. Sensible values for gate stopper resistors are and drain capacitances are 100Ω and 220nF respectively.

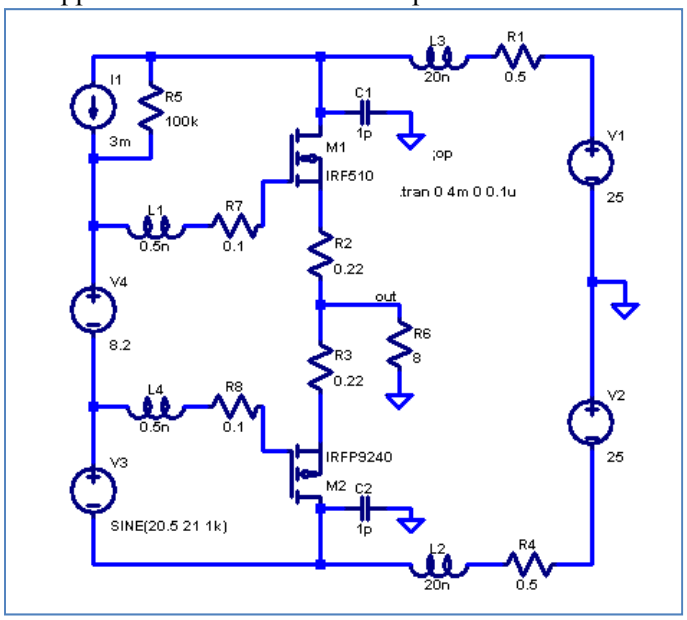


Figure 1: FET OPS with some plausible parasitic components

Simulating the circuit as shown in Figure 1 yields:

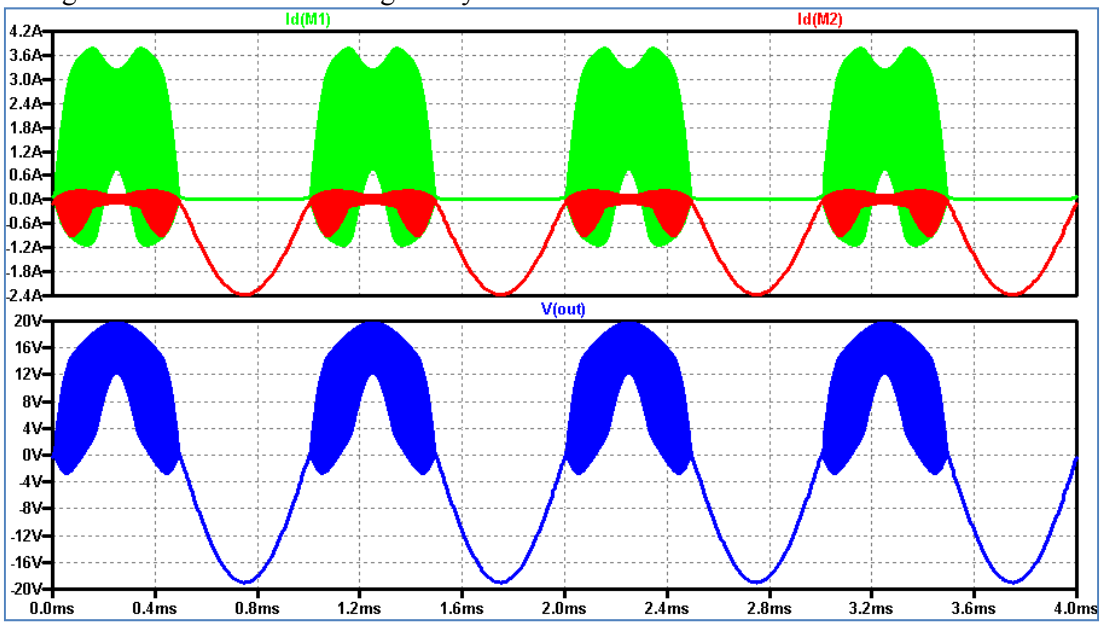


Figure 2: Oscillation is clearly visible in the output voltage (blue) and in the high side drain current (green) and to a lesser extent in the low side drain current(red).

Increasing the gate stopper resistances to 100Ω and increasing the drain capacitances to 220nF kills the oscillation, and provides a pleasant graph that describes better than words how a class B output stage works.

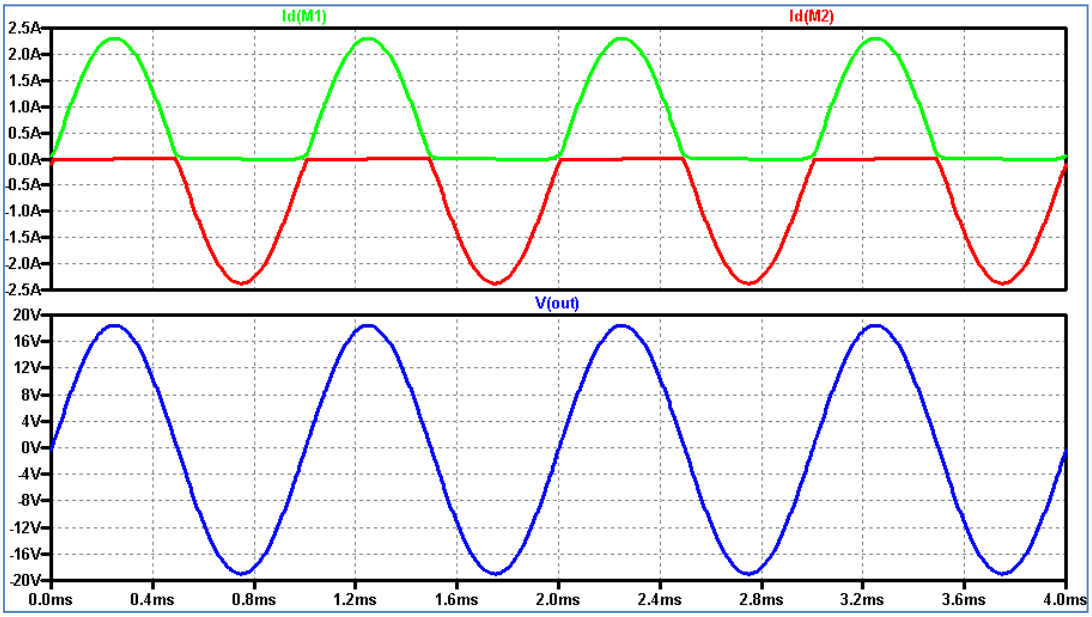


Figure 3: The oscillation has been resolved...

If you simulate this particular circuit, you'll find that it'll oscillate happily without a gate leg inductance (provided no stopper is present and no drain bypass capacitance is present). You'll also find that either a gate stopper OR a drain capacitance will kill the oscillation. This is sometimes normal, but if the physical distances are large or you are particularly unlucky both will be required.

It's hard to *accurately* simulate parasitic effects such as this without expending a lot of time and effort figuring out exactly where each parasitic component is and what its value is likely to be. It is, with sufficient effort, and the right design tools, possible though. Not all oscillation problems in FET circuits take the form shown above. There are lots of ways to get a circuit with active components to oscillate, this is just an example.

When designing PCBs for FET circuits it is standard practice to fit bypassing capacitors to the drains, and to provide a space for a gate stopper resistor, even if you end up putting a wire link in it. You may wish to consider why, in some circumstances not having a gate stopper if you don't absolutely need one is desirable.